Notes from Interview with John Reed
Regarding Development of Intel 1103 1Kb DRAM

Jeff Katz 24 Jan 2007

SUMMARY

We met in John's office for about 90 min, and discussed his recollections of the development of Intel's 1103 DRAM, for which he was the lead engineer during the phase of design completion and production start. John was at Intel from June 1970 through late 1971.

WHO DID WHAT IN EARLY DRAM DEVELOPMENT?

John recalled several early contributors to DRAM technology that preceded Intel's efforts which began in 1969:

1963 **Howard Bogert**, then working at General Micro Electronics patented the idea of storing charge on an MOS transistor. (Later John worked for Bogert at AMI before he worked at Intel.)

1968 **Dennard** at IBM patented a 1-Transistor DRAM cell.

68-69 **Sven Wahlstrom and Alton Christianson**, then working for Shell Oil , developed (and patented?) a 3-Transistor cell with balanced sense amps. Shell was interested in having a 100 nsec cycle CPU to capture and analyze oil field exploration data. Existing Core memory systems simply weren't fast enough.

HOW DID INTEL GET INVOLVED IN DRAM DEVELOPMENT?

In 1969 Honeywell engineer **Bill Regitz**, then working for **Bill Jordan**, was seeking a supplier to make his idea of a 512b 3T-cell MOS DRAM. Most semiconductor suppliers were not forthcoming, preferring to concentrate on bipolar SRAMs. Intel did show interest, with **Joel Karp** and his boss **Leslie Vadasz** getting very excited over the possibilities. Intel at the time was also working on bipolar SRAMs. (Later both Regitz and Jordan worked for Intel in memory components and systems.)

Karp and Vadasz suggested to Honeywell that the proposed project could instead be a 1Kb product. They proceeded to develop it, the 1102. When the device emerged it worked, but not very well, having very poor margins and yields stemming from a hard-to-make butted contact, and requiring substrate bias voltage that originally hadn't been planned. This required an extra power supply pin on the package, and the project had to stop and change from a 16 pin to an 18 pin DIP. Part way through the project, John believes during a return flight from visiting Honeywell, Karp and Vadasz discussed making an improved version with a different X-Y architecture that could take advantage of a new easier-to-make buried contact to greatly improve the yield and margins. Without telling Honeywell (but with the support of senior Intel management) Intel quietly started the 1103 project. Karp continued to work with Honeywell, and newly hired engineer **Bob Abbott** was assigned to develop the 1103., in late 69 or early 70.

JOHN REED'S 1103 CONTRIBUTIONS

John came to Intel in June 1970, and was first assigned to work on a custom 512b SRAM for customer Ampex. When Abbott had gotten the 1103 to the point of design and layout completion, John was assigned to take over the project, and make the product work. The first silicon didn't work well at all, having extremely critical timing requirements between two of the clock signals, Precharge and Cenable, which gave the device essentially zero operating margins. Though Reed and his boss Vadasz both declared the device not yet production-worthy, the marketing V.P. **Bob Graham** insisted that it should be introduced anyway to get a jump on the competition. Graham won the argument. The strategy worked. While the product was alone in the market during its introductory phase, John continued to improve it step-by-step until at about the 4th or 5th revision it was performing and yielding well, just as the production demand soared.

John recalls that when his first revision was expected out of the fab, he was working late on a Friday evening. Vadasz began calling him from what was apparently a party he was attending, asking "Is it out yet?" every half hour or so. When the wafer finally emerged around 2AM, long after Vadasz had given up, John was virtually alone in the lab and had to learn on his own how to dice the wafer by hand.

John's project schedule had a few basic milestones:

Design tape-out
Wafer out of Fab
Chip works
Champagne party

He recalls that Andy Grove and Les Vadasz did indeed bring champagne to celebrate the greatly improved yield, at about the "C" revision.

There was a moment of truth at Honeywell when the customer had to be told that their original idea, which resulted in the poor yielding 1102, was inferior to the new 1103. **Bob Noyce,** Marketing VP **Bob O'Hare**, and John Reed went to Honeywell's Framingham HQ to present the news in late 70 or early 71. John recalls doing his technical pitch for 1103 superiority before about 35 un-receptive Honeywell engineers who didn't like what they were hearing. Then Noyce got up and used his typical charismatic charm to convince the customers they should switch to 1103.

OTHER 1103 PROJECT CONTRIBUTORS

The development team was small: John was the lead engineer; **Paul Metrovich** (a recent Intel retiree?) was his technician; **Pat Earhart** did the layout, and **Barbara Maness** and **Judy Garcia** were Ruby-cutters. Test Engineer **George Staudacher** was responsible for empirically discovering the critical timing in the original revision; the "fix" wasn't easy to achieve, requiring a couple of mask-revision cycles before a reasonable level of yield was reached. Along the way, a Honeywell engineer, **Hank Bodio**, made some contributions towards solving the problem. One of the problem aspects that he discovered was called from then on, the "Bodio Effect."

JOHN'S LATER CONTRIBUTIONS IN DRAMs

Following the 1103 project, John worked on a dual-purpose Intel project to make both a 1KB SRAM and a 1Kb 4T-cell DRAM. These used N-channel technology, more amenable to easy system interface. These were the 2102 and 2105, respectively. The 2105 was designed to be

fast enough to be used in mainframe add-on memory boards. It came out and it worked, but it was not successful. Competitor AMS had a better, faster part for mainframe add-ons.

Disliking Intel's intense focus on problem areas, along with minimal recognition of successes, an environment John described as "negativity", he left the company in late 71.

Remaining at Intel, Karp and newly hired Regitz developed the 4Kb 2107 DRAM. This device had many improvements, including on-chip intermediate-voltage generation for simpler system interface. It also used a more size-efficient 1X-1Y architecture, which happened to make it more vulnerable to soft errors due to alpha particle disturbances. That phenomenon was first described by a team of Western Electric engineers who were evaluating 2107-based systems. (John referred to a paper by Intel engineer **Timothy May**, published in ~78, which described the problem and its implications for semiconductor memory in general.)

Later (1974) Karp joined Reed in a DRAM consultancy. Among their early developments/accomplishments, they were jointly responsible for inventing what Foss later named the "Folded Bit Line" architecture, on behalf of client Burroughs Corporation, in 1974. Another one of their clients was National Semiconductor, whose engineer Ilbok Lee had come from Intel in late 1977. Lee was constrained by NDA from his Intel departure to not discuss the soft error phenomenon or its causes or cures. But he told Karp and Reed, and other National engineers, that there was a lower limit to the size of memory cell capacitor they should be considering.

OTHER POTENTIAL SOURCES FOR STORIES ON EARLY SEMICONDUCTOR MEMORY

J. Reese Brown, a component manager at Burroughs Piscataway in the 70s, who kept tabs on all semiconductor memory suppliers. John suggested this last known phone number for Brown: 619-434-7724.

Fairchild memory designers: **Gil Amelio, Hsing Tuan, John Chan, Mark Guidry**

National Semi memory designer: **Dale Mrazek**

OTHER ITEMS

John loaned me several original documents on the early Intel DRAMs for archival scanning at the museum:

1103 data sheet Oct 1970 (with JR's hand written changes showing "b" step parameters)
1103 technical brochure Oct 1970
1103 revised data sheet July 1971
1101A data sheet Sept 1971
2105 data sheet July 1973

Should the CHM Semiconductor SIG decide to an Oral History panel discussion on early DRAMs, John would be a candidate participant.