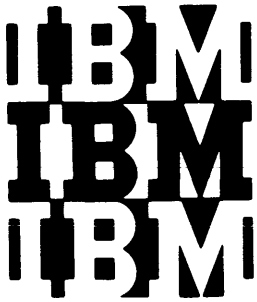

File Number S360-30 (OS)
Order Number GY28-6616-9

Program Logic

OS I/O Supervisor Logic

Release 21

Program Number 360S-CI-505

This publication describes the input/output supervisor, which consists of the control program routines that carry on input/output activity for the IBM Operating System. Input/output supervisor routines start, monitor, and, where necessary, restart activity on input/output devices. Following an introduction, there is a Method of Operation section in this publication which is organized to reflect the sequence of events that takes place when the input/output supervisor receives a request for input/output (I/O) activity:

- Validating Input Data
- Scheduling I/O Operations
- Starting I/O Operations
- Terminating I/O Operations
- Restarting I/O Operations
- Recording Error Data

The remaining sections of this publication support the Method of Operation section, and include descriptions of program organization, directories for PLM-to-listing and listing-to-PLM transitions, descriptions of data areas, diagnostic aids, and appendixes.

This manual is intended for persons involved in program maintenance, and system programmers who are altering the program design. Program logic information is not necessary for the use and operation of the program.

Tenth Edition (February 1972)

This edition, as amended by technical newsletter GN26-8036, applies to Release 21.7 of the Operating System (OS) and to all subsequent releases until otherwise indicated in new editions or technical newsletters.

Information in this publication is subject to significant change. Any such changes will be published in new editions or technical newsletters. Before using the publication, consult the latest *IBM System/360* and *System/370 Bibliography,* GA22-6822, and the technical newsletters that amend that bibliography, to learn which editions and technical newsletters are applicable and current.

Requests for copies of IBM publications should be made to the IBM branch office that serves you.

Forms for readers' comments are provided at the back of the publication. If the forms have been removed, comments may be addressed to IBM Corporation, Programming Center--Publishing, Department D58, Monterey and Cottle Roads, San Jose, California 95193. All comments become the property of IBM.

PREFACE

This publication, when used in conjunction with program listings, will enable you to understand enough about the input/output (I/O) supervisor to be able to make changes to it.

The publication relies heavily on operation diagrams that show how the I/O supervisor operates and identify the routines that perform the operations. The operation diagrams are keyed to other parts of the publications. For further information, you can refer to flowcharts or, via a directory of symbolic names, to the program listing.

This manual is not designed to replace the program listings; it supplements them and makes the information they contain more easily accessible. It is divided into seven sections, each describing certain aspects of the program:

"Section 1: Introduction," relates the I/O supervisor to users of its services and to the operating system, and describes overall I/O supervisor operation.

"Section 2: Method of Operation," contains diagrams that describe how the I/O supervisor functions, with emphasis on the data it uses, where it obtains the data, and how it acts upon that data to initiate and control I/O activity.

"Section 3: Program Organization," contains a functional organization chart and flowcharts of individual I/O supervisor routines.

"Section 4: Directories," contains information to be used for PLM–to–listing and listing–to–PLM transitions. Included are a module directory and a data area directory.

"Section 5: Data Areas," contains descriptions of the interrelationship and content of principal data areas used by the I/O supervisor.

"Section 6: Diagnostic Aids," contains information of a general nature which could be helpful in interpreting program listings.

"Section 7: Appendixes," is intended to supplement both this publication and the listings. Included are descriptions of SVC routines not covered in other sections, descriptions of some of the more involved optional features, descriptions of messages produced by I/O supervisor routines, a list of abbreviations, and a glossary.

Before using this publication, read the Introduction to establish perspective, and then at least scan the remainder to familiarize yourself with its content. This publication is primarily a reference manual because each section contains a specific type of information. You will be better able to service the program when you can refer quickly to the section containing the type of information you need.

You are assumed to have a knowledge of programming for OS and should at least have reviewed recently the section on I/O programming in the publications *IBM System/360 Principles of Operation,* GA22–6821, and *IBM System/370 Principles of Operation,* GA22–7000. Continual reference to the above publications is encouraged in order that readers fully understand the significance of some aspects of I/O supervisor logic.

This publication can serve Multiprogramming with a Fixed Number of Tasks (MFT) users and Multiprogramming with a Variable Number of Tasks (MVT) users. First read the introductory PLMs for your respective systems:

OS MFT Supervisor Logic, GY27-7236

OS MVT Supervisor Logic, GY28-6651

There are publications available that contain information about individual I/O devices. These are listed in the publication *IBM System/360 and System/370 Bibliography*, GA22-6822.

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SUMMARY OF CHANGES FOR RELEASE 21

Item	Description	Areas Affected
Model 135	CCH support	Section 2: Operation Diagrams Section 3: Flowcharts Section 5: Recovery Management Support Communications Area Section 7: Appendix C
3505/3525	New I/O error routines	Section 2: Device Dependent Error Recovery Routines
Write Inhibit Switch	New sense byte information	Section 2: 2301, 2302, 2302, 2305, 2311, 2314, 2327, and 3330 Error Routine
SYS1.LOGREC Revisions	Changes in error recovery	Section 2: Writing Error Recovery Messages to the Operator Section 5: SYS1LOGREC Data Set
Generalized Trace Facility	Addition of new routine	Section 3: Flowcharts Section 6: Generalized Trace Facility
OLTEP IOS	Additional support	Section 7: Appendix J
3420/3803	New devices	Section 2: 2400 Tape Series Error Routine Section 3: Flowcharts Section 5: Data Area Layouts Section 7: Appendix A
3410	New device	Same as 3420/3803
M65MP	Shared DASD	Section 2: Starting I/O Devices Section 3: Flowcharts Section 5: Data Area Layouts

SECTION 1: INTRODUCTION

Following execution of the statements or instructions written by programmers to cause I/O activity, a sequence of events begins in which the I/O supervisor plays a major role. This section defines that role and describes the environment in which it is performed.

Introduction

An input/output operation can be described as the sequence of events beginning with execution of the statement or instruction a programmer writes to cause data to be written on or read from an input/output device and ending when all related activity is completed. Although the input/output supervisor plays a major role in the performance of an input/output operation, it is not the only control program element that is involved. The purpose of this section is to establish the scope and objectives of the input/output supervisor.

First, the I/O supervisor as it relates to the user of its services is decribed. The user can be a programmer who writes using a higher–level language, or who writes using an assembler language with access method macro instructions. The user may also be a control program routine that is writing data into a system data set. All users of the I/O supervisor must provide it with certain information, and all users are provided with information about the success or failure of the I/O operation.

Second, the relationship between the I/O supervisor and the rest of the operating system is discussed. The supporting role the control program plays in the performance of an I/O operation is entirely different from its role when it is a user.

The third part of this section describes how the I/O supervisor achieves its objectives. To understand how the I/O supervisor functions, one must distinguish carefully between what is done to perform an I/O operation, and what is done to coordinate the performance of an I/O operation with other I/O operations. A Start I/O instruction, for example, would be issued to perform an I/O operation, while a queue representing requests that could not be satisfied because needed devices were busy would be maintained as a coordinative function.

In the fourth part of this section, the concept of logical channels is presented. It is a prerequisite for the descriptions, in later sections, of how the I/O supervisor queues requests for I/O operations.

The User and the I/O Supervisor

Three methods a programmer can use to request an I/O operation are shown in Figure 1. The actions taken by the I/O supervisor in satisfying the request are shown below the horizontal line that divides the figure. Specific input data must always be provided to the I/O supervisor, but the extent to which the programmer must define that input data depends upon the method he is using to request the I/O operation.

The user of a higher–level language (PL/I, for example) describes files and writes OPEN and GET statements. When his program is executed, one PL/I subroutine uses a DCB macro instruction to build a data control block (DCB), and an OPEN macro instruction to cause data management routines to build a channel program, an input/output block (IOB), a data extent block (DEB), and an event control block (ECB). Another PL/I subroutine uses a GET macro instruction, and a data management routine executes an EXCP macro instruction that causes entry to the I/O supervisor.

Adjacent to the steps taken by a programmer who uses a higher–level language are shown the steps a programmer must take when he is using an assembler language and chooses to use an access method. This is the path normally taken by control program routines. With an access method, a programmer must essentially do what the PL/I

compiler did; that is, he must himself write all needed DCB, OPEN, and GET macro instructions.

The user of an EXCP macro instruction must provide directly all of the input that is required by the I/O supervisor. He may use the DCB and OPEN macro instructions, and he may use the I/O appendages—user–written routines that receive control at appropriate exits in the I/O supervisor code—but he must write his own channel program, and he must build his own IOB and ECB. To request any kind of I/O activity, he must use the EXCP macro instruction. The EXCP user has the option, at OPEN time, to specify the use of I/O appendages during the progress of I/O operations associated with his data set. These appendages gain control at specific points in the EXCP supervisor and the I/O interrupt supervisor. They gain control:

- During extent checking, if an out–of–extent condition is detected
- Prior to issuing the SIO instruction
- If a PCI interrupt is received
- If a normal channel end interrupt is detected
- If any abnormal conditions are detected with a primary interrupt

The purpose of I/O appendages is to give the EXCP user a means of extending and altering I/O operations. For further information about I/O appendages, see *OS Data Management For System Programmers,* GC28–6550.

Note from Figure 1 how a higher–level language compiler makes use of access method routines, and note also the similarity between what is done by access method routines and what a programmer must do when he chooses to use the EXCP macro instruction.

The I/O Supervisor and the Control Program

There are a number of control program elements involved in I/O operations besides the I/O supervisor. For the most part, however, the functions they perform are supporting functions needed to coordinate the actions of the I/O supervisor with other system actions. The general system environment of the I/O supervisor is shown in Figure 2.

When an EXCP macro instruction is encountered during assembly of a processing program, the assembler obtains the corresponding macro expansion from the SYS1.MACLIB data set and inserts it into the object program. The last instruction in the EXCP macro expansion is an SVC 0 instruction.

During execution of the processing program, the SVC 0 instruction causes an SVC interruption and immediate entry to the supervisor's SVC first level interruption handler (SVC FLIH). The SVC FLIH is always given control after SVC interruptions. It refers to a list of SVC numbers (called an SVC table) to determine 1) what SVC routine is to service the request and 2) whether or not the needed SVC routine is of the type that is contained in main storage. In the case of SVC 0, the routine to be given control is always the I/O supervisor's EXCP routine, which is a type 1 SVC routine and is contained in the nucleus.

In giving control to the EXCP routine, the SVC FLIH passes the address of the input/output block (IOB), the key item of input data, to the I/O supervisor.

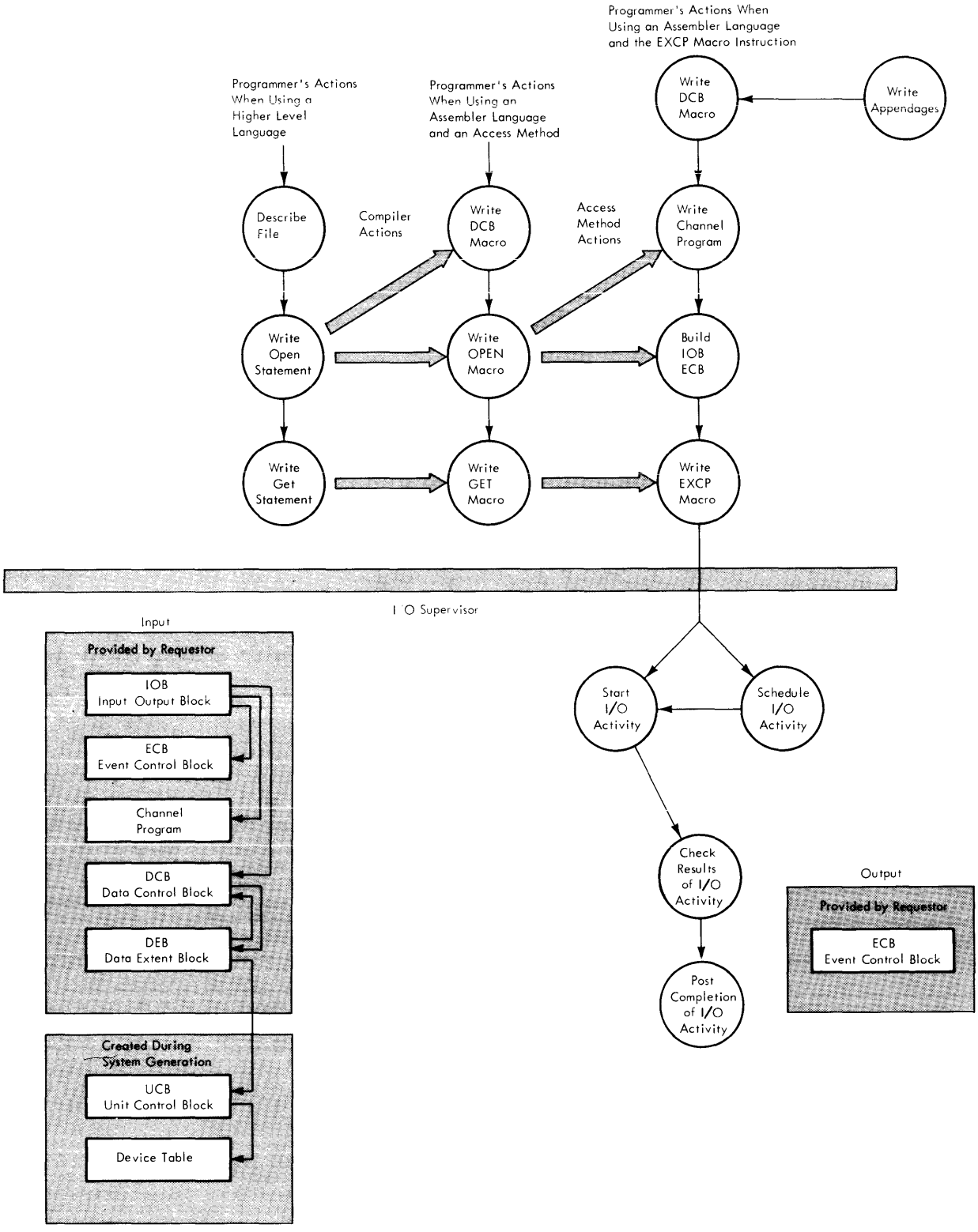

Figure 1. The User and the I/O Supervisor

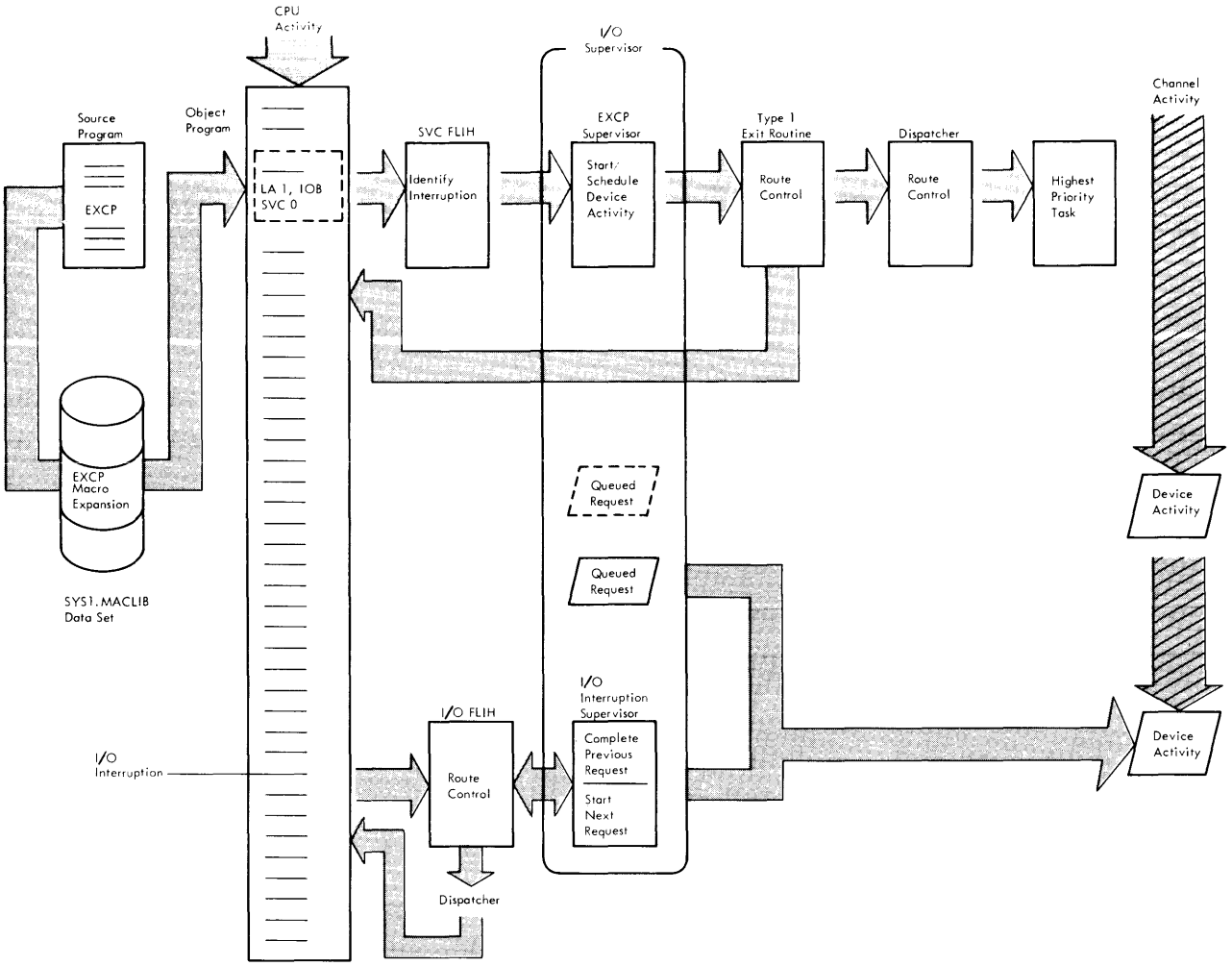

Figure 2. The I/O Supervisor and the Control Program

Using input data it obtains at addresses contained in the IOB, the EXCP supervisor either starts the I/O device or, if the needed device is unavailable, schedules the request for activity on the device by placing an element representing the request into a queue.

The EXCP supervisor then gives control to the supervisor's type 1 Exit routine. All type 1 SVC routines (except those abnormally terminated) pass control to the type 1 Exit routine.

If the routine in which the request for the I/O operation was made is still the highest–priority task in the system, the type 1 Exit routine restores the environment that existed at the time of the interruption and returns control to the requesting routine. Alternatively, it passes control to the supervisor's dispatcher routine, which routes control to a routine of a new highest–priority task.

The next event occurs asynchronously. When the device has completed its part of the I/O operation, it causes an I/O interruption. Following I/O interruptions, CPU control is given to the supervisor's I/O first-level interruption handler (I/O FLIH). The I/O FLIH saves a record of the interrupted environment and gives control to the second of the two major I/O supervisor routines, the I/O interruption supervisor.

While the I/O interruption handler processes one interruption, one or more I/O operations may occur. Such interruptions are "stacked"—saved by the hardware, thus creating a "pending interrupt." The I/O interruption handler processes stacked interruptions by enabling twice: before channel restart is attempted and prior to exiting to the I/O FLIH.

The I/O interruption supervisor signals the requestor that the I/O operation is completed (the task supervisor's POST routine posts the requestor's event control block), and starts other devices on the channel in response to any requests that were queued while the device, data set, or channel was busy with the just-completed request.

The I/O interruption supervisor then returns control to the I/O FLIH and, via the dispatcher, control is routed either to the requesting routine or to a routine of a higher-priority task.

The I/O Supervisor

The overall objective of the I/O supervisor is to make sure that a requested I/O operation is performed. To achieve its objective, the I/O supervisor performs three major functions: starting I/O operations, terminating I/O operations, and restarting I/O operations (for error-correction purposes). These functions, the two major I/O supervisor routines and the general control flow to and from the routines, are shown in Figure 3.

The EXCP supervisor is shown twice intentionally. Even though the same routines start and restart I/O operations, the two functions are separate and distinct functions and are treated separately in the remainder of this publication.

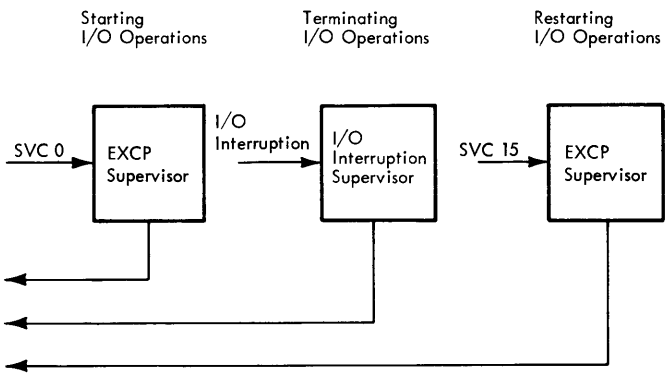

Figure 3. I/O Supervision

The basic control flow to and from the EXCP supervisor and the I/O interruption supervisor has already been shown in Figure 2. One exception to the material already presented is that, for restarting I/O operations, an SVC 15 instruction (rather than an SVC 0 instruction) causes entry to the EXCP supervisor.

The same type of diagram is used in Figure 4, where the major functions are expressed in more detail, and the three coordinative functions have been added: scheduling I/O operations, starting scheduled I/O operations, and scheduling restarts of I/O operations.

The first flow diagram in Figure 4 shows the flow for a straightforward I/O operation, where the Start I/O instruction is accepted and there is no need to schedule I/O device activity. This flow is shown separately to illustrate how the request queue is checked following completion of every I/O operation. The queue is checked repeatedly until no pending requests remain. After terminating an I/O operation, the I/O interruption supervisor invokes a user–written or IBM–supplied error correction routine if the status indicators show an error conditon to exist. Error routines can request a retry by issuing an SVC 15 instruction, which will result in entry to the EXCP supervisor for the retry.

The second flow diagram in Figure 4 shows the flow for an I/O operation that could not be started immediately. Note that the request queue is examined after a restart of the I/O operation is scheduled, just as it is when an I/O operation is terminated.

Concept of Logical Channels

The queues into which request elements are placed when I/O activity cannot be started immediately do not always correspond one–for–one with the physical channels attached to a system. Rather, they correspond to what are called logical channels. A logical channel is the set of all physical channels by which a device can be reached.

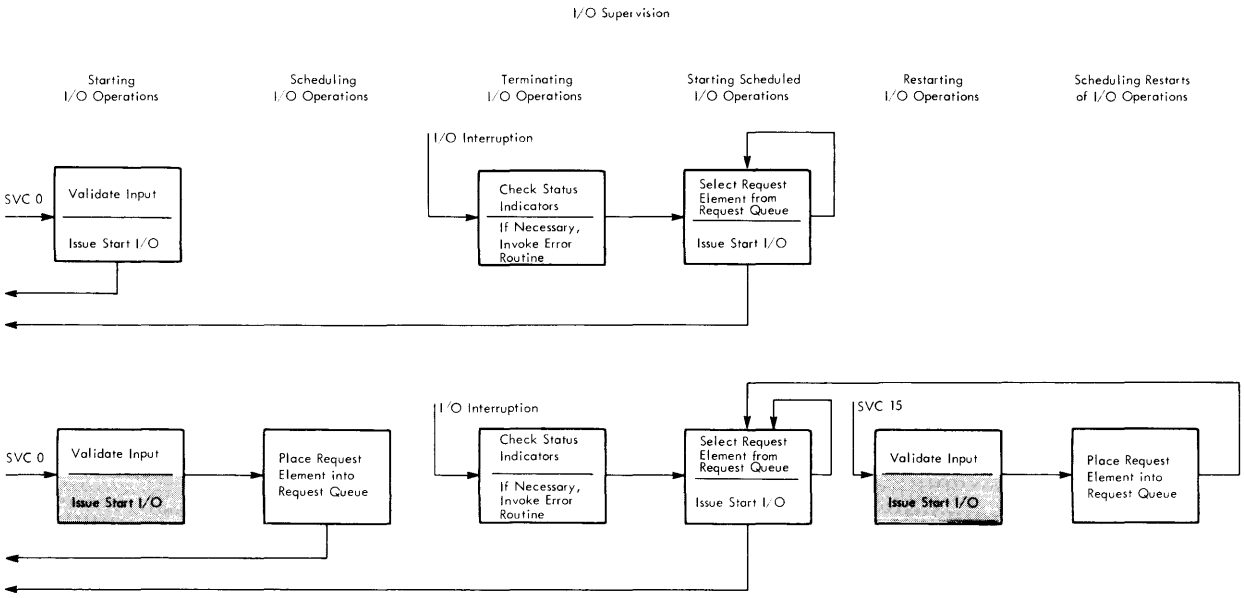

Figure 4. I/O Supervisor Functions

Queuing in logical channel queues makes possible path–device groups in which a common set of paths can be tried for each device of a group. The result is simplified alternate–path logic.

Unless a switching device is installed, providing multiple–path capability, every physical channel is also a logical channel and there is a one–for–one correspondence. With

switching devices, however, the relationship between physical and logical channels varies, depending upon both the number of switches and their placement.

A system with no two–channel switches is shown symbolically at the top of Figure 5. Because each device can only be reached via one path, each physical channel is also a logical channel.

Also shown in Figure 5 is a system in which a switching device connects two control units. Devices B and C can then be reached via channel 1 or channel 2. The devices B and C are both in the logical channel comprising physical channels 1 and 2.

Another configuration with a switching device is shown at the bottom of Figure 5. This time, devices B, C, and D may be reached via channels 1, 2, and 3; devices B, C, and D are all in the same logical channel.

Except for the 2870 Multiplexor Channel, all devices attached via the same multiplexor channel will always be in the same logical channel. The devices attached via a 2870 Multiplexor Channel may be contained in more than one logical channel, however, because each of the four optional selector subchannels is considered separately.

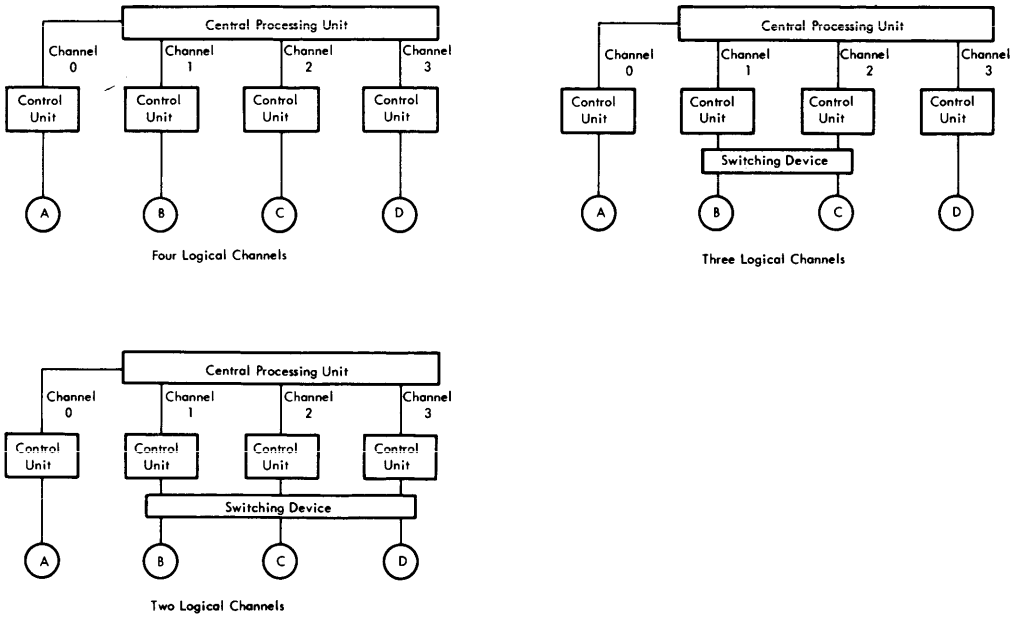

Figure 5. Logical Channel—Physical Channel Relationships

SECTION 2: METHOD OF OPERATION

This section describes the I/O supervisor in terms of the operations it performs. Operation diagrams (Diagrams 1 through 16 at the end of this section) show the movement of data through the tables, blocks, work areas, and data sets used by the program, and describe the processing performed at each stage. The operation diagrams are designed to be used in conjunction with supporting text.

Operation diagrams are not flowcharts. (Flowcharts are provided in Section 3.) An operation diagram shows where information comes from, how it is processed, and where the results are stored. The diagrams include symbolic names that identify the areas of code involved with the operation.

If you are already familiar with the program, the operation diagrams will act as a recall mechanism. If you are learning the program, the diagrams and their supporting text will help you to quickly understand the I/O supervisor or the part of the I/O supervisor that you are interested in.

Overall Operation

Because the I/O supervisor has access to and can change vital system data, it checks all input it receives. Then it builds a control block called a request queue element (RQE) to represent the request for I/O activity. When processing of a request must be delayed because a device or channel is busy or unavailable, the I/O supervisor places the RQE into a queue. When a device is free and a path to the device is open, the activity is started. An I/O interruption signals the end of the activity. If it was not completed successfully, the I/O supervisor invokes an error routine, which may attempt the activity again.

Validating Input Data

Before any action is taken on a request for I/O activity, the input data is checked. Figure 6 shows what checks are made upon each of the data areas passed to the I/O supervisor when I/O activity is requested.

Scheduling I/O Operations

To schedule an I/O operation, the I/O supervisor initializes a request queue element and links it to the logical channel queue for the channel on which the operation is to be performed.

Initializing a Request Element

The first major step taken by the I/O supervisor in satisfying a request for I/O device activity is to initialize a control block to represent the request. The control block is called a request queue element (RQE), and it is initialized to contain pointers to information that is used in processing the request. Once an RQE has been initialized, it can, by means of a link field, be placed in or removed from any of several request queues that are used in coordinating and monitoring the progress of I/O activity.

A request queue is shown in Diagram 1 as it exists before any requests for I/O device activity have been received. Note that the size of the queue is established during system generation.

The NEXAVL (next available) pointer and the TSTLNK fields of individual request elements are initialized during assembly of the I/O supervisor control section. The NEXAVL pointer contains the address of the first free request element. The TSTLNK fields of all but the last element contain the address of the next element; the last element contains distinguishing 1s in its TSTLNK field.

The NEXAVL pointer always begins a queue called the freelist. NEXAVL is continually updated so as to point to the first available request element, and all free request elements are chained via their TSTLNK fields. Before any requests for I/O activity are received, all request elements are contained in the freelist.

The method by which elements are obtained and removed from the freelist is straightforward: the NEXAVL pointer is used to locate the first freelist request element, and the element is removed when the TSTLNK field of the selected element is placed into NEXAVL.

Intercept Processing

The addressed device is then checked for an intercept condition. An intercept condition is an abnormal condition such as device end and unit check—caused by a previous request for the same device. The determination of an intercept condition

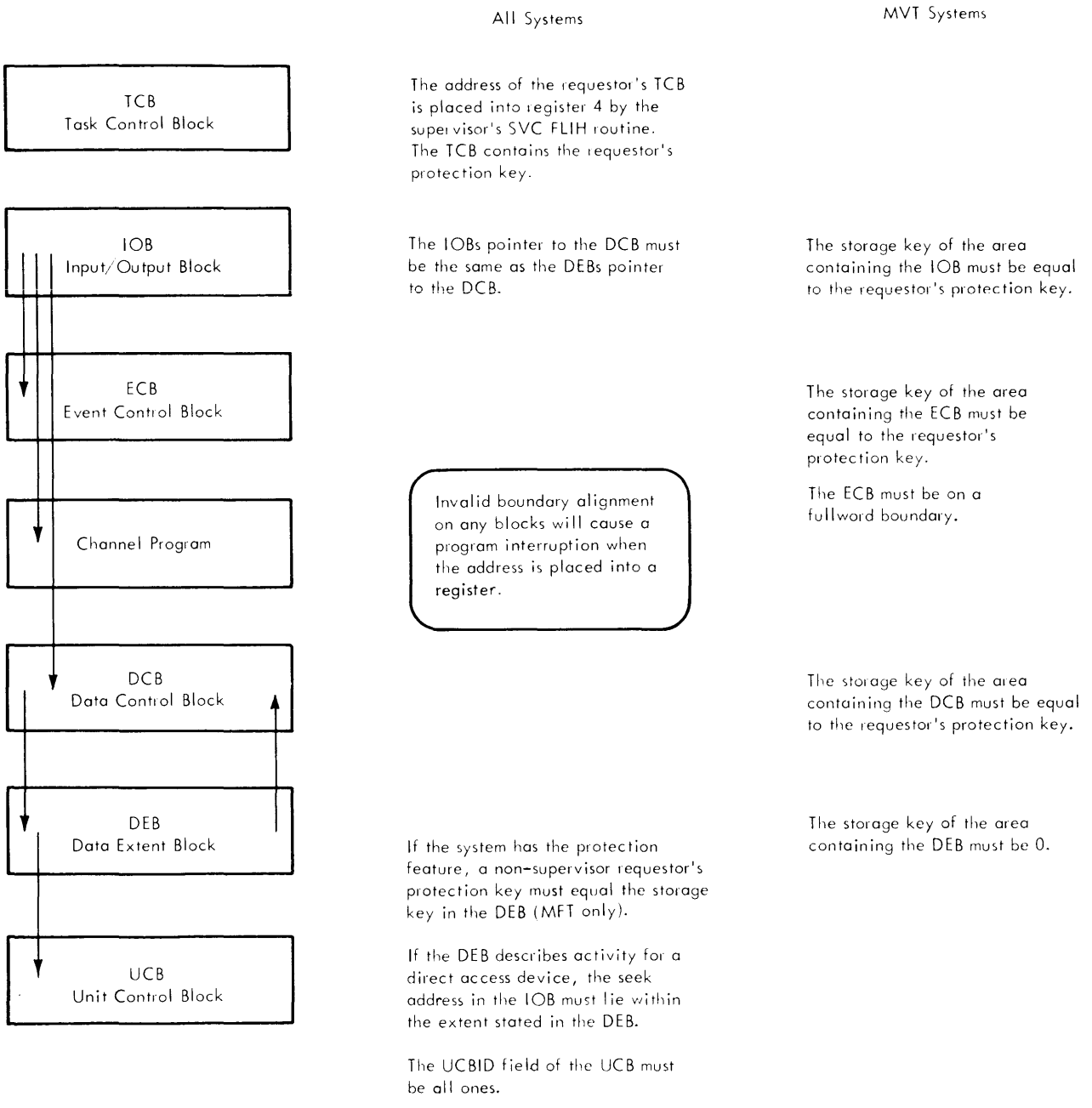

Figure 6. Validating Input Data

depends on the setting of the UCB intercept flag. If the flag is on, the intercept processing code (INTERR5) begins. It consists of:

- Moving the saved CSW status bytes and the sense bytes from the UCB to the input/output block (IOB) associated with the current request. (The status and sense bytes are thus available for use by the error recovery routine that may be scheduled.)
- Setting the intercept code (hex. '7E') in the ECB code field of the IOB. The code (changed to hex. '44') will be posted in the event control block for the current request, if the intercept condition proves to be uncorrectable.
- Branching to the dequeue module (XCPPDQ) to remove the request element from the request queues. Control is then given sequentially to the user abnormal end appendage and the error routine interface (INTERR). If the user has selected the use of IBM error recovery procedures, the request element is used to schedule an error recovery routine. Otherwise, the request is posted complete with permanent error.

If the flag is off, an intercept condition does not exist, and the appropriate common test channel routine (chart AB) is entered.

See the sections "Testing Channel Availability" and "Starting I/O Devices" for further information.

Queuing a Request Element

Not all requests for input/output activity can be satisified immediately. When a needed device is unavailable because it is being used or because its channel is busy, the request element representing the request for the device is placed into a queue.

To determine whether or not a device is available, the Get Request Element routine checks the UCBFL1 field of the unit control block for the device, where a record of the device's status is maintained (Figure 7).

There is a queue for every logical channel. Furthermore, there can be up to three ways by which a request element can be added to one of the queues, depending upon the queuing option selected for the device during system generation:

- FIFO queuing—it can be added to the end of a queue. RQEs are added at the end of the queue in the order in which they occur.
- Priority queuing—it can be added to a place in a queue determine by the requestor's priority. RQEs are added according to the priority of the requested task.
- Ordered Seek queuing—it can be added to a place in a queue determined by the seek address. Depending on the access method, RQEs are added according to the cylinder address on direct access devices.

Therefore, the process of queuing a request element includes first selecting one of up to three queuing routines and then providing the selected routine with a pointer to the queue on which it should place the request element. The mechanism by which the selection of a queuing routine and queue combination is achieved is illustrated graphically in Figure 8, while a more detailed view of the entire process is shown in Diagram 2. Note from Figure 8 how two fields of the unit control block—UCBDTI and UCBLCI—are used in selecting the needed combination of queuing routine and queue.

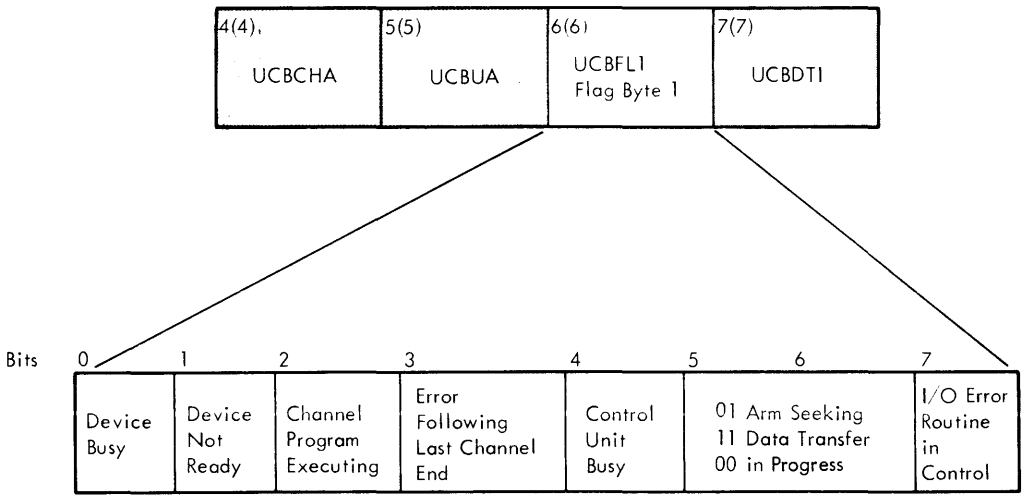

Figure 7. UCB Flags Examined to Determine Device Availability

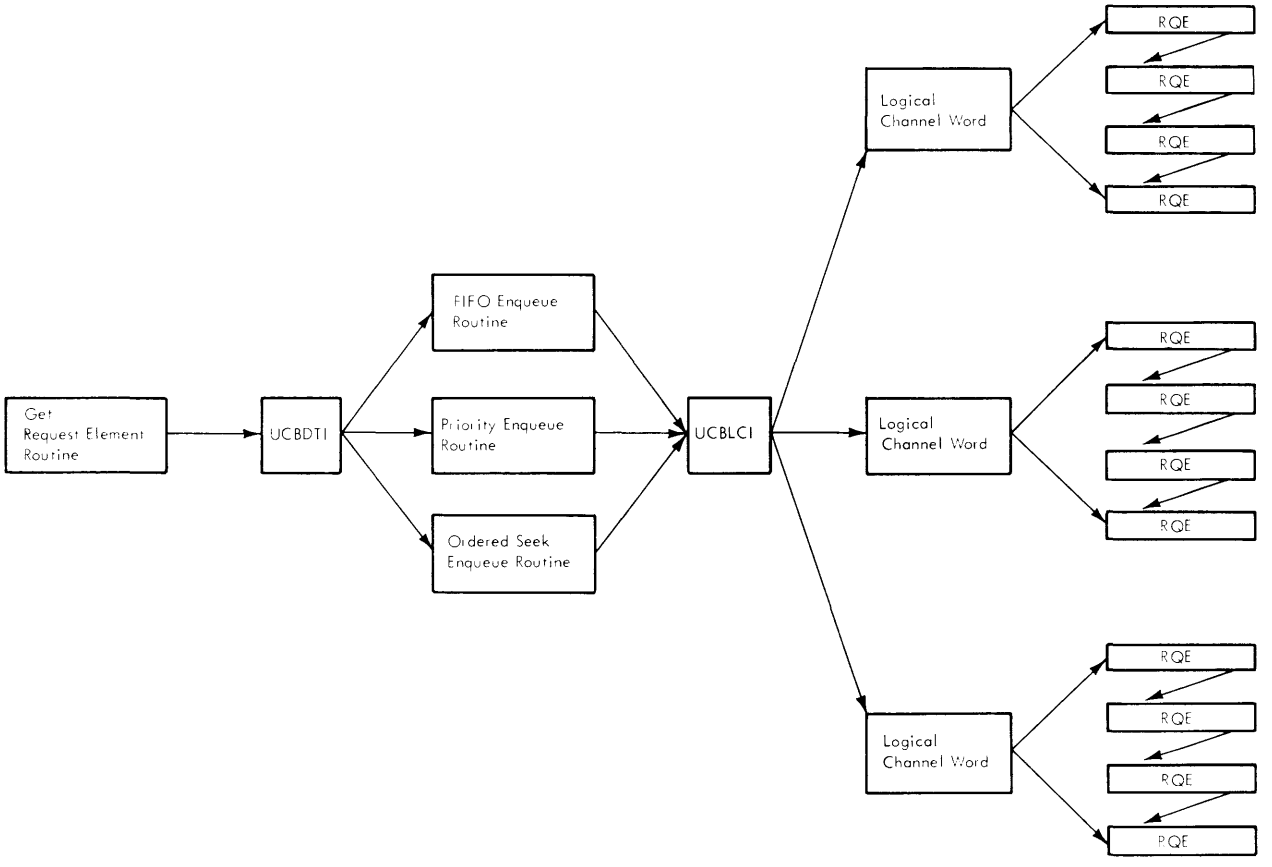

Figure 8. Queuing Routine—Queue Relationships

Starting I/O Operations

Starting an I/O operation involves: making sure that a path to the device is free; preparing a channel program to be executed prior to the requestor's channel program; executing the Start I/O instruction; and checking the condition code resulting from the Start I/O instruction.

Testing Channel Availability

When a device is found to be available, the next step taken is to make sure that a channel by which the device can be reached is available. Byte multiplexor channels are not tested, because the Test Channel instruction cannot be used for testing individual subchannels. (When any one of the subchannels is free, the response to the Test Channel instruction is channel available.) Selector and block multiplexor channels are checked. The checking consists of obtaining the channel's address and using it in a Test Channel (TCH) instruction, and then checking the resulting condition code (Diagram 3).

For each logical channel in the system, there is a unique Test Channel routine entry point, and the address of that entry point is contained in the channel's logical channel word. When only one path to a device exists, there is a direct relationship between the entry point and the channel address. Therefore, at each entry point a predetermined constant value can be used for the channel address. The value is placed into a register to be used with the Test Channel instruction.

When alternate paths to a device exist, there are instructions at the Test Channel routine entry point which select a channel address from addresses contained in an alternate path table. If the first channel selected is found to be busy when the TCH instruction is executed, another address is selected. The select–test sequence is repeated until an available channel is found, or until all possible paths to the device are exhausted. If a channel that is available is found, preparations for starting I/O device activity are continued. If there are no free paths to the device, the request is queued.

One of four condition codes will be set following execution of a TCH instruction. If the Interruption Pending in Channel (cc 1) or the Channel Operating in Burst Mode (cc 2) condition codes are on, the request element is queued. No distinction is made between the Channel Available (cc 0) and the Channel Not Operational (cc 3) condition codes. If the channel is not operational, information of a more detailed and helpful nature can be obtained by issuing the Start I/O instruction.

Starting I/O Devices

When both a device and the channel by which the device can be reached are available, the activity requested for the device is begun. There are two major factors that influenced the design of the I/O supervisor in this area: differences in the characteristics of individual devices; and a need to distinguish between a normal start and a restart (as when an error routine is retrying an I/O operation to attempt a recovery). The logic involved in allowing for the characteristics of individual devices is described here. The operation diagrams and flowcharts do include some restart–related information, but this is done to preserve overall continuity of Figures in this publication. Restarts are discussed under "Restarting I/O Devices."

Allowances need not be made for every type and model of I/O device that can be attached to a system. Certain groups, or classes, of devices have common characteristics and all devices in a group can be treated alike. There are three device classes:

- Unit–record and communications devices
- Magnetic–tape devices
- Direct–access devices

There is one device–related Start I/O routine for each device class (Charts AD thru AI). Each of these makes use of a Start I/O subroutine (Chart AK), which executes the Start I/O instruction and, to a limited extent, checks the resulting condition code.

Unit–Record, Communications, and Graphics Devices

The logic involved in starting activity on unit record, communications, and graphics devices is not complex (Diagram 4 and Chart AD). For immediate operations, which involve no transfer of data, a single channel command word (CCW) contained at the location named SYSIMD is used. The command code is the only variable, and it is obtained from offset 24 of the input/output block (IOB). The address of the single, or "stand–alone," CCW is placed into the channel address word (CAW). Therefore, when the Start I/O instruction is executed, the channel will fetch and execute the stand–alone CCW.

For operations involving a transfer of data, the address of the requestor's first CCW is placed into the CAW, and the requestor's channel program is fetched and executed by the channel after the Start I/O instruction is executed by the CPU.

Magnetic–Tape Devices

Except for operations following those in which a cyclic redundancy check was detected, the IOS channel program for magnetic tape devices consists of two CCWs: the first contains a Set Mode command code (Set Density, Set Parity, etc.), and the second contains a Transfer–in–Channel command having as its data address the address of the requestor's first CCW (Diagram 5).

Three CCWs are used for magnetic tape operations following those in which a cyclic redundancy check was detected (Diagram 6). The first and third of these contain the Set Mode and Transfer–in–Channel commands, respectively. The second CCW contains a Track–in–Error command code.

Direct–Access Devices

If a direct access device has a movable access mechanism, it must be positioned to the required seek address before data transfer can begin. During the time interval needed to position the access mechanism, the channel is free to perform I/O operations for the other control units attached to it. For this reason, (except for 3330) two seeks are issued to service an I/O request to such a direct access device. The first seek is a "stand alone seek"—it is not chained to the other CCWs. As soon as the control unit receives the seek address, it signals channel end, and the I/O interruption handler can start other I/O operations on the channel. The second seek is needed because the other I/O operations for the channel may include seek requests for other devices connected to the control unit. The second seek reinstates in the control unit the address at which data transfer is to begin (the access mechanism of the device will still be positioned at the correct address, which was given in the first seek).

Except for 3330, the Start I/O instruction is therefore executed twice for direct access devices with movable access mechanisms. The first time, the CAW points to the CCW for the stand–alone seek. The second time the Start I/O instruction is executed (Diagram 7), the CAW points to the first CCW of a three–CCW IOS channel program consisting of: the second Seek command; a Set File Mask command for indicating to the channel which commands are valid for the current operation; and a Transfer–in–Channel command containing the address of the requestor's first CCW.

If a condition code of 0 is returned from the first execution of the start I/O instruction, the routine effects a loop with a test I/O (TIO) instruction until the CSW is stored. The stored CSW indicates that channel end has occurred and that the seek address has been transferred to the head register of the control unit. Then the routine tests for any abnormal conditions received as a result of the TIO instruction.

The routine tests to see if the access arm has reached its destination (device end). If the seek was not completed, the routine either branches to the enqueue routine if I/O was entered via the EXCP subroutine, or gets the next request via the channel search routine if I/O was entered via the channel restart procedure. If the seek was completed, the UCB busy and post flags are turned off indicating that the device has reached its destination and that the data transfer operation can be started.

If the direct access device does not have a movable access mechanism, a stand–alone seek is not performed. One Start I/O instruction is executed, and the CAW is made to point to the first CCW of the three–CCW channel program shown in Diagram 7.

Notes: In a Model 65 multiprocessing system that supports shared DASD, the I/O supervisor insures that Start I/O instructions for a shared device that is reserved are issued via the reserved path and by the CPU that reserved the device.

If the device is a Rotational Position Sensing (RPS) device, IOS does not issue a "stand alone seek." After the seek argument is transferred to the control unit, the block multiplex channel disconnects from this request and is free to handle other I/O requests. When the seek argument has been completed and the block multiplex channel is free, the channel reconnects to the original request. In its work area, each 3330 device has its own Seek command, Set File Mask command, and a Transfer–in–Channel command containing the address of the requestor's first CCW.

2305 SIO Subroutine: The 2305 SIO subroutine is provided to perform those functions of the SIO process which are unique to 2305. Refer to the flowcharts for a detailed description.

Upon entry to the 2305 SIO subroutine, the RQE will contain the base address UCB, except for those requests which are in an error recovery process. The UCB chain pointers are used to search for a free exposure on which this request can be started. For non–sequential requests (unrelated), the first available exposure encountered can be used. Handling of sequential requests requires that all exposures be checked for an available request which is related to this one. If no available related exposure is found, the request is started on any available exposure. If no active exposure exists, the request is queued.

Before starting a request on an exposure, the seek address is extent checked, then the exposure UCB address is stored into the RQE and the base UCB workarea. Also the CAW and system channel program (Seek, Set File Mask, and TIC) are initialized for this request.

The process for starting direct access devices differs in a system that has the Shared DASD option. Because a single direct access device is shared between two CPUs with this option, special commands are used by the I/O supervisor and the user. Reserve and Release are commands used by the I/O supervisor; RESERVE and DEQ are macro instructions used by the user. The Reserve command is chained to the I/O supervisor channel program when a check of the Reserve Count Field in the UCB shows it to be one or greater or when any stand–alone seek is issued. The RESERVE macro instruction is issued by the user when he needs exclusive use of a shared direct access device. Issuance of the RESERVE macro instruction causes the count in the Reserve Count Field of the UCB to be increased by one. The I/O supervisor then issues the Reserve command to prevent the second CPU from accessing the shared direct access device. The DEQ macro instruction is used by the user to indicate the end of his need for exclusive use of the shared direct access device. The DEQ macro instruction reduces the count in the Reserve Count Field of the UCB by one. The Release command is used by the I/O supervisor when the Reserve Count Field in the UCB is zero to free an exclusively used device.

Checking Condition Codes

The result of a start I/O instruction is indicated by the condition code that is placed into the current program status word (PSW) by the CPU. One of four condition codes could appear in a PSW after a Start I/O instruction is executed:

0 The I/O activity was begun.

1 The channel status word (CSW) was stored.

2 The channel or subchannel is busy.

3 The channel or control unit is not operational.

For condition code 0 (the I/O activity was begun) the request queue element for the started request is removed from a logical channel queue if it is in one. The request queue element would be in a queue if the request was scheduled after a previous unsuccessful attempt to start the activity. Once a request has been started, an interruption signals to the I/O supervisor that the activity has been completed. At that time, the I/O interruption supervisor will be entered (see 'Terminating I/O Operations').

For condition code 1 (the CSW was stored) the status bits of the CSW are examined. Diagram 8 shows which status bits are checked, what events they signify, and what actions are taken.

When the condition code is 2 (the channel or subchannel is busy) the requested I/O activity cannot be started because another I/O operation is in progress. The control unit busy flag in the UCB is turned on and control is given to the Test Channel routine so that another path may be tried.

A condition code of 3 (not operational) means that due to an equipment failure the device or the channel cannot be used. The actions taken when the condition code is 3 depend upon whether:

- The system has the Alternate Path Retry selective retry option.
- There are alternate paths to the device.

- An IBM error routine is to be used.
- This is the first occurrence of this condition code 3 on this path.

Terminating I/O Operations

When the interruption that signals completion of I/O activity occurs, an indication of why the activity stopped appears in the channel status word (CSW). The CSW status indicators are checked, and if the activity was completed successfully the requestor's RQE is freed. If not, the actions taken depend upon an analysis of the error condition.

Every time one I/O operation is completed an attempt is made to start other I/O operations, including those scheduled to be performed on the same logical channel, and also those scheduled for any other logical channels containing the physical channel on which the operation was completed.

I/O interruptions, prevented from occurring during execution of most of the I/O supervisor, are allowed to occur before the attempt to start scheduled I/O operations and once again after channel restart has been completed.

Checking Status Indicators

Except for immediate operations, once activity is started on an I/O device it continues until:

- An error condition causes premature termination.
- The activity is completed.

For both cases, the means by which termination of the I/O activity is made known to the I/O supervisor is the I/O interruption, and the means by which the I/O supervisor can determine what caused termination are status indicators, contained in the channel status word (CSW).

Unlike the case of the Start I/O instruction, where the status information is stored only when an exceptional condition occurs, status information is always stored in the CSW when an I/O interruption occurs (Part 1 of Diagram 9). Also, the contents of the current PSW are stored at the I/O old PSW location. In effect, the CSW shows what happened; the PSW shows where it happened. Chart BB shows the CSW bits tested.

When a channel end status is received and no errors have occurred during the activity, the contents of the CSW are moved into the requestor's input/output block (IOB), and the requestor's channel end appendage is given control if one is provided. Then the requestor's event control block (ECB) is posted complete and his request queue element (RQE) is returned to the freelist (Part 2 of Diagram 9).

If a check of the status shows 0 status or Control Unit End, it is considered a Channel Available End and handled as a signal to start a new I/O operation on the associated channel.

Should an analysis of the CSW status bits reveal a unit check, the sense routine (INTSEN) is entered (Charts BG and BH). The sense routine constructs and issues a sense command to the device in error. It then copies the first two sense bytes into the IOB; these are subsequently examined and handled by the appropriate error recovery routine. If the shared DASD option is in the system, a read home address and a read record 0 commands are chained to the sense command, except for the 2305 and 3330.

Furthermore if the Reserve count field is zero, the sense command is changed to a RELEASE command—a special type of sense command. This frees the device for use by the other CPU. The home address and record 0 data is read into the UCB work area.

If an error occurs after the channel end status is received, it will be too late to act upon the completed request, but the next request for activity on the same I/O device will be intercepted, and the error condition will be checked at that time (Chart AB, Get Request Element Routine). The I/O interruption supervisor locates the UCB address of a device in error in one of two ways: by using the last UCB for the channel on which the error occurred, or by using the value in the UCB lookup table in an algorithm. (See Figure 43 for the algorithm.)

The actions taken for each type of error depend upon: the nature of the error; the context of the error (other conditions detected at the same time); and, in some cases, the optional features contained in a system.

Starting Scheduled I/O Operations

When a needed device is unavailable at the time a request for I/O activity is received, the activity is scheduled. That is, the request element for the request is placed into a logical channel queue. While one I/O operation is being performed, a number of requests might be received that require scheduling. An attempt is made to retry all such outstanding requests for I/O activity on a channel when an I/O interruption occurs and the needed channel becomes available.

The actions taken to start one or more I/O requests depend upon the type of channel made available (multiplexor or selector) and the number of logical channels in which a just–freed selector channel is included. The objective is the same, however, regardless of what type of arrangement exists—to start processing as many requests as possible. To do this, a channel search module provides the Channel Restart routine with the address of the logical channel. To provide for overlapped seek and data transfer operations (on separate devices), the logical channel is searched twice; once for all requests which require seeks, and once for a data transfer operation. When an RQE for a device with a movable access–arm is found in the queue, the status of the device is tested. If the device is not available, the module searches for the next RQE for a device with a movable access–arm. If the device is available, a test channel module is entered to determine if the channel is available.

Each channel has a unique channel search routine, tailored to its channel type and channel path arrangement, even though the bulk of the instructions in that channel search routine are common to all arrangements and are shared. This is set up during system generation, when for each channel there is included one of four unique sets of branch instructions to direct CPU control to entry points in the common routine. These channel search routines supply addresses of logical channel queues for a particular physical channel. With this, the Channel Restart routine obtains the proper channel search routine by multiplying the address of the available physical channel by four and adding that product to the address of the channel table. The channel search routines are shown in charts BM to BP, where no distinction is made between the branch instruction group and the common group of channel search instructions. The data flow for starting scheduled I/O operations is shown in Diagram 10.

Restarting I/O Operations

When channel status word indicators show that an error occurred during I/O activity, an I/O error routine is invoked and a cycle of restarts begins which continues either until the error is corrected or until it is declared to be permanent (uncorrectable). This cycle is illustrated in Figure 9. The controlling routine of the cycle is the I/O error routine, which upon exit may indicate that:

- The activity is to be retried.
- The error is permanent.
- The error has been corrected.

If the I/O error routine indicates that the I/O activity is to be retried, the I/O supervisor returns the request queue element (RQE) to the request queue. The restart takes place when the Channel Restart routine, during its normal processing, reaches the RQE and passes its address to the EXCP routine. After the I/O activity is completed, a series of switches causes control to return to the I/O error routine, even if no errors occurred during the retry.

I/O error routines count the number of retries and indicate to the I/O supervisor that the error is permanent when the maximum allowable number has been reached. When an I/O error routine indicates that an error condition is permanent, the I/O supervisor places a 'permanent error' return code into the requestor's event control block and places the RQE into the freelist.

An error is considered by an I/O error routine to be corrected when no errors occurred during a retry of the I/O activity. For corrected errors, the I/O supervisor places a 'completed without error' code into the requestor's ECB, and continues processing as it would have had there been no error the first time the activity was attempted.

When a data set has been found to be involved in permanent error, none of the related requests for that data set should be started. Therefore, before a restart is attempted, the RQEs for the related requests are removed from logical channel queues. The removal is performed by the I/O Purge routine (IGE0025E), which is invoked after an error routine has determined that an uncorrectable I/O error has occurred. The I/O Purge routine removes the request elements for the related requests from the logical channel queues, links the input/output blocks for purged requests in a chain, and posts the ECB for each purged request with a 'request element has been freed' code.

IBM Error Routines

IBM supplies four types of optional error routines for their customers: device–dependent routines, common routines, outboard–error recording routines, and miscellaneous data recording routines. The device–dependent routines are entered after either a unit check, a unit exception, a wrong–length indication, a protection check, a channel control check, an interface control check, a program check, a chaining check, or a channel data check condition as indicated in the CSW status byte. The IBM device–dependent error routines attempt error recovery. The common routines, comprised of the error interpreter, the write–to–operator routine, and the statistics update routine, are used by the device–dependent routines.

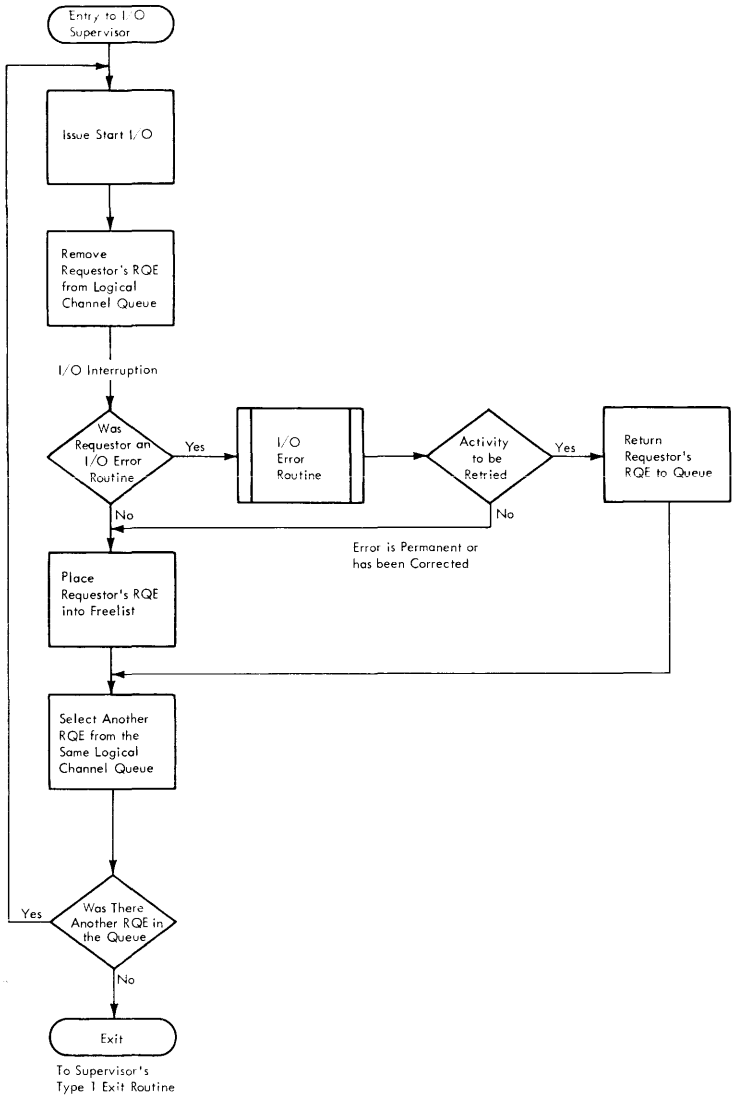

Figure 9. The I/O Restart Cycle

Invoking Error Routines

The order in which status indicators are checked, and the network of switches that controls entry to and exit from I/O error routines are shown in Figure 10. Diagram 11 shows how an I/O error routine is invoked.

Device–Dependent Error Recovery Routines

This section gives a general operating procedure for device–dependent error routines and explains the actions of each device–dependent routine.

General Operating Procedures

Device–dependent error routines gain control from either the contents supervisor in MFT systems or the stage–3 exit effector in MVT systems. (For a description of three stages of the MVT supervisor, see *OS MVT Supervisor Logic,* GY28–6659.) Even though each routine has specific characteristics tailored for each device type, the basic programming techniques are similar. Each routine sets the IOB error indicator bits, examines the sense and CSW status bits that are stored in the IOB to determine the type of error, and attempts to recover from the error, if at all possible, by retrying the channel program by means of an SVC 15 instruction.

The IOB exception flag (IOBEX) and error flag (IOBERR) are turned on by all the device–dependent error routines. These settings serve a three–fold purpose: both flags on indicate that an error routine is in process; IOBEX on and IOBERR off indicate a permanent error; and both flags off indicate a successful retry. The tables included for each error routine explain the sense bit settings and describe when retry is or is not attempted.

The sense and CSW bits that are stored in the IOB are checked by the device–dependent error routines. By checking the IOBFL1 field of the IOB, chaining types are determined. If the IOBFL1 field indicates data and command chaining, no error retry is attempted; if it indicates command chaining, error retry is attempted from the address of the CCW which caused the error; and if it indicates data chaining or no chaining, the error is retried from the first CCW. By checking the CSW status bits in the IOB, the error routine determines the type of error that occurred. The bits tested, the priority of the testing, and the labels in the error routine to which control goes are shown in the tables listed for each device–dependent routine.

The device–dependent error routines attempt retry of the channel program by issuing an SVC 15 instruction. If the retry succeeds, the IOB exception bit and errors flags are reset to zero, and normal processing continues. The number of retries attempted depends on the device.

If the CSW status contains a unit check, the device–dependent routine (except for the 2305 and 3330) gives control to the statistics update routine to update the statistics table.

Individual Routines

This section contains information about individual error recovery routines. The descriptions are arranged in numerical order according to machine–type. All follow the same organization scheme: a brief description of any characteristics of the routine or device that could be of use in interpreting the listings; a table, the Error Analysis Sequence Table, showing the order of examination of sense and status bits with

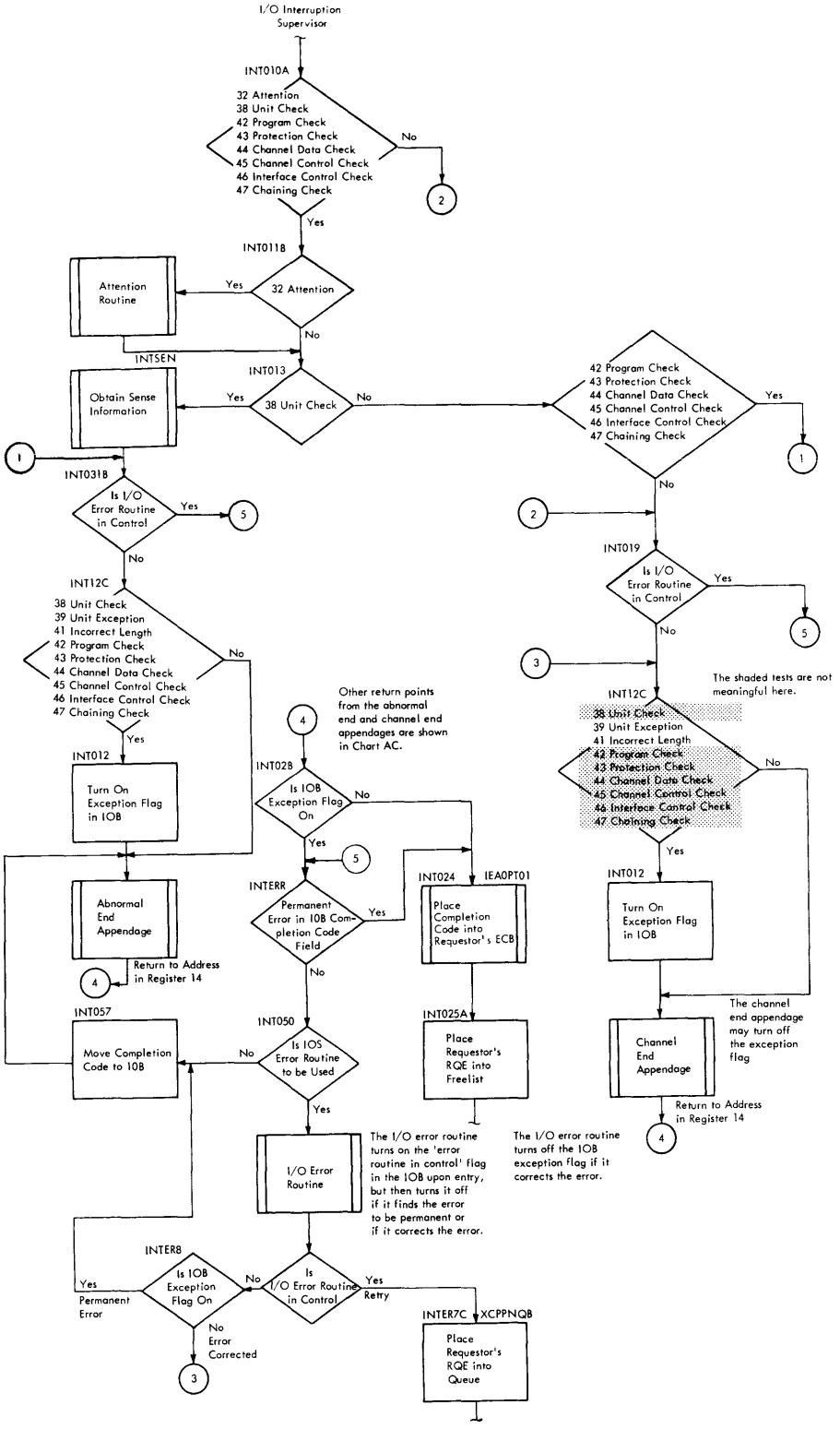

Figure 10. Setting I/O Error Flags

pointers to the listings; and a table showing the meanings of IOB sense bits, flags, and error count fields for the particular device.

The tables are to be used as guides in getting to and interpreting the listings, which should be considered the final authority. Also:

- Cross references may sometimes point to approximately where in a listing some action is taken. This is because some functions cannot be grouped 'cleanly.' As a result, some studying may be required to check fully what happens when a particular condition arises.
- The explanations of sense bit meanings are meant to be quick–reference guides. More information can be found in the publications mentioned with each routine.
- The priority of examination of status and sense bits is a design priority. In some cases a variation will be found in the implementation.

The examination of status and sense bits is usually performed by a small utility–type routine called the Error Interpreter routine, which is used in common by the error routines. It determines which status or sense bits are on, and returns control to requesting error routines at the instruction sequences where the errors can be handled.

Each time the Error Interpreter routine is entered, it checks one bit. An arrangement of offset values and addresses in a list within the requesting I/O error routine directs the Error Interpreter. The list indicates which bits are to be tested and in what order, and it also contains the addresses of the instruction sequences to be used for 'on' conditions.

If the system has the Channel Check Handler routine, and a channel error has occurred, the error recovery routine that is entered will have available to it an 8–byte area called the error recovery procedure interface block. This is produced by the Channel Check Handler routine and includes information that could be of use in determining whether or not a restart should be attempted.

1052 Error Routine

Special considerations are necessary for errors on 1052 console typewriters. Messages can be issued through the Write–to–Operator routine only for read errors. The operator is notified of other types of errors by use of the console alarm bell.

The 1052 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 1052 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The 1052 Error routine uses bits M0 and M1 in the third byte of the IOB flags field to control its procedure on subsequent entries after an error. If both bits are set to 0, the Error Interpreter routine is used to determine the type of error. If M0 has been set to 1, a permanent error has occurred and control has been received from the Error EXCP routine to ring the console alarm. If M1 has been set to 1, 'intervention required' has been signaled, and the original channel program is to be retried.

The error analysis sequence for the 1052 Printer–Keyboard is shown in Table 1. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Table 2. More information about the IBM 1052 Printer–Keyboard can be obtained from *IBM System/360 Component Descriptions and Operating Procedures: IBM 1052 Printer–Keyboard Model 7 with IBM 2150 Console,* GA22–6877.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when an invalid command code is detected. The IOB error flag is turned off and the IOB exception flag is turned on indicating a permanent error. Control is returned to the I/O supervisor via an SVC 15 instruction for abnormal termination.

Bit 1: Intervention Required

This bit is set when the printer runs out of forms or when the not–ready key has been depressed. The error routine places the control command to ring the console alarm in the reposition modifier field of the IOB. The modifier flag 1 is set in the IOB to signal the Unit Record SIO routine to build a CCW employing this command code. Bit M1 is set in the IOB and control returned by SVC 15. The intervention–required condition does not terminate a read or write operation that is already in progress.

Bit 2: Bus–Out Check

This bit is set when a parity error is detected on a command or data byte. The error routine sets the bus–out flag in the IOB and retries the user's channel

Table 1. IBM 1052 Printer–Keyboard Error Analysis Sequence (Module IGE0000D)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to: Read	Write	Pointer
1	45			Channel Control Check	X	X	ERR530
1	46			Interface Control Check	X	X	ERR530
2	47			Chaining Check	X	X	ERR524A
3	38			Unit Check	X	X	ERR501
4		0	7	Should Not Occur	X	X	ERR504
5		0	6	Should Not Occur	X	X	ERR504
6		0	5	Should Not Occur	X	X	ERR504
7		0	4	Should Not Occur	X	X	ERR504
8		0	3	Equipment Check	X	X	ERR506
9		0	1	Intervention Required	X	X	ERR509
10		0	2	Bus–Out Check	X	X	ERR510
11		0	0	Command Reject	X	X	ERR518A
12	44			Channel Data Check	X	X	ERR525
13	42			Program Check	X	X	ERR518A
14	43			Protection Check	X	X	ERR518A
15	39			Unit Exception	X		ERR518B
16	41			Incorrect Length	X	X	ERR518A

See page 27 for an explanation of the pointers.

Table 2. IBM 1052 Printer–Keyboard Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	——	——	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	Modifier Flag 1	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	——	Write Error Count	Bus-Out Error Count	Control Bit M1	Message Type	Control Bit M0	Logout Flag
Error Counts IOBECT Byte 1	——	——	——	——	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry	Channel Data Check and MCS Retry
Error Counts IOBECT Byte 2	——	——	——	——	——	——	——	Channel Control Check, Interface Control Check

program via SVC 15. If the error recurs, the control command to ring the console alarm is placed in the reposition modifier field of the IOB, and modifier flag 1 is set to signal the Unit Record SIO routine to construct a CCW with this command. IOB bit M0 is set and control returned via SVC 15. Five retries are attempted on console devices of systems with multiple console support.

Bit 3: Equipment Check

This bit is set when one of the following occurs:

- Keyboard parity error.
- Keyboard–printer compare check.
- Printer failed to take a mechanical cycle during a read or write operation.

If the error occurred on a read command, a permanent error is assumed and the Write–to–Operator routine is invoked; it writes a message (IEA000I) indicating failure to read input messages. For write errors, the error routine retries the channel program via SVC 15. On the second occurrence of the error, the console bell is rung via the procedure described above for bus–out check. Five retries are attempted on console devices of systems with multiple console support.

Bits 4–7: Should Not Occur

If any of these bits is set, a catastrophic error is assumed. A permanent error is signaled to the Unit Record SIO routine and control is returned via SVC 15. Five retries are first attempted on console devices of systems with multiple console support.

1285, 1287 and 1288 Error Routines

The 1285 Error routine (module IGE0011B), 1287 Error routine (module IGE0011C), and the 1288 Error routine (module IGE0011D) all attempt recovery from channel data checks. When the Channel Check Handler is included with a system, they also examine the error recovery procedure interface block to determine whether they should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 1285 Optical Reader is shown in Table 3, and the error analysis sequence for the IBM 1287 and 1288 Optical Readers is shown in Table 4. The meanings of sense bits, IOB flags, and IOB error counts for the three devices are shown in Table 5. More information can be obtained from the following publications:

- *IBM 1285 Optical Reader Component Description and Operating Procedures* GA24-3256
- *IBM 1287 Optical Reader Component Description and Operating Procedures,* GA21-9064
- *IBM 1288 Optical Page Reader Model 1 Component Description,* GA21-9081

Table 3. IBM 1285 Optical Reader Error Analysis Sequence (Module IGE0011B)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR0041
2	46			Interface Control Check	ERR0041
3	44			Channel Data Check	ERR0041
3	33			Status Modifier	ERR0041
3	34			Control Unit End	ERR0041
4	38			Unit Check	ERR0041
5		0	3	Equipment Check	ERR006C
6		0	1	Intervention Required	ERR006C
7		0	6	Non-Recovery	ERR006C
8		0	2	Bus-Out Check	ERR006C
9		0	4	Data Check	ERR006C
10		0	5	Overrun	ERR006C
11		0	0	Command Reject	ERR006C
12	47			Chaining Check	ERR04B1
13	42			Program Check	ERR04B1
14	43			Protection Check	ERR04B1
15	41			Incorrect Length	ERR04B1

See page 27 for an explanation of the pointers.

Table 4. IBM 1287 and 1288 Optical Readers Error Analysis Sequence

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR0041
2	46			Interface Control Check	ERR0041
3	44			Channel Data Check	ERR0041
4	32			Control Unit End	ERR0041
5	38			Unit Check	ERR0041
6		1	3	Should Not Occur	ERR006
6		1	5	Should Not Occur	ERR006
6		1	6	Should Not Occur	ERR006
6		1	7	Should Not Occur	ERR006
7		1	0	Tape Mode (1287 only)	ERR006
8		0	7	Should Not Occur	ERR006
9		0	3	Equipment Check	ERR006C
10		0	6	Non–Recovery	ERR006C
11		0	1	Intervention Required	ERR006C
12		0	2	Bus–Out Check	ERR006C
13		0	4	Data Check	ERR006C
14		0	5	Overrun	ERR006C
15		0	0	Command Reject	ERR006C
16		1	4	Invalid Operation	ERR006C
17	47			Chaining Check	ERR004B1
18	42			Program Check	ERR004B1
19	43			Protection Check	ERR004B1
20	41			Incorrect Length	ERR004B1

See page 27 for an explanation of the pointers.

Sense Byte Meanings

Byte 0, Bit 0: Command Reject

This bit is set when the command is incorrect for the operating mode, such as a Mark Line command in document mode or a normal command in CE diagnostic mode. An invalid command sequence, such as two consecutive ejects, will also cause the bit to be set.

Byte 0, Bit 1: Intervention Required

This bit is set when the device is not in ready status.

Byte 0, Bit 2: Bus–Out Check

This bit indicates that invalid parity has occurred in a command or data.

Table 5. IBM 1285, 1287, and Optical Readers Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Non-Recovery	Keyboard Correction (1285, 1287 Tape Mode Only)
Sense Byte 1 (1287, 1288 Only)	Tape Mode (1287 Only)	Late SS or End of Page	No Document Found	——	Invalid Operation	——	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	——	——	——	——	Message Type	——	Logout Flag
IOBINCAM (Byte 1)	Data Check Count							
IOBINCAM (Byte 2)	Incorrect Length Count							
IOB Error Counts Byte 1	Equipment Check Count							
IOB Error Counts Byte 2	Overrun Error Count				Bus-Out Count	Chaining Check Count		

Byte 0, Bit 3: Equipment Check

One of the following has occurred: (1) the device was unable to completely read a line or field, (2) the 1287 or 1288 could not locate the reference mark, or (3) the 1288 failed to find a timing mark.

Byte 0, Bit 4: Data Check

The optical reader has sent at least one reject character or substitute character.

Byte 0, Bit 5: Overrun
An overrun condition occurs when the channel fails to service the optical reader in time and at least one character is lost.

Byte 0, Bit 6: Non–recovery
The operator must reload and restart the optical reader because (1) the document or tape is jammed, (2) the runout key was depressed while a document or tape was being processed, or (3) the scanner door was open when the device was not in the line display mode.

Byte 0, Bit 7: Keyboard Correction
The 1287 or 1285 has displayed at least one unreadable character for online correction.

Byte 1, Bit 0: Tape Mode
The 1287 Model 2 is operating in the tape mode.

Byte 1, Bit 1: End of Page (1288)
The bottom of the page has been detected while reading in the unformatted document mode.

Byte 1, Bit 1: Late Stacker Select (1287)
The Stacker Select command did not arrive in time and the document was placed into the reject stacker.

Byte 1, Bit 2: No Document Found
A document did not enter the reading station after the last eject command and there was no jam.

Byte 1, Bit 3: Not Used

Byte 1, Bit 4: Invalid Operation
Invalid information was specified in the load format instruction. For example: bit 2, 3, 4, or 5 of the fourth byte represents bits not used; fewer than four bytes were transmitted; or an uninstalled font was specified in the CCW.

Byte 1, Bits 5–7: Not Used

1403 and 1443 Error Routine

The 1403 and 1443 Error routine attempts recovery from the special condition where channel data checks occur with bus–out checks. When the Channel Check Handler is included with a system, the 1403 and 1443 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 1403 Printer and the 1443 Printer is shown in Table 6. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 7. More information about the IBM 1403 and 1443 Printers can be obtained from the following publications:

- *IBM 1403 Printer Component Description,* GA24–3073
- *IBM 1443 Printer Models 1 to 4 and N1; IBM 1445 Printer Models 1 and N1,* GA24–3120

Table 6. IBM 1403 Printer and 1443 Printer Error Analysis Sequence (Module IGE0000G)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR051
1	46			Interface Control Check	ERR051
2	47			Chaining Check	ERR071
3	38			Unit Check	ERR053
4		0	6	Should Not Occur	ERR052F
5		0	3	Equipment Check	ERR052F
6		0	1	Intervention Required	ERR054
7		0	2	Bus–Out Check	ERR056
8		0	7	Channel 9	ERR059
9		0	0	Command Reject	ERR052E
10	44			Channel Data Check	ERR067
11	42			Program Check	ERR063
12	43			Protection Check	ERR063
13	39			Unit Exception	ERR064
14	41			Incorrect Length	ERR068

See page 27 for an explanation of the pointers.

The sequence shown above is for the 1403 without the Universal Character Set (UCS) feature, and for the 1443.

For 1403s with UCS, bits 4 and 5 of sense byte 0 mean 'data check' and 'parity check,' respectively. Their priority falls between 9 and 10 and 5 and 6, respectively.

9.1		0	4	Data Check	ERR052E
5.1		0	5	Parity Check	ERR052D

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when one of the following occurs:

- A Read Backward command is received.
- A carriage instruction to space more than three lines is received.
- A carriage instruction to skip to channel 0, 13, 14, or 15 of the carriage control tape is received.
- Any command is received which the device is not designed to execute.

The error is considered permanent.

Table 7. IBM 1403 Printer and 1443 Printer Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check / Typebar Selection	Parity Error / Typebar Selection	—	Channel 9
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	—	—	Exceptional Condition	—	0 Start 1 Restart
IOBFL3	—	Entry Bit	UCS Parity Error Count	Bus-Out or Channel Data Check Error Count	—	Message Type	—	Logout Flag
Error Counts IOBECT Byte 1	—	—	—	—	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry	Multiple Console Support Retry
Error Counts IOBECT Byte 2	—	—	—	—	—	—	—	Channel Control Check, Interface Control Check

Bit 1: Intervention Required

This bit indicates a not–ready condition due to one of the following:

- The printer has run out of forms or the forms have jammed.
- The Stop Key has been depressed.
- The cover interlock switch is open.
- The typebar motor switch is set to the OFF or REMOVE position.

When this bit and bit 7 (Channel 9) are on, the error is handled as a Channel 9 condition. In all cases, an Intervention Required message is issued to the operator who must correct the condition. When the intervention required condition alone is corrected, the last operation is repeated.

Bit 2: Bus–Out Check

This bit indicates that a parity error has occurred on a bus–out command or data byte. If this bit is set during the initial selection of a control unit or a device, the operation is retried. If it is set during channel end, the error is automatically considered permanent unless it occurs on the console device of a system having the Multiple Console Support feature, where it is retried five times.

Bit 3: Equipment Check

This bit indicates that a program–correctable malfunction was detected in the printer or in its controls. The malfunctions are buffer or hammer checks on the 1403 and typebar–synchronization errors on the 1443. These errors are reset by the next Write or Control command. Five retries are attempted on systems with

multiple console support before the error is considered permanent, if the printer is being used as a console. Otherwise, the error is considered to be permanent, and no retry is attempted.

Bit 4: Data Check (1403 Only)
If the 1403 has the Universal Character Set (UCS) feature, this bit is set when a code in a data record sent to the printer does not match a code in the UCS feature storage. (Without UCS, this bit should not be set.) The error is automatically considered permanent unless it occurs on the console device of a system having the Multiple Console Support feature, where it is retried five times.

Bit 5: Parity Error (1403 Only)
If the 1403 has the Universal Character Set (UCS) feature, this bit indicates a parity error was detected in data being written into or read from UCS feature storage. If the error occurs while the UCS storage is being loaded, one retry is attempted. If it occurs at any other time, the error is considered permanent. In systems having the Multiple Console Support feature, five retries are attempted for console devices.

Bits 4 and 5: Typebar Selection (1443 Only)
The combination of these two bits indicates the position of the typebar selector switch.

Bit 4	Bit 5	Switch Setting
0	0	52-character set
0	1	13-character set
1	0	39-character set
1	1	63-character set

These bits can be changed only by repositioning the typebar selector switch. They are considered normal, and error routine coninues the channel program.

Bit 6: Should Not Occur
If this bit is set, a catastrophic error is assumed. The logout flag is set in the IOB, a permanent error is signaled to the Error EXCP routine, and control is returned via SVC 15.

Bit 7: Channel 9
This bit is set when a hole is sensed in channel 9 of the carriage control tape.

1419/1275 Error Routine

The 1419/1275 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 1419/1275 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 1419/1275 Magnetic Character Reader is shown in Table 8. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 9. Sense byte 2 is applicable only to the secondary control unit of systems with the Dual Address Adapter feature.

More information can be obtained from the following publications:

- *IBM 1219 Reader Sorter, IBM 1419 Magnetic Character Reader,* GA24–1499
- *IBM 1419 Magnetic Character Reader and IBM 1275 Optical Reader Sorter, Device–Dependent BSAM Program Logic Manual,* GY21–0012

Table 8. IBM 1419/1275 Magnetic Character Reader Error Analysis Sequence (Module IGE0011E)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR020
2	46			Interface Control Check	ERR020
3	44			Channel Data Check	ERR020
4	38			Unit Check	ERR020
5		0	3	Should Not Occur	ERR051
6		0	7	Document Spacing Error	ERR051
7		0	1	Intervention Required	ERR051
8		0	2	Bus–Out Check	ERR051
9		0	4	Data Check	ERR051
10		0	5	Overrun	ERR051
11		0	6	Auto Select	ERR051
12		0	0	Command Reject	ERR051
13	47			Chaining Check	ERR069
14	42			Program Check	ERR069
15	43			Protection Check	ERR069
16	41			Incorrect Length	ERR069

For the secondary control unit, the following sense bytes are examined in place of those shown above:

5		2	2	Bus-Out Check	ERR061
6		2	4	Should Not Occur	ERR061
7		2	3	Should Not Occur	ERR061
8		2	1	Intervention Required	ERR061
9		2	7	Operator Attention	ERR061
10		2	0	Command Reject	ERR061
11		2	5	Late Stacker Select	ERR061
12		2	6	Auto Select	ERR061

See page 27 for an explanation of the pointers.

Table 9. IBM 1419/1275 Magnetic Character Reader Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	——	Data Check	Overrun	Auto-Select	——
Sense Byte 1	——	——	Document Under Read Head	Amount Field Valid	Process Control Field Valid	Account Number Field Valid	Transit Field Valid	Serial Number Field Valid
Sense Byte 2 (Secondary Control Unit Only)	Command Reject	Intervention Required	Bus-Out Check	——	——	Late Stacker	Auto-Select	Operator Attention
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	——
IOBFL2	——	Sense Bit	Purge Flag	——	——	——	——	——
IOBFL3	——	——	——	——	——	Permanent Error	——	Logout Flag

IBM 1419/1275 Magnetic Character Reader Sense Byte Meanings

Byte 0, Bit 0: Command Reject

This bit is set when an invalid command is received. Invalid commands include:

- Two Read commands without an intervening Stacker Select command when the 1419 is in program–sort mode
- A Stacker Select command given for an auto–selected document
- A second Stacker Select command after one has been accepted for a document
- A Write command given when the machine is not in diagnostic mode

Byte 0, Bit 1: Intervention Required
This bit indicates that operator attention is needed for one or more of the following reasons:

- Document jam
- Full stacker
- Sort–check
- Endorser stop
- End–of–transport stop
- Film stop
- Batch number advance check stop
- Motor not running

Byte 0, Bit 2: Bus–Out Check
This bit is set for parity errors on information coming from the CPU via the interface.

Byte 0, Bit 3: Should Not Occur

Byte 0, Bit 4: Data Check
This bit indicates that one or more of the selected fields in the document was not read correctly.

Byte 0, Bit 5: Overrun
This bit is set when a character is not accepted. The field containing the error is identified by a 0 in bits 3 to 7 of sense byte 1.

Byte 0, Bit 6: Auto-Select
This bit is set when a document is automatically selected into the reject pocket. A 51–column card turns the indicator on if the 51–column feature is not installed. If a Stacker–Select command is issued for an auto–selected document, the command reject bit will be set.

Byte 0, Bit 7: Should Not Occur

Byte 1, Bit 0: Should Not Occur

Byte 1, Bit 1: Should Not Occur

Byte 1, Bit 2: Document Under Read Head
This bit is normally used in diagnostic mode only.

Byte 1, Bit 3: Amount Field Valid[1]

Byte 1, Bit 4: Process Control Field Valid[1]

Byte 1, Bit 5: Account Number Field Valid[1]

Byte 1, Bit 6: Transit Field Valid[1]

Byte 1, Bit 7: Serial Number Field Valid[1]

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[1]When this field is selected at the operator panel, and is read without error (including symbols), the bit is set to one.

Byte 2 (Secondary Control Unit Only):

Byte 2, Bit 0: Command Reject
This bit is set when an invalid command is received by the secondary control unit (SCU). The following commands are considered invalid in the SCU:

- Read
- Read Backwards
- Write

Byte 2, Bit 1: Intervention Required
See byte 0, bit 1.

Byte 2, Bit 2: Bus–Out Check
This bit is set for parity errors on information coming from the CPU via the interface.

Byte 2, Bit 3: Should Not Occur

Byte 2, Bit 4: Should Not Occur

Byte 2, Bit 5: Late Stacker Select.
This bit is set when a Stacker–Select command is given for a document which has passed the select station. The document is rejected.

Byte 2, Bit 6: Auto–Select
This bit is set when a Stacker–Select command is issued for a document that is auto–selected.

Byte 2, Bit 7: Operator Attention
This bit is set when the Update switch is off and a Stacker–Select command is issued to effect batch–numbering update.

1442, 2501, and 2520 Error Routine

The 1442, 2501, and 2520 Error routine attempts recovery from channel data checks on 1442, 2501, and 2520 read errors. Each read operation is retried once.

The error analysis sequence for the IBM 1442 Card Read Punch, 2501 Card Reader, and 2520 Card Read Punch is shown in Table 10. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Table 11. More information about the individual devices can be obtained from the following publications:

- *IBM 1442–N1 and N2 Component Description and Operating Procedures,* GA21–9025
- *IBM 2501 Models B1 and B2 Component Description and Operating Procedures,* GA21–9026
- *IBM 2520–B1, B2, and B3 Component Description and Operating Procedures,* GA21–9027

Table 10. IBM 1442 Card Read Punch, 2501 Card Reader, and 2520 Card Read Punch Error Analysis Sequence (Module IGE0000E)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR002
1	46			Interface Control Check	ERR002
2	38			Unit Check	ERR002
3		0	6	Should Not Occur	ERR004
4		0	3	Equipment Check	ERR008
5		0	7	Should Not Occur	ERR004
6		0	1	Intervention Required	ERR036
7		0	2	Bus–Out Check	ERR013
8		0	4	Data Check	ERR017
9		0	5	Overrun	ERR020
10		0	0	Command Reject	ERR006
11	44			Channel Data Check	ERR035
12	47			Chaining Check	ERR029
13	42			Program Check	ERR029
14	43			Protection Check	ERR029
15	39			Unit Exception	ERR029
16	41			Incorrect Length	ERR029

See page 27 for an explanation of the pointers.

Table 11. IBM 1442 Card Read Punch, 2501 Card Reader, and 2520 Card Read Punch Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	——	——
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL3	——	Entry Bit	Read Error Count	Bus-Out Error Count	Data Check Flag	Message Type	Overrun Count	Logout Flag

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when a Read Backward command is issued, or when any other command is received which the device has not been designed to execute. The error is considered permanent.

Bit 1: Intervention Required

This bit is set when one of the following occurs:

- The power is off.
- Cards are not registered at the read station.
- The stacker is full.
- The feed check light is on.
- The stop key has been depressed.
- The chip box is full, or has been removed.
- There are no cards in the hopper and the End–of–File light is not on.
- The cover interlock switch is open.

A message is given the operator, who must take action. Upon correction of the condition, the interrupted operation is repeated.

Bit 2: Bus–Out Check

This bit is set when a parity error has occurred on bus–out during transfer of command or data bytes, but not during the time period of address–out or command–out proceed. For a command byte one retry is attempted. If the error is not corrected it is considered permanent. For a data byte, the card is already punched and the error is considered permanent. However, on a 2501, the error is automatically retried once.

Bit 3: Equipment Check

This bit is set when one of the following occurs:

- An invalid card code is detected during a punch operation.
- During a read or punch operation an error is detected during the 9–bit match.

The invalid card code part of equipment check is not set during card image punch.

If the error occurs during a punch operation other than QSAM, it is automatically considered permanent. With QSAM an error occurring during a punch operation is retried. If it occurs during a read operation, one retry is attempted.

Bit 4: Data Check

This bit is set when an invalid card code is detected during a read operation. This error pertains to the last card for which data was sent. A message is typed and an operator must reposition the cards for one retry. If the error persists, it is considered permanent.

Table 12. IBM 2250 Display Unit Error Analysis Sequence (Module IGE0010A)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to 2250–1	Applicable to 2250–2	Pointer
1	45			Channel Control Check	X	X	ASRON
2	46			Interface Control Check	X	X	ASRON
3	44			Channel Data Check	X	X	TESTST
4	38			Unit Check	X	X	MAINER
5		0	1	Should Not Occur	X		SEROUT
5		0	3	Should Not Occur	X	X	SEROUT
5		0	5	Should Not Occur	X	X	SEROUT
5		0	7	Should Not Occur	X	X	SEROUT
6		0	2	Bus-Out Check	X	X	B01CHK
7		0	4	Data Check	X	X	DATACX
8		0	0	Command Reject	X	X	PERMER
		0	0	Command Reject	Note 1		PERMER
9		0	6	Buffer Running	X	X	
10	42			Program Check	X	X	PERMER
11	43			Protection Check	X	X	PERMER
12	41			Incorrect Length	X	X	PERMER

See page 27 for an explanation of the pointers.

Note: For an unbuffered 2250 Model 1 the following changes are necessary:

a. Command Reject with Buffer Running is a 'Should Not Occur' condition with Priority 5, Pointer SEROUT.

b. Priorities 10, 11, and 12 become 9, 10, and 11, respectively.

Bit 5: Overrun

This bit is set if during a read operation the interface has not transmitted a character by the time the next character is to be read into the register. The operator must reposition the cards. The operation is retried once and if the error persists it is considered permanent, and a message is written to the console.

Bits 6 and 7: Should Not Occur

If either of these bits is set, a catastrophic error is assumed. A permanent error is signaled to the Error EXCP routine and control is returned via SVC 15.

2250 Error Routine

The 2250 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 2250 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 2250 Display Unit is shown in Table 12. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 13. More

information about the IBM 2250 Display Unit can be obtained from the following publications:

- *IBM System/360 Component Description: IBM 2250 Display Unit Model 1,* GA27-2701
- *IBM System/360 Component Description: IBM 2250 Display Unit Model 2; IBM 2840 Display Control Model 1,* GA27-2702

Table 13. IBM 2250 Display Unit Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	———	Bus-Out Check	Equipment Check (Model 2)	Data Check	———	Buffer Running	———
Sense Byte 1	Light Pen Defect	End Order Sequence	Character Mode	———	———	2840 Output Check	2840 Input Check	———
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	———	———	Exceptional Condition	———	0 Start 1 Restart
IOBFL2	Halt I/O Issued	Sense Flag	———	———	———	———	Film Unit Flag	———
IOBFL3	———	———	———	———	———	Message Type	———	Logout Flag
IOB Error Counts Byte 1	Bus-Out 1 Retry Indicator	Bus-Out 2 Retry Indicator	Data Check	Equipment Check	2840 Input Check	2840 Output Check	Abnormal End Appendage Bit	Channel Data Check
IOB Error Counts Byte 2	Interface Control Check or Channel Control Check	———	———	———	———	———	———	———

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when there is an invalid modifier bit in a command or an invalid invalid command sequence. The error is considered permanent.

Bit 1: Should Not Occur

When this bit is set, a catastrophic error is assumed. The logout flag in the IOB is set and the permanent error procedure is performed.

Bit 2: Bus–Out Check
This bit is set when a parity error is detected on a command or data byte during bus–out. The operation is retried once. If the retry is unsuccessful, a message is written to the operator.

Bit 3: Equipment Check (Model 2); Should Not Occur on Others (See Bit 1).

Bit 4: Data Check
This bit is set when a buffer parity error is detected either during a read operation or during image regeneration. The operation is retried once. If the retry is unsuccessful, a message is written to the operator.

Bit 5: Should Not Occur (See Bit 1)

Bit 6: Buffer Running
This bit indicates that regeneration is in process. When accompanied by Command Reject, a permanent error is assumed.

Bit 7: Should Not Occur (See Bit 1)

Table 14. IBM 2260 Display Station and 1053 Printer Error Analysis Sequence (Load 1—IGE0010B or Load 2—IGE0110B)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to 2260	Applicable to 1053	Pointer	Load[1]
1	45			Channel Control Check	X	X	ASRON	1
2	46			Interface Control Check	X	X	ASRON	1
3	44			Channel Data Check	X	X	TESTST	1
4	38			Unit Check	X	X	MAINER	1
5		0	4	Should Not Occur	X	X	SEROUT	1
5		0	5	Should Not Occur	X	X	SEROUT	1
5		0	6	Should Not Occur	X	X	SEROUT	1
6		0	3	Equipment Check	X		EC	1
7		0	1	Intervention Required		X	2260–SEROUT 1053–WOPOST	1
8		0	2	Bus–Out Check Initial Selection	X	X	B01	1
8		0	2	Bus–Out Check Data Transfer	X		ISBUSOUT	1
8		0	2	Bus–Out Check Data Transfer		X	ISBUSOUT	1
9		0	0	Command Reject	X	X	PERMER	1
10	42			Program Check	X	X	PERMER	1
11	43			Protection Check	X	X	PERMER	1
12	41			Incorrect Length	X	X	PERMER	1

[1]Only first–time equipment check errors are handled by load 2.

See page 27 for a explanation of the pointers.

2260 and 1053 Error Routine

The 2260 and 1053 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 2260 and 1053 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 2260 Display Station and IBM 1053 Printer is shown in Table 14. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 15. More information about the IBM 2260 Display Station and 1053 Printer can be obtained from the publication *IBM System/360 Component Description: IBM 2260 Display Station; IBM 2848 Display Control,* GA27-2700.

Table 15. IBM 2260 Display Station and 1053 Printer Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	—	—	—	—
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	—	—	Exceptional Condition	—	0 Start 1 Restart
IOBFL2	—	Sense Flag	—	—	—	—	Film Unit Flag	—
IOBFL3	—	—	—	—	—	Message Type	—	Logout Flag
IOB Error Counts Byte 1	Bus-Out Count 1	Bus-Out Count 2	Bus-Out Count 3	Error Routine Channel Program	—	Channel Data Check	Abnormal End Appendage Bit	Check
IOB Error Counts Byte 2	Interface Control Check or Channel Control Check	—	—	—	—	—	—	—

Sense Byte Meanings and Actions Taken

Bit 0: Command Reject This bit is set when there is an invalid modifier bit in a command, or an invalid command sequence. The error is considered permanent.

Bit 1: Intervention Required
This bit is set when a Write 1053 Printer command is given but the 1053 Printer is not ready. A message is written to the operator.

Bit 2: Bus–Out Check
This bit is set when a parity error is detected on a command or data byte during bus–out. Processing depends upon when the bus–out check occurred and what command was last executed:

If the bus–out check occurred during initial selection, or during data transmission for the 2260 after a Write Line Address or an Erase command, one retry is attempted. If the retry is unsuccessful a message is written to the operator.

If the bus–out check occurred during data transmission for the 2260 after a Write Buffer Storage command, one retry is attempted, but before that retry an Erase Buffer Storage command is issued. If the retry is unsuccessful, a message is written to the operator.

Bit 3: Equipment Check
This bit is set when a parity error is detected during a manual read input operation. The second load of the 2260 and 1053 Error routine erases the message in error and displays an error message on the screen. No automatic retry occurs. If a retry is desired, the necessary coding must be included in the user's program. (If the error occurs a second time, the user's program should consider it permanent.)

Bits 4–7: Should Not Occur
If one of these bits is set, a catastrophic error condition is assumed. The logout bit in the IOB is set, and a permanent error procedure is performed.

2301, 2302, 2303, 2305, 2311, 2314, 2321, and 3330 Error Routine

This routine has several resident versions, one of which is chosen during system generation to service the types of devices at an installation.

This routine attempts recovery from channel data checks. If the Channel Check Handler is included with the system, it also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

Channel programs are usually restarted from the beginning to avoid a repositioning problem, command and data chaining problems, and to simplify the handling of errors within errors.

When a track condition check error occurs, the home address record and record 0 are read to determine whether the track is defective or is an alternate track. If the track is defective, the address of the alternate track is used in a Seek command, and the the operation is resumed on the alternate track. If the track condition check occurred on an alternate track, the defective track's address, plus 1, is used in a Seek command and the operation is resumed on the new track.

When a no–record–found error occurs, a console message is not issued if the access arm has been positioned at the correct track. A 'permanent error' indicator is set in the input/output block.

When the overflow incomplete bit (sense byte 1, bit 7) is set, only a partial record has been read or written, and a CCW is constructed so the remainder of the record can be processed. When the overflow incomplete bit is set and the file mask violation, end of cylinder, or track condition check bit is also set, the error routine assumes that the first record of the continuation track is properly identified as record number 1.

This error routine handles cylinder and head switching for both sequential and split cylinders.

When a 2305 or 3330 presents a unit check, IOS performs a sense I/O command for 24 bytes and then enters the resident direct access ERPs. The ERP then checks the error indications in the CSW and sense bits according to the following precedence table (Table 17) until a bit is found on. The action referred to will then be performed.

The control units for the 2305 and 3330 have an error correction capability known as the Error Correction Function, or ECF. If a data check occurs in a count or key area, the control unit performs ECF internally. If a data check occurs in the data field, the sense bytes contain a displacement and a 3–byte correction code for the ERP to use in correcting the error.

The 3330 control unit presents the displacement to the error starting from the beginning of the data field, which allows the ERP to apply the correction code when data chaining is being performed in the data field. Because the 2305 control unit presents the displacement from the last byte transferred, the ERP only corrects the last segment if data chaining in the data field is used. If the error is not in the last segment, up to ten retries are performed, but the correction code is not applied.

The ECF supplied by the 3330 and 2305 corrects up to three contiguous bytes of data.

The error analysis sequence for the IBM 2301 Drum Storage, 2302 Disk Storage, 2303 Drum Storage, 2311 Disk Storage Drive, and 2314 Direct Access Storage Facility is shown in Table 16. Table 17 shows the error analysis sequence for the IBM 2305 Fixed Head Storage and 3330 Disk Storage. The meanings of sense bits, IOB flags, and IOB error counts for all of the direct access devices are given in Table 18. More information about the individual devices can be obtained from the following publications:

- *IBM System/360 Component Descriptions — 2841 and Associated DASD,* GA26–5988
- *IBM System/360 Component Descriptions: 2314 Direct Access Storage Facility and 2844 Auxiliary Storage Control,* GA26–3599
- *IBM System/360 Component Descriptions: 2820 Storage Control and 2301 Drum Storage,* GA22–6895
- *IBM System/360 Component Descriptions: 2835 Storage Control and 2305 Fixed Head Storage,* GA26–1589
- *IBM System/360 Component Descriptions: 3830 Storage Control and 3330 Disk Storage,* GA26–1592

Table 16. IBM 2301 Drum Storage, 2302 Disk Storage, 2303 Drum Storage, 2311 Disk Storage Drive, 2314 Direct Access Storage Facility, and 2321 Data Cell Error Analysis Sequence (Module IEC23XXF)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERNT
2	46			Interface Control Check	ERNT
3	44			Channel Data Check	ERNT
4		0	3	Equipment Check	ERNT
5		1	4	No Record Found	ERNT
6		0	7	Seek Check	ERNT
7		0	1	Intervention Required	ERNT
8		0	2	Bus–Out Check	ERNT
9		0	4	Data Check	ERNT
10		0	5	Overrun	ERNT
11		1	6	Missing Address Markers	ERNT
12		0	0	Command Reject	ERNT
13		0	6	Track Condition Check	ERNT
14		1	1	Track Overrun	ERNT
15		1	2	End of Cylinder	ERNT
16		1	5	File Protect	ERNT
17	38			Unit Check	ERNT
18	47			Chaining Check	ERNT
19	42			Program Check	ERNT
20	43			Protection Check	ERNT
21	39			Unit Exception	ERNT
22	41			Incorrect Length	ERNT

IEC23XXF logs statistics in the System Data Recording work area for all direct–access devices.
See page 27 for an explanation of the pointers.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

When this bit and bit 5 of sense byte 1 (File Protected) are set, the write inhibit portion of the file mask has been violated.

When this bit and bit 3 of byte 1 (Invalid Command Sequence) are set, one of the following has occurred:

- A Write command was not preceded by the necessary Search or Write command.

Table 17. IBM 2305 Fixed Head Storage and 3330 Disk Storage Error Analysis Sequence (Module IEC23XXF)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERNT
2	46			Interface Control Check	ERNT
3	44			Channel Data Check	ERNT
4	47			Chaining Check	ERNT
5		1	0	Permanent Error	ERNT
		0	3	Equipment Check	ERNT
7		0	2	Bus–Out Check	ERNT
8		0	1	Intervention Required	ERNT
9		0	0	Command Reject	ERNT
10		1	4	No Record Found	ERNT
11		0	5	Overrun	ERNT
12		1	1	Invalid Track Format	ERNT
13		0	4	Data Check	ERNT
14		1	2	End of Cylinder	ERNT
15		1	5	File Protect	ERNT
16		1	7	Overflow	ERNT
17	38			Unit Check	ERNT
18	42			Program Check	ERNT
19	43			Protection Check	ERNT
20	39			Unit Exception	ERNT
21	41			Incorrect Length	ERNT

IEC23XXF logs statistics in the System Data Recording work area for all direct–access devices.
See page 27 for an explanation of the pointers.

- A Set File Mask, Reserve, or Release command has been issued in a chain where a previous Set File Mask command was given.
- Head switching is being attempted in a command chain not containing a previous seek.
- Space count has been chained from a Write command.
- A formatting command is being attempted after record 0 on a defective track or following a record which is flagged as an overflow record.

When this bit and bit 7 of byte 0 (seek check) are set, the 2841 detected an invalid seek address or was given a seek address consisting of fewer than six bytes. A seek is not initiated.

Table 18. IBM 2301 Drum Storage, 2302 Disk Storage, 2303 Drum Storage, 2305 Fixed Head Disk Storage, 2311 Disk Storage Drive, 2314 Direct Access Storage Facility, 2321 Data Cell (handled by 2321 error routine), and 3330 Disk Storage Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0 2301, 2305, 3330	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	———	Invalid Address (2301 only)
Sense Byte 0 All Except 2301, 2305, 3330	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Track Condition Check	Seek Check
Sense Byte 1 2301	Data Check in Count Area	Track Overrun	End of Cylinder	Invalid Command Sequence	No Record Found	File Protected	Service Overrun	Overflow Incomplete
Sense Byte 1 2305, 3330	Permanent Error	Invalid Track Format	End of Cylinder	———	No Record Found	File Protected	Write Inhibit (3330 only)	Operation Incomplete
Sense Byte 1 All Except 2301, 2305, 3330	Data Check in Count Area	Track Overrun	End of Cylinder	Invalid Command Sequence	No Record Found	File Protected	Missing Address Marker	Overflow Incomplete
Sense Byte 2 2305, 3330	Buffered Log Full (2305 only)	Correctable	———	Environmental Data Present	———	———	———	———
IOBFL1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	———	———	Exceptional Condition	———	0 Start 1 Restart
IOBFL2	———	Sense Bit	Purge Flag	Read Home Address Flag	No End Extent Flag	Track Address Update Flag	———	———
IOBFL3 2321	Indicator 1	Track Condition Flag	No Record Found	Pick Flag	Restore Flag	Message Type	Sweep Flag	Logout Flag
IOBFL3 All Except 2321	Indicator 1	Track Condition Flag	No Record Found	Bus-Out Error Count	Restore Flag	Message Type	———	Logout Flag
IOB Error Counts Byte 1 2321	Bits Incremented for: No Record Found, Bus-Out Check, Seek Check, Chaining Check, Data Check, Overrun and Missing Address Marker				Bits Incremented for Data Check or Missing Address Marker			
IOB Error Counts Byte 2 2321	Incremented for Data Check or Missing Address Marker							
IOB Error Counts Byte 1 2301, 2311	Data Check Count							
IOB Error Counts Byte 2 2301, 2311	Write Indicator	Overrun Count or Chaining Check Count			No Record Found, Missing Address Marker, or Seek Check Count			

This table applies to all direct access devices, including the 2321 Data Cell Drive, which is handled by the 2321 Error routine

*This bit may be used to indicate "write inhibit." In such a case, the command reject bit (byte 0, bit 0) is also turned on.

When the command reject bit is on and the File Protected, Invalid Command Sequence, or Seek Check bits mentioned above are not on, one of the following has occurred:

- An invalid command was given.
- An invalid file mask was given.
- The sum of a key length plus data length exceeds $2^{16}-1$.
- An IPL command was given after a Set File Mask command.
- Command out has been presented in response to a request for the first byte of a Write Home Address CCW.

Bit 1: Intervention Required
This bit indicates that the device is not physically attached to the system, or is physically attached but is not available for use because the file motor is not on, a cover is open, etc.

Bit 2: Bus–Out Check
This bit is set when a parity error is detected during information transfer from the channel to the control unit. The check is an odd parity check which is made on control, write, and search operations. (Parity errors which are detected during command transfer result in bus–out checks and not command reject.) Ten retries are attempted. If the error remains uncorrected, a message is written to the operator and the control unit is considered inoperative.

Bit 3: Equipment Check
This bit indicates a malfunctioning control unit or device. A message is written to the operator. Except for 2305 and 3330, the conditions that cause this bit to be set are defined in sense byte 2, bits 0, 2, 4, and 5.

Bit 4: Data Check
This bit is set when an error is defected in the information received from the device. Data Check will usually occur when an attempt is made to read a record which overflows a track. For the 2305 and 3330, if the correctable bit (byte 2, bit 1) is on, the Error Correction Function is used.

Bit 5: Overrun
This bit is set when a chained CCW is received too late to be properly executed or when channel response is too slow during data transfer. Ten retries are attempted. If the retries are unsuccessful the error is considered permanent and a message is written to the operator. An overrun condition always results in an immediate stop of data transmission. For Write operations, the record area is padded with zeros.

Bit 6: Track Condition Check (All except 2301)
This bit is set when one of the following conditions has occurred:

- Any single track command other than Search Home Address, Read Home Address, or Read Record 0 is executed on a defective track.
- Any multitrack command other than Search Home Address, Read Home Address, or Read Record 0 causes a switch to a defective track, or an overflow operation is attempted to a defective track.

- Any multitrack command or overflow operation attempts to switch from an alternate, or defective track on which a read or search type command has been executed.

Bit 7: Seek Check

This bit is set when the device is unable to successfully complete a seek because:

- The seek address is invalid. Command Reject (byte 0, bit 0) is also set.
- The seek address consists of fewer than six bytes. Command Reject (byte 0, bit 0) is also set.
- The access mechanism has malfunctioned.
- The last three bytes at the track's home address are not identical to the last three bytes of the seek address.

The meanings of sense bits, IOB flags, and IOB error counts have been combined for the 2301, 2302, 2303, 2311, and 2314 and are shown in Table 16. Table 17 shows the combination for 2305 and 3330. More information about the IBM 2321 Data Cell Drive can be obtained from the following publication: *IBM System/360 Component Descriptions — 2841 and Associated DASD,* GA26–5988.

2400/3400 Tape Series Error Routine

The 2400/3400 Tape Series Error routine uses two operations designed to clear or circumvent sections of the tape that are presumably contaminated or defective. These operations are (1) the tape cleaner action and (2) the erase gap action.

The tape cleaner action is a "shoe shining" operation in which the tape is run back and forth to produce a wiping action both at the read head and at the tape cleaner blade. This action transfers contaminants from the read head to the tape and from the tape to the cleaner blade.

If the tape is being read forward, the cleaner action consists of a backward motion (toward the supply reel) equal in length to five records, followed by a forward motion equal in length to four records, positioning the read/write head at the beginning of the record that was being read when the data check occurred.

If the tape is being read backward, the cleaner action consists of a backward motion equal in length to four records, followed by a forward motion equal in length to five records, positioning the read/write head at the end of the record that was being read when the data check occurred.

The erase gap action is performed whenever a write error is detected. It consists of erasing a 3–1/2 inch portion of the tape, starting at the beginning of the write area assumed to be defective. This action treats the error as unrecoverable; the gap is a detour around the defective area.

The noise bit (byte 1, bit 0) is set if a data check occurs and: phase encoding (PE) is used; or non–return–to–zero–inverted recording (NRZI) is used. If a data check occurs and the noise bit is not set, it is assumed that the data check may have been caused by too short a record block. In this case, the record length is checked, and if it is less than 12 bytes, the record block is defined as a "noise block." Noise blocks are skipped and treated as permanent errors except when found by an integrated emulator on 7–track tapes; then all noise blocks are returned to the emulator for further processing. The DEBOFLGS field of the DEB identifies the tape as an emulator tape.

The error routines also treat parity errors differently on 7–track tapes being read by an integrated emulator. Rather than being a permanent error, the parity is switched (DEBVMOD field of the DEB) and the block reread in the alternate parity until 10 read–recovery sequences have been executed (40 retries) or the read is successful. After 10 read–recovery sequences, the parity is switched back to the original parity and the block is reread until 10 read–recovery sequences have been executed (a permanent error) or the read is successful.

Table 19. IBM 2400/3400 Series Magnetic Tape Units Error Analysis Sequence (Load 1—IGE0000I, Load 2—IGE0100I, Load 3—IGE0200I, Load 4—IGE0300I, Load 5—IGE0400I, or Load 6—IGE0900I)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to: Read	Write	Control	Pointer	Load[1]
1	45			Channel Control Check	X	X	X	ER2404B	4
2	46			Interface Control Check	X	X	X	ER2404B	4
3	38			Unit Check	X	X	X	ER2404B	4
4		0	3	Equipment Check	X	X	X	ER2404A	4
5		0	2	Bus–Out Check	X	X	X	ER2404A	4
6		0	1	Intervention Required	X	X	X	ER2404A	4
7		0	0	Command Reject	X	X	X	ER2404A	4
8		0	5	Overrun	X	X		ER2404A	4
9		1	4	Load Point	X	X		ER2404A	4
10		0	4	Data Check	X	X	X	ER2404A	4
11		7	4	Data Security Erase			X	ER2402A	2
12	44			Channel Data Check	X	X	X	ER2404A	4
13		0	7	Data Converter Check	X			ER2404A	4
14		1	7	Not Capable	X			ER2404A	4
15		5	3	PE ID Burst Check		X	X	ER2401A	1
16				No Previous Sense Bits On	X	X	X	ER2404A	4
17	47			Chaining Check	X			ER2404B	
18	42			Program Check	X	X	X	ER2404B	4
19	43			Protection Check	X			ER2404B	4
20	41			Incorrect Length	X	X		ER2404B	4

[1] Only errors that occur during Read–opposite recovery are handled by Load 3.

See page 27 for an explanation of the pointers.

Table 20. IBM 2400/3400 Series Magnetic Tape Units Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Overrun	Word Count Zero	Data Converter Check
Sense Byte 1	Noise Bit	Unit Status A	Unit Status B	7-Track Tape Unit	Tape at Load Point	Unit in Write Status	File Protect Status	Not Capable
Sense Byte 2	———	———	———	———	———	———	Multi Error	Track Exists
Sense Byte 3	Read/Write Vertical Redundancy Check	Longitudinal Redundancy Check	Skew	Cyclic Redundancy Check	Skew Register Vertical Redundancy Check	Phase Encoding	Backward	C-Compare
Sense Byte 4	———	Reject Tape Unit	Read Clock	Write Clock	Delay Counter	C Sequence	B Sequence	A Sequence
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	Reposition Tape	Cyclic Redundancy Check Bit	Exceptional Condition	———	0 Start 1 Restart
IOBFL 2	———	Sense Bit	Purge Flag	———	Read/Write Unit Exception	Use Read Opposite Recovery CCW from IOB	———	———
IOBFL 3	Noise Message Given	IOB Entry Bit	Tape Cleaning Bit	Control Flag	Read Opposite Recovery	Message Type	Control Unit Busy	Logout Flag
IOB Error Counts Byte 1	Interface Control Check or Channel Control Check	Overrun, Bus-Out Check, Channel Data Check, Chaining Check			———	Cleaner Control Count		
IOB Error Counts Byte 2	Write Indicator	Read Data Check Counts			User ERG Data Check			
		Error Routine ERG Data Check			Write Check Counts			

When an ending status (channel end, device end, or unit check) appears in the channel status word, the 2400/3400 Tape Series Error routine increments the 'block count' field of the data control block by the amount shown in the 'block count increment' field of the input/output block (IOB).

If an error remains uncorrected after retry attempts, or if no retries are attempted, a message (IEA000I) is written to the operator. For all error conditions except 'command reject, load point, data converter check' and 'not capable,' the logout flag of the IOB is set before entry to the I/O supervisor's Write–to–Operator routine. This is an indication to the I/O supervisor's Write–to–Operator routine to invoke the Outboard Recorder after it writes the message.

The error analysis sequence for the IBM 2400/3400 Series Magnetic Tape Units is shown in Table 18. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Table 19. More information about IBM 2400/3400 Series Magnetic Tape Units can be obtained from the following publications:

- *IBM System/360 Component Description: 2400 Series Magnetic Tape Units, 2803/2804 Tape Controls, and 2816 Switching Unit, Model 1,* GA22–6866
- *IBM System/360 Component Description: 3803/3420 Magnetic Tape Subsystems,* GA32–0020

Sense Byte 0 Meanings and Actions Taken

Byte 0 Bit 0: Command Reject
This bit is set when a command is received which the device has not been designed to execute. The error is considered permanent.

Byte 0 Bit 1: Intervention Required
This bit indicates a not–ready condition. Actions taken depend upon whether a device end status was also received:

With no device end, unit status B (sense byte 1, bit 2) is examined. If 0, the device is assumed not to exist and the error is considered permanent. If unit status B is 1, a message is given the operator. When he readies the device, the operation is attempted again.

With device end, if a Rewind Unload command was the last command executed, a successful completion is assumed and processing continues. Otherwise, the condition is ignored and the scan of sense bits is continued.

Byte 0 Bit 2: Bus–Out Check
This bit is set when even parity appears on the information bus lines from the channel to the control unit. The command is attempted again. The tape is first repositioned if the bus–out check occurred during a write operation.

Byte 0 Bit 3: Equipment Check
This bit is set when a unit fails to respond to a set read or a set write status when instructed, or becomes not ready during execution of a tape motion operation. The error is considered permanent.

Byte 0 Bit 4: Data Check
During a read or read backward operation: If the noise bit (byte 1, bit 0) is off and the blocksize is less than 12 bytes, the noise block flag in the statistics update mask is set and regular operation is resumed with the next block (except when 7–track tapes are being read by an integrated emulator, in which case the noise block is passed back to the emulator).

If the noise bit is off, but the blocksize is 12 bytes or greater, or if noise bit is on, a read recovery sequence is initiated. This sequence consists of the following steps:

1. Reposition the tape.
2. Issue the Track–in–Error command to send error information (byte 2, bit 7) to the tape control unit.
3. Re–read the tape. If error persists, post (or repost) the applicable flag bit (representing a temporary 'read' error) in temporary storage.
4. Repeat steps one through three for a total of four rereads unless a good read is obtained.
5. Perform a tape cleaner action and increment the temporary cleaner action counter in the Volume Statistics Table.

A total of ten read recovery sequences can be initiated. If the error is not cleared by that time, a read–opposite recovery sequence is initiated, provided that none of the following conditions exists:

- Data chaining is being performed.
- Data conversion mode and 7–track tape are being used.
- The original CCW count is less than the physical block size on the tape.
- "Suppress data transfer" is specified in the original CCW.

During a write or write tape mark operation: reposition the tape, issue an erase gap, issue a mode set (if 7–track), and reissue the command.

3400 write: repeat this procedure until successful or until 14 retries have been attempted. If the error persists after 14 retries, go to step 1 below.

2400 write: (2400/3420 write tapemark) repeat this procedure until successful or until 15 retries have been attempted. If the error persists after 15 retries, go to step 2 below.

Step 1. Change the failing write CCW to a "loop–write–to–read" CCW. The write CCW must not be command or data chained from or to any of the CCWs in the original failing CCW chain. After the loop–write–to–read has been completed, the failing write CCW is issued to complete the fifteenth retry.

Step 2. Provide an operator message, post completed with error condition, and exit to operating system.

During an ERG: reissue the command. Repeat this procedure until 3 retries have been attempted. If the error persists, provide an operator message, post completed with error condition, and exit to the operating system.

Byte 0 Bit 5: Overrun

This bit is set when service is requested but data cannot be transferred during a read, write, or read backward operation. Five retries are attempted. Before each retry, the tape is repositioned. *Note:* A data check during overrun suppresses the overrun indication.

Byte 0 Bit 6: Word Count Zero
This bit is set during a write operation if transfer of data is prevented before the first byte is written. This indicator is ignored.

Byte 0 Bit 7: Data Converter Check
This bit is set when an error occurs during operation of the data conversion feature. The error is considered permanent.

Other Actions Taken

Byte 1 Bit 7: Not Capable
Set on some models when density handling features are not compatible with actual tape density. No retries are attempted.

Byte 5 Bit 3: Phase Encoding ID Burst Check
Reposition to load point with a Rewind command and reissue the command. Repeat this procedure until successful, or until 14 retries have been attempted. A Loop–write–to–read command is issued and the fifteenth write retry is issued.

Byte 7 Bit 4: Data Security Erase Error
Print a message to the operator and record as a permanent error.

Unexpected Device End
Print a message to the operator and reissue the command.

Channel Data Check
This status bit is set when a channel detects a parity error in the information transferred to or from main storage during an I/O operation. Five retries are attempted. The tape is repositioned before each retry of a read or write operation.

Chaining Check
This status bit is set when channel overrun occurs during data chaining on read operations. Five retries are attempted. The tape is repositioned before each retry.

Interface Control Check
Channel Control Check
An interface control check is caused by an invalid signal on the I/O interface; channel control check is caused by any machine malfunction affecting channel controls. The 2400/3400 Series Magnetic Tape Error routine receives control only if the Channel Check Handler is in the system. Actions taken by the 2400/3400 Series Magnetic Tape Error routine are shown below. Error recovery procedure interface bytes (ERPIB) are supplied by the Channel Check Handler routine. The 2400 Channel Check ERP passes control to the 3400 Series Channel Check routine if the device is one of the IBM 3400 series.

No retries are attempted when:

- ERPIB byte 4, bit 7 is on (unconditional no–retry).
- ERPIB byte 6, bit 3 or 4 or 5 is off (retry code invalid, unit status invalid, or command address invalid).
- ERPIB are not produced.
- ERPIB byte 7, bits 0 and 1 are both on (system reset).
- ERPIB byte 4, bit 2 is on (Test I/O with no pending interruption stored a CSW).

- ERPIB byte 4, bit 3 is on (Halt I/O stored a CSW).
- ERPIB byte 4, bits 0 and 1 are both on or both off.
- ERPIB byte 4, bit 5 is off (if unit check).
- There is a unit check and an equipment check.
- The interface control check or channel control check occurred during tape repositioning (unless cc=1).

Retries are attempted when none of the above conditions exists and ERPIB termination codes and retry combinations are:

- Termination code 10, retry code 010. Write command—retry once.
- Termination code 01, retry code 011 or 101. Write or Read command—reposition and retry once. For other commands (except Set, Mode, and Transfer–in–Channel) the operation is considered complete and no recovery is attempted.

If the device is one of the 3400 series, retries are attempted when any of the following conditions exist:

- Read or Read Backward, termination code of 00, 01, or 10, and sequence code 001.
- Write, termination code 00, 01, or 10, and sequence code 001.
- Control (Read/Write), termination code 00, 01, or 10, and sequence code 001.
- Control (Rewind/Unload/Mode Set), termination code 00, 01, or 10, and sequence code 001 or 010.
- Sense, termination code 00 or 01, and sequence code 001, 010, 011, or 101.
- For all other termination and sequence code combinations, the errors are not retriable.

2495 Error Routine

The 2495 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 2495 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 2495 Tape Cartridge Reader is shown in Table 21. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 22.

More information about the IBM 2495 Tape Cartridge Reader can be obtained from the following publication: *IBM System/360 Component Description, IBM 2495 Tape Cartridge Reader,* GA27–2726

Table 21. IBM 2495 Tape Cartridge Reader Error Analysis Sequence (Module IGE0011A)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR033
2	46			Interface Control Check	ERR033
3	44			Channel Data Check	ERR033
4	42			Program Check	ERR033
5	43			Protection Check	ERR033
6	38			Unit Check	ERR033
7		0	5	Should Not Occur	ERR046
7		0	7	Should Not Occur	ERR046
8		0	3	Equipment Check	ERR046
9		0	2	Bus–Out Check	ERR046
10		0	1	Intervention Required	ERR046
11		0	6	Position Check	ERR046
12		0	4	Data Check	ERR046
13		0	0	Command Reject	ERR046
14				None of the Above Sense Bits On	ERR046
None	39			Unit Exception	ERR033
None	41			Incorrect Length	ERR033

See page 27 for an explanation of the pointers.

IBM 2495 Tape Cartridge Reader Sense Byte Meanings

Bit 0: Command Reject

This bit is set when:

- An invalid command is received and the control unit is not busy.
- A Read command is received after end–of–tape has been sensed and blank tape is encountered.
- A Control Rewind or Control Backspace command is received when the tape is in the load position.
- A Control Backspace command is received immediately following a position check caused by another Control Backspace command.

No retries are attempted.

Table 22. IBM 2495 Tape Cartridge Reader Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	Position Check	——
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	Unrelated Flag	0 Start 1 Restart
IOBFL 2	——	Sense Bit	Purge Flag	——	——	——	——	——
IOBFL 3	——	IOB Entry Flag	Read Channel Data Check Count	Bus-Out Error Count	——	Message Type	——	Logout Flag
IOB Error Counts Byte 1	Read Position Check Count				Read Data Check Count			

Bit 1: Intervention Required

This bit is set when a command is received and the control unit is in the not–ready state because:

- The stop key was depressed.
- The hopper is empty and the end–of–file key has not been depressed.
- The power is off.
- The stacker is full.
- An auto–loader malfunction occurred.

The requestor's RQE is queued so that when the tape drive is made ready the command will be reissued.

Bit 2: Bus–Out Check

This bit is set when a command with even parity appears on a bus–out operation. If the bit is set during initial selection, the operation is retried once. On the second occurrence, the error is considered permanent.

Bit 3: Equipment Check
This bit is set when:

- The leader is disconnected.
- The tape is jammed.
- The tape is not repositioned.
- A motion detection device fails.

The error is considered permanent.

Bit 4: Data Check
This bit is set when a byte with even parity is detected in the data register during a Read command. The tape is backspaced one byte and the remaining portion is read. The sequence is repeated up to ten times. The UCB extension is used as a work area for constructing a backspace CCW, a residual read CCW, and, for command chaining, a transfer–in–channel to the next user CCW. If the error remains after ten retries, it is considered permanent.

Bit 5: Should Not Occur
When this bit is set, a catastrophic error is assumed.

Bit 6: Position Check (Read Command)
This bit is set when a Read command causes the reading of tape past the stop code, beyond the end of valid data. The stop code was not detected or was ignored by the program. The tape is backspaced one byte and the data is reread. The sequence is repeated up to ten times. If the error remains, it is considered permanent. The UCB extension is used as a work area for constructing a backspace CCW, a residual read CCW, and, for command chaining, a transfer–in–channel to the next user CCW.

Bit 6: Position Check (Control)
This bit is set by indicate that a Control Backspace command has caused backspacing to the beginning of the tape. No retries are attempted.

Bit 7: Should Not Occur
When this bit is set, a catastrophic error is assumed.

2540 Error Routine

The 2540 Error routine attempts recovery from channel data checks. Read operations are retried five times; punch operations are retried once, if a bus–out check resulted from the channel data check. When the Channel Check Handler is included with a system, the 2540 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the IBM 2540 Card Read Punch is shown in Table 23. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 24. More information about the IBM 2540 Card Read Punch can be obtained from the following publications:

- *IBM System/360 Component Description and Operating Procedures: IBM 2540 Card Read Punch,* GA21–9033
- *IBM 2821 Control Unit,* GA24–3312

Table 23. IBM 2540 Card Read Punch Error Analysis Sequence (Load 1–IGE0001C or Load 2–IGE0101C)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to: Read	Punch	Control	Pointer	Load
1	45			Channel Control Check	X	X	X	ERR551	1
1	46			Interface Control Check	X	X	X	ERR551	1
2	47			Chaining Check	X	X	X	ERR546	1
3	44			Channel Data Check	X			ERR524	1
4	38			Unit Check	X	X	X	ERR525	1
5		0	5	Should Not Occur	X	X	X	ERR546	1
5		0	7	Should Not Occur	X	X	X	ERR546	1
6		0	3	Equipment Check	X	X		ERR528	1
7		0	1	Intervention Required	X	X		ERR552	2
8		0	2	Bus–Out Check	X	X		ERR534	2
9		0	4	Data Check	X			ERR536	2
10		0	0	Command Reject	X	X	X	ERR548	2
11		0	6	Unusual Command Sequence	X			ERR555	2
12	42			Program Check	X	X	X	ERR543	2
13	43			Protection Check	X	X	X	ERR543	2
14	39			Unit Exception	X			ERR543	2
15	41			Incorrect Length	X	X		ERR543	2

See page 27 for an explanation of the pointers.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

The setting of this bit indicates one of the following:

- A Read Backward or a Write command was issued to the reader.
- A Read Backward control other than NOP or a Read Feed and Stacker Select command was issued to a punch without the Punch Feed Read feature.
- A Read Backward or Control command was issued to a punch with the Punch Feed Read feature.
- An incorrect sequence of instructions was issued.
- An invalid command was received.

The error is considered permanent.

Bit 1: Intervention Required

The setting of this bit indicates a not–ready condition due to one of the following:

- Cards are not at each station (not end–of–file for the reader).
- The stacker is full.
- The hopper is empty (not end–of–file for the reader).

- The Stop key was depressed.
- The chipbox is full or has been removed.
- There is a card jam.

A message is given the operator, who must take action. Upon correction of the condition, the interrupted operation is repeated.

Bit 2: Bus–Out Check

This bit is set when a parity error has occurred on bus–out on a command or data byte (bus–out is a data transfer from the processing unit to the control unit). When this error is detected, no punching occurs. The operation is retried once and if the error occurs a second time it is considered to be permanent.

Bit 3: Equipment Check

This bit is set after one of the following:

- A hole count error
- A buffer parity error
- A translate check
- An address check

Table 24. IBM 2540 Card Read Punch Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	Unusual Command Sequence	——
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL 2	——	——	——	——	——	——	——	QSAM Access Method
IOBFL 3	Indicator 1	Entry Flag	Read Error Count	Bus-Out Error Count	Punch Relay	Message Type	QSAM Count	Logout Flag
Error Counts IOBECT Byte 2	Accept Unusual Command Sequence	——	——	——	Data Check, Channel Data Check, Equipment Check Count			Channel Control Check, Interface Control Check

The error applies to the card that preceded the one from which data was transmitted; it is considered permanent. If the error occurred during the processing of a Read command, the operation is retried five times. If the error occurred during a QSAM operation, one retry is attempted.

Bit 4: Data Check
This bit is set when an invalid card code is detected. The operation is retried five times. On the sixth occurrence, it is denoted as a permanent error.

Bit 5: Should Not Occur

Bit 6: Unusual Command Sequence
This bit is set when there are two consecutive reads without an intervening feed. The error is considered permanent.

Bit 7: Should Not Occur

Table 25. IBM 2671 Paper Tape Reader Error Analysis Sequence (Module IGE0002[1])

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERZERIB
1	46			Interface Control Check	ERZERIB
2	47			Chaining Check	ERR611
3	38			Unit Check	ERR601
4		0	5	Should Not Occur	ERR611
5		0	6	Should Not Occur	ERR611
6		0	7	Should Not Occur	ERR611
7		0	3	Equipment Check	ERR611
8		0	1	Intervention Required	ERR608
9		0	2	Bus-Out Check	ERR609
1	0	0	4	Data Check	ERR611
11		0	0	Command Reject	ERR612
12	44			Channel Data Check	ERR625
13	42			Program Check	ERR618
14	43			Protection Check	ERR618
15	39			Unit Exception	ERR619
16	41			Incorrect Length	ERR619

See page 27 for an explanation of the pointers.

[1]The eighth character in the module name is not printable, but can be represented by X'C0'.

2671 Error Routine

The 2671 Error routine treats all channel errors as permanent. Because the IBM 2671 Paper Tape Reader cannot be backspaced or repositioned under program control, all unit check errors except a bus–out check are considered permanent. The bus–out check is retried once and if not corrected, is considered permanent.

The error analysis sequence for the IBM 2671 Paper Tape Reader is shown in Table 25. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Table 26. More information about the IBM 2671 Paper Tape Reader can be obtained from the following publication: *IBM 2671 Paper Tape Reader; IBM 2822 Paper Tape Reader Control,* GA24–3388

Table 26. IBM 2671 Paper Tape Reader Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	——	——	——
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	——	——	Exceptional Condition	——	0 Start 1 Restart
IOBFL 3	——	Equipment Check Count		Bus-Out Error Count	——	Message Type	——	Logout Flag

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set when a Read Backward or a Write command is received at the tape reader, or when valid commands have invalid modifier bits. A parity error on the command prevents this condition from being detected. This bit also indicates a permanent error.

Bit 1: Intervention Required

This bit is set when the device is "not ready." A Paper Tape Reader becomes ready when:

- Power is on.
- The tape is loaded.
- The Start key is pressed.

The Paper Tape Reader becomes not ready immediately when:

- The Stop key is pressed while no read operation is in progress.
- The Load key is pressed.
- The Power–On and Reset keys are pressed.

The Paper Tape Reader becomes not ready after a read operation when:

- There is an overstep condition (the tape did not stop on one character).
- Tape jams in the take–up stacker.
- The end of the tape is detected at the reading station but the end–of–file light is off.
- The Stop key has been depressed during the read operation.

When the device is made ready, a device end interruption occurs.

Bit 2: Bus–Out Check
This bit is set when a parity error is detected on a command byte. One retry is attempted.

Bit 3: Equipment Check
This bit indicates that a timeout has been detected in the tape reader since the last data byte was sensed at the tape read station. This timeout of approximately one second can be caused by:

- A photocell failure
- A tape drive motor failure
- An unusual tape creeping condition
- A length of unpunched tape
- Tape jamming in the optional stackers
- A light projection system failure
- A permanent error

Bit 4: Data Check
This bit is set when an invalid character is read; it indicates a permanent error.

Bits 5–7: Should Not Occur
If any of these bits are set, a catastrophic error is assumed. The logout flag is set in the IOB, a permanent error is signaled to the error EXCP routine, and control is returned via SVC 15.

3211 Error Routine

The 3211 Error routine attempts recovery from channel data checks only if they occur with bus–out checks. A channel data check occurring alone is not considered an error.

When the Channel Check Handler is included with a system, the 3211 Error routine also attempts recovery from channel control checks and interface control checks.

In addition to handling the normal functions of an error recovery procedure, the 3211 ERP compiles data for device dependent OBR records. These records are then recorded on SYS1.LOGREC by the recording module IGE0625F. The following information will be recorded:

1. FCB Parity Check—Carriage Control Address Register (CCAR) and the FCBID in the UCB
2. PLB Parity Check—Diagnostic Check Read Data and the first 10 positions of the PLB
3. UCS Parity Check—Contents of UCS buffer and the UCSID in the UCB

The error recovery procedure for the 3211 Printer is shown in Table 27. The meanings of sense bits, IOB flags and IOB error counts are shown in Table 28.

More information can be obtained from the following publication: *IBM 3211 Printer and 3811 Control Unit Component Description,* GA24–3543.

Table 27. IBM 3211 Printer Error Analysis Sequence (Module IGE0000F)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR031
1	46			Interface Control Check	ERR031
2	47			Chaining Check	ERR070
3	38			Unit Check	ERR040
4		1	5	Command Suppress	ERR050A
5		0	3	Equipment Check	ERR051
6		0	2	Bus–Out Check	ERR052
7		0	4	Data Check	ERR055E
8		0	5	Buffer Parity Check	ERR053
9		0	0	Command Reject	ERR071
10		0	6	Load Check	ERR070
11		0	1	Intervention Required	ERR055
12		0	7	Channel 9	ERR064A
13	44			Channel Data Check	ERR061
14	42			Program Check	ERR062
15	43			Protection Check	ERR062
16	41			Incorrect Length	ERR063
17	39			Unit Exception	ERR064

See page 27 for an explanation of pointers.

Table 28. IBM 3211 Printer Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	Buffer Parity Error	Load Check	Channel 9
Sense Byte 1	Command Retry	Print Check	Print Quality	Line Position	Forms Check	Command Suppress	Mechanical Motion	——
Sense Byte 2	Carriage Fail to Move	Carriage Sequence Check	Carriage Stop Check	Platen Fail to Advance	Platen Fail to Retract	Forms Jam	Ribbon Motion	Train Overload
Sense Byte 3	UCSB Parity	PLB Parity	FCB Parity	Coil Protect	Hammer Fire Check	Field Engineering	UCSAR Sync Check	Sep Sync Check
IOBFL1	00 - No Chaining 01 - Command Chaining 10 - Data Chaining 11 - Both		Error Routine in Control	——	——	Exceptional Condition	——	0 - Start 1 - Restart
IOBFL3	MCS Flag	Entry Flag	Command Suppress Error Count	Bus-Out Error Count	Buffer Flag	Message Type	TPER Flag	Logout Flag
IOBECT	FCB Count	——	——	——	FCB Count	UCS Count	Channel Error Count	——
IOBECT+1	——	——	——	——	——	MCS Count	MCS Count	MCS Count

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set during Initial Selection when a command other than those defined for the printer is given. The error is considered permanent.

Bit 1: Intervention Required

This bit indicates a not–ready condition due to one of the following:

- Platen failure
- Ribbon motion or ribbon skew
- Jammed or torn forms
- Carriage Stop–Release Off
- Interlock condition

An Intervention Required message is issued for the operator; when the condition is corrected the last operation is repeated. If this occurs with channel 9 (bit 7) the message is given to the operator, but the error is handled as a channel 9 condition. The operator has the option of forcing a permanent error by pressing the Cancel button on the 3211.

Bit 2: Bus–Out Check
This results when the control unit receives a data byte or a command byte with invalid parity. The operation is retried once in a non–multiple console support system and 5 times in an MCS system.

Bit 3: Equipment Check
This bit indicates a malfunction that affects the operation in process. The specific condition will be indicated by a bit in byte 1.

Bit 4: Data Check
This bit signifies that there is an incomparable code in the UCSB or in the FCB. An Intervention Required message will be written to the operator and when the condition is corrected the previous operation will be retried. The operator will have the option of causing a permanent error by pressing the Cancel button on the 3211.

Bit 5: Buffer Parity Check
This bit indicates invalid parity in the UCSB or FCB. The error is considered permanent.

Bit 6: Load Check
This bit is given for a load UCSB or load FCB command when the load was invalid. The error is considered permanent.

Bit 7: A channel 9 code was sensed in the FCB during a carriage motion.

Sense Byte 1 Meanings

Bit 0: Command Retry—This indicates a parity error in the print line buffer. The error is considered permanent. In a system with MCS the error is retried 5 times before it is considered permanent.

Bit 1: Print Check—Indicates the line in process may contain one or more print errors.

Bit 2: Print Quality—Indicates a machine failure that could affect print quality.

Bit 3: Line Position—Indicates that the previous line or next line to be printed may be in the wrong place.

The last three conditions will result in an Intervention Required message to the operator. When the condition is corrected the last operation is repeated. The operator will have the option to cause a permanent error by pressing the Cancel button on the 3211.

Bit 6: Mechanical Motion—Signifies that the command in process cannot be completed and the results are unpredictable due to hardware failure. The error is considered permanent.

If bit 3 of byte 0 is set and no bits in byte 1 are set, a sync check or train overload exists. These errors are considered permanent.

3505/3525 Error Routine

The 3505/3525 Error routine attempts recovery from I/O errors that cause an interruption. The condition causing the interruption is indicated in the channel status word (CSW). If the unit check (bit 38) is present in the CSW, a sense command is performed to obtain further information about the error interrupt. The status byte and sense byte 0 provide information and reasons for a unit check detected in the last operation. Sense byte 1 defines the ERP actions required for the unit check.

The error analysis sequence for the IBM 3505 Card Reader and the IBM 3525 Card Punch with Read and Print feature is shown in Table 29. The meanings of the sense bits, IOB flags, and IOB error counts are shown in Table 30. More information about the IBM 3505/3525 can be obtained from *IBM 3505 Card Read and IBM 3525 Card Punch Subsystem,* GA21–9124.

Table 29. IBM 3505/3525 Error Analysis Sequence (Module IGE0001A)

Priority	Status Bit	Sense Byte	Sense Bit	Condition	Applicable to: Read	Punch	Printer	Control	Pointer
1	45			Channel Control Check	X	X	X	X	ERR001
2	46			Interface Control Check	X	X	X	X	ERR011
3	44			Channel Data Check		X	X	X	ERR012
4	32			Should Not Occur	X	X	X	X	EXIT12
5	33			Should Not Occur	X	X	X	X	EXIT12
6	34			Should Not Occur	X	X	X	X	EXIT12
7	38			Unit Check	X	X	X	X	SENSE0
8		0	5	Should Not Occur	X	X	X	X	EXIT12
9		0	7	Permanent Error (Key)	X	X	X	X	EXIT22
10		0	3	Equipment Check	X	X	X		ERR002
11		0	6	Abnormal Format Reset	X				SENSE1
12		0	1	Intervention Required	X	X	X	X	ERR003
13		0	2	Bus–Out Check	X	X	X	X	SENSE1
14		0	4	Data Check	X				SENSE1
15		0	0	Command Reject	X	X	X	X	SENSE1
16	47			Chaining Check	X				EXIT12
17	42			Program Check	X	X	X		ERR004
18	43			Protection Check	X	X	X	X	ERR004
19	39			Unit Exception	X				ERR004
20	41			Incorrect Length	X	X			ERR004

See page 27 for an explanation of the pointers.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject

This bit is set on for invalid commands such as read backwards and for commands for uninstalled features. The error is considered a permanent condition.

Bit 1: Intervention Required

This bit is set on for a hopper misfeed, hopper jam, cornering station misfeed, Read station check, transport jam, and normal user occurrences such as hopper empty, joggler open, stacker full, stop key depressed, or covers open.

Recovery from this error is possible as defined by recovery indicators on the machine.

Table 30. IBM 3505/3525 Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	Intervention Required	Bus-Out Check	Equipment Check	Data Check	—	Abnormal Format Reset	Permanent Error Key
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	—	—	Exceptional Condition	—	0 Start 1 Restart
IOBFL 2	—	—	—	—	—	—	—	QSAM Access Method
IOBFL 3	Auto. Retry Flag Command	Entry Flag	Channel Control Check	Interface Control Check	Punch Retry	Message Type	QSAM Count	Logout Flag
Error Counts IOBECT Byte 2		—	—	—				Channel Control Check, Interface Control Check

Bit 2: Bus–Out Check
This results in a bad parity on bus–out during initial selection. The error is considered a permanent condition only after the second try.

Bit 3: Equipment Check
This bit is turned on for errors due to data compare check, emitter check, and CU internal parity check detected between IS and CE.

A recovery can be made as defined by the recovery indicators on the machine.

Bit 4: Data Check
This results when an invalid EBCDIC card code is found when Data Mode 1 is read. Recovery can be made as defined by recovery indicators on the machine.

Bit 5: Not Used

Bit 6: Abnormal Format Reset

Bit 7: Permanent Error (Error Bypass Key)
This results when the operator presses the Error Bypass Key rather than performing recovery assistance. The error is considered a permanent condition.

Sense Byte 1 Meanings

Bit 0: Permanent Error
This bit directs the ERP to post a permanent error condition and proceed with appropriate disposition of the condition. It is set only with sense byte 0, bit 0 or bit 1.

Bit 1: Automatic Retry
This results in retrying the failing CCW once. If successful, normal program execution continues. If unsuccessful, a permanent error condition is posted and the procedure is continued with the appropriate disposition of the condition. This occurs only with sense byte 0, bits 2 and 3.

Bit 2: Motion Malfunction
This bit is turned on with Intervention Required when the cause is other than a normal user occurrence. It is set only with sense byte 0, bit 1. This bit is not required by the ERP to effect recovery but is included to facilitate the measurement of SSIs.

Bit 3: Retry After Intervention Required Complete
After a normal not–ready to ready Device End, the failing CCW is reissued. This occurs only with sense byte 0, bits 1, 3, 4, and 6.

Bits 4–7: Not Used.

Sense Byte 2 Meanings

This sense byte is for diagnostic purposes only. It defines the first error in the 3505 or 3525 and also serves as a pointer to the appropriate maintenance documentation.

Sense Byte 3 Meanings

This sense byte is for diagnostic purposes only. It serves to further resolve a limited group of errors.

Channel Checks

Recovery from channel errors (channel control check, interface control check, and channel data check) is as follows:

If Selective Reset or Interface Disconnect was given between Initial Selection and Channel End, reissue the command to the 3505 or 3525.

5450 Error Routine

The 5450 Error routine attempts recovery from channel data checks. When the Channel Check Handler is included with a system, the 5450 Error routine also examines the error recovery procedure interface block to determine whether it should attempt recovery from channel control checks and interface control checks.

The error analysis sequence for the 5450 Integrated Console for Model 85 is shown in Table 31. The meanings of sense bits, IOB flags, and IOB error counts are shown in Table 32.

Table 31. IBM 5450 Integrated Console for Model 85 Error Analysis Sequence (Module IGE0010D)

Priority	Status	Sense Byte	Sense Bit	Condition	Pointer
1	45			Channel Control Check	ERR450
2	46			Interface Control Check	ERR450
3	44			Channel Data Check	ERR450
4	38			Unit Check	ERR600
5		0	1	Should Not Occur	ERR600
5		0	5	Should Not Occur	ERR600
6		0	2	Bus–Out Check	ERR600
7		0	4	Data Check	ERR605
8		0	7	Buffer Address Parity Check	ERR600
9		0	6	Invalid Buffer Address	ERR600
10		0	0	Command Reject	ERR600
11		0	3	Equipment Check	ERR600
12	42			Program Check	ERR618
13	43			Protection Check	ERR618
14	39			Unit Exception	ERR618
15	41			Incorrect Length	ERR618

See page 27 for an explanation of the pointers.

Sense Byte 0 Meanings and Actions Taken

Bit 0: Command Reject
This bit is set when there is an invalid modifier bit in a command, or an invalid command sequence. One retry is attempted. If the retry is unsuccessful, the error is considered permanent.

Bit 1: Should Not Occur
When this bit is set, a catastrophic error is assumed.

Bit 2: Bus–Out Check
This bit is set when a parity error is detected on a command or data byte during bus–out. One retry is attempted. If the retry is unsuccessful, the error is considered permanent.

Bit 3: Equipment Check
This bit is set when an error is detected during a keyboard operation. The error is considered permanent.

Bit 4: Data Check
This bit is set when a buffer parity error is detected. One retry is attempted. If the retry is unsuccessful, the error is considered permanent.

Table 32. IBM 5450 Integrated Console for Model 85 Sense Bits, IOB Flags, and IOB Error Counts

	Bit 0	Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Sense Byte 0	Command Reject	———	Bus-Out Check	Equipment Check	Data Check	———	Invalid Buffer Address	Buffer Address Parity Check
IOBFL 1	00 No Chaining 01 Command Chaining 10 Data Chaining 11 Command and Data Chaining		Error Routine in Control	———	———	Exceptional Condition	———	0 Start 1 Restart
IOBFL 2	———	Sense Flag	Purge Flag	———	———	———	———	———
IOBFL 3	Command Reject Retry	Bus-Out Error Retry	Equipment Check Retry	Data Check Retry	Buffer Address Parity Check Retry	Invalid Buffer Address Retry	———	Logout Flag

Bit 5: Should Not Occur
When this bit is set, a catastrophic error is assumed.

Bit 6: Invalid Buffer Address
This bit is set upon detection of a buffer or cursor address having valid parity but lying outside of the valid buffer xy address range. One retry is attempted. If the retry is unsuccessful, the error is considered permanent.

Bit 7: Buffer Address Parity Check
This bit is set when there is a parity error on a buffer or cursor address. One retry is attempted. If the retry is unsuccessful, the error is considered permanent.

Writing Error Recovery Messages to the Operator

When an error is uncorrectable or when a condition exists that could be changed by operator action, an I/O error routine invokes the I/O supervisor's Write–to–Operator routine, which composes a message to be written on the console output device (Diagram 12). The Write–to–Operator routine handles three messages: Uncorrectable Input/Output Error (IEA000I), Inoperative Path (IEA001I), and Intervention Required (IEA000A). It uses a Write–to–Operator macro instruction to cause them to be written on the console output device.

The I/O supervisor Write–to–Operator routine is contained in five modules. The first (IGE0025C) determines which modules to invoke and produces the Intervention Required message. The second (IGE0125C) determines which message is to be written and invokes either the third (IGE0225C) or fifth (IGE0425C) load to produce the Uncorrectable Input/Output Error message. Load four (IGE0325C) produces Start I/O condition code 3 error messages. The full text of each message is in the "I/O Supervisor Messages" part of Section 7.

Recording Error Data

Two types of data are produced to document I/O device failures: error statistics and environmental data. Error statistics are counts of the number of times errors have occurred on individual I/O devices. Environmental data documents the time and circumstances of the errors. Both types of data are recorded in the SYS1.LOGREC data set, where they can be retrieved in an edited format by means of the IFCEREP0 Utility program, described in the publication *OS Utilities*, GC28-6586. Operations discussed in the following text are:

- Recording outboard records
- Recording inboard records
- Recording miscellaneous data records
- Interfacing with IFBSTAT (SVC 76)
- Writing environment recording error messages to the operator

The routines involved in the above operations are shown in Figure 11.

Recording Outboard Records

The Outboard Recording routine (OBR) is called through a special XCTL entry. The OBR XCTL load name is 025F. The XCTL routine loads the requested segment of the Outboard Recording routine into the error transient area. The address of the request element (RQE) is passed in register 1.

Upon completion of its assigned functions, OBR issues SVC 15 to free the request element and returns control the the supervisor via SVC 3. When an EOD command is entered for terminals using TCAM, OBR passes control to the error recovery procedure until all internal counters are recorded, before returning control to the supervisor.

As indicated in Figure 11, the Outboard Recording routine receives control for one of the following operations:

- Overflow recording—A statistics table entry has reached maximum value.
- Permanent error recording—A permanent I/O device failure has occurred.
- TCAM statistics recording—One of TCAM's two counters has reached its maximum value, a terminal error has occurred, or an End-of-Day (EOD) command has been entered.

Overflow Recording

Counts of the number of times I/O devices have failed are not maintained directly on the SYS1.LOGREC data set. Instead, intermediate counters are used. The intermediate counters are contained in a main-storage table called the device statistics table. There is one entry in the device statistics table for every I/O device.

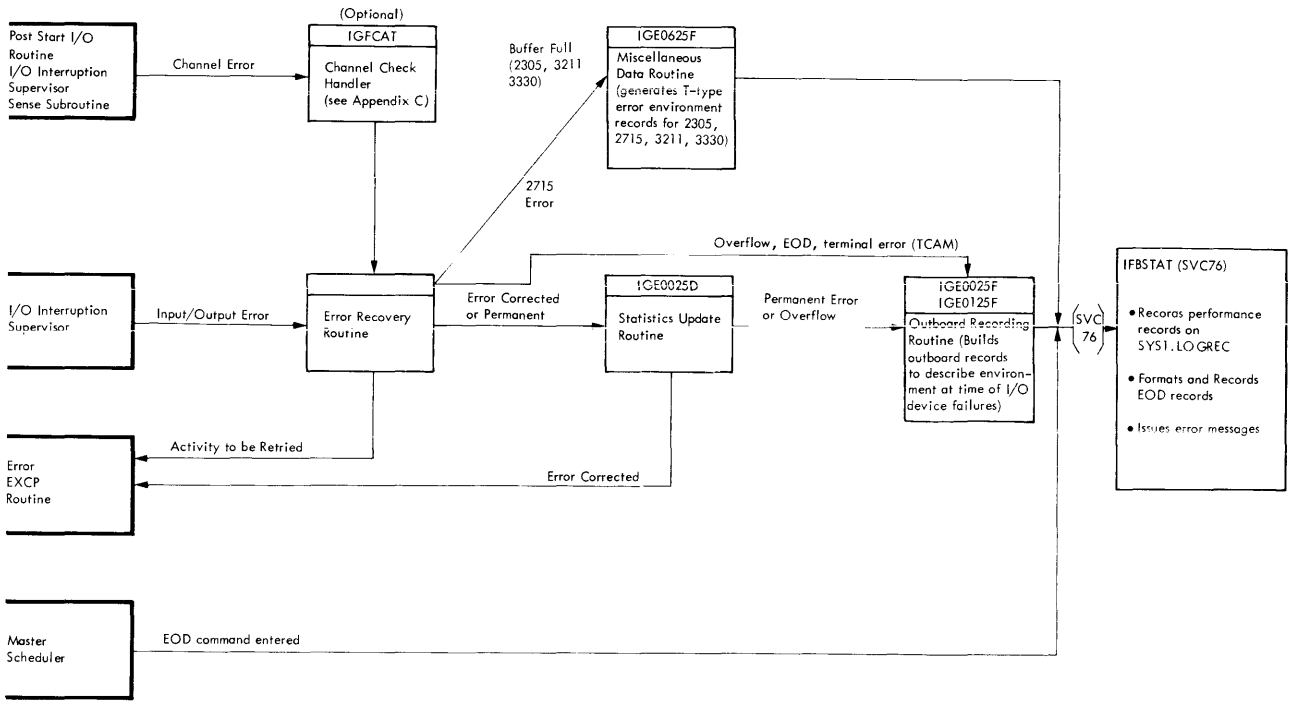


Figure 11. Recording Error Data

When an I/O error routine finds that a unit check condition has occurred, it stores the sense bit settings it obtains in the device statistics table entry for the failing device. After it has corrected the error or has found the error to be uncorrectable, the I/O error routine invokes the Statistics Update routine, which examines the sense bit settings and increments the appropriate counters in the device statistics table.

When any counter in the device statistics table reaches it maximum value of 15 the Statistics Update routine invokes the Outboard Recording routine (OBR). The Outboard Recording routine must first determine what type of record it is to prepare:

- Short OBR record—Temporary failure statistics (bit 5 of UCBFL5 field in UCB is set to 0). Refer to Figure 39 for the format of a Short OBR record.
- Long OBR record—Temporary failure statistics (bit 5 of UCBFL5 field in UCB is set to 1). Refer to Figure 38 for the format of a Long OBR record.

When the Outboard Recording routine has prepared the appropriate record, it issues SVC 76 to write the record on the SYS1.LOGREC data set.

Permanent Error Recording

Every time there is a permanent I/O device failure, environmental data is collected, placed into a record called an outboard record, and written onto the SYS1.LOGREC data set. For permanent errors, the Statistics Update routine gives control to the

Outboard Recording routine after error counters have been updated. The Outboard Recording routine collects the data it needs, creates a long OBR record (see Figure 38), and issues SVC 76 to write the record on the SYS1.LOGREC data set.

TCAM Statistics Recording

For each terminal in a system, TCAM provides two 2–byte counters. The first counter keeps track of the number of SIO commands issued to the terminal. The second counter provides a count of all failure incidents at the terminal in one byte, and a count of selective failure incidents in the other. Both counters are updated by the terminal error recovery procedure and are reset to zero after they have been recorded by the Outboard Recording routine.

There are three types of recordings:

- Normal: Error information, including the contents of the two counters, is recorded for all non–correctable incidents. The long OBR record (see Figure 38) is used.
- Intensive: All error incidents are recorded whether or not they are correctable. Intensive mode operation must be specifically requested for a particular terminal through the operator's console. An additional facility of the selective intensive mode enables records to be created when specific errors occur. For example, a record can be created each time a data check occurs on a particular terminal.
- Counter Overflow/End–of–Day: When either of the two previously described counters is about to overflow, or when there is an End–of–Day request, a Long OBR record is prepared and written on the SYS1.LOGREC data set. (Since information such as first or failing CCW, CSW, and sense information is not meaningful in this situation, it is not recorded.)

Record Inboard Records

On systems with a Channel Check Handler routine, inboard records are created for channel failures. The creation of these records takes place before error recovery routines are entered. The Outboard Recording routine writes the inboard records created by the Channel Check Handler onto the SYS1.LOGREC data set via SVC 76.

The Channel Check Handler requires input describing when and under what conditions the channel failure occurred. Therefore, there is a complex interface between the Channel Check Handler and other I/O supervisor routines. The interface is shown in Diagram 15.

Detailed information on the Channel Check Handler is contained in Appendix C.

Recording Miscellaneous Data Records

The Miscellaneous Data Recording routine collects and formats buffered data stored by device dependent error recovery procedures for IBM Models 2305, 3211, and 3330.

The location of the buffered data depends on the type of device, so the Miscellaneous Data Recorder must first check the UCB to determine the device type. It then calculates an offset from the UCB to locate the buffer.

Once it has located the buffer, the routine generates a Miscellaneous Data Record (see Figure 40). The record is then written on the SYS1.LOGREC data set via SVC 76.

The Miscellaneous Data Recording routine also formats and records IBM Model 2715 error data that is not stored in a buffer.

The Miscellaneous Data Recording routine receives control from a device dependent error recovery procedure via an XCTL macro instruction. The address of the request element (RQE) is register 1.

Upon completion of its assigned functions, the routine checks a return indicator which it extracted from the third and fourth bytes of the buffer or from the 2715 interface. If the indicator contains a nonzero value, the address of the RQE is place in reigster 1 and control is passed to a special XCTL interface location. From there, control is returned to the caller. If the indicator equals 0, the routine issues SVC 15 to free the RQE and returns to the supervisor via SVC 3.

Using the IFBSTAT Interface (SVC 76)

Both the Outboard Recording routine and the Miscellaneous Data Recording routine pass the following information to the IFBSTAT routine:

- Address of the record in register 1
- Twos complement of the record length in register 0

When IFBSTAT receives control, it checks the contents of register 0. If the value is negative, it performs a recording function. If the value is positive, an EOD (End–of–Day) record is to be formatted and written on the SYS1.LOGREC data set. Further information on SVC 76 is contained in Appendix A.

Writing Environment Recording Error Messages to the Operator

When an I/O error occurs during activity on the SYS1.LOGREC data set, when the SYS1.LOGREC data set is almost full, or when there is not enough room on the SYS1.LOGREC data set for another record, the fourth load module of IFBSTAT (SVC 76) is invoked to write a message to the operator (Diagram 15).

Operation Diagrams

This section contains diagrams that illustrate how the I/O supervisor performs I/O operations, with particular emphasis on where it obtains data and how it acts upon that data.

In the program listings, the symbolic names which are shown in individual data area fields are equated to the offset, in bytes, from the beginning of a table to the field. Access is gained to a specific field by using an instruction in which the beginning address of the table (usually contained in a register) is the base address, and the symbolic field name represents the displacement.

There are places where the symbolic field names will differ from names used in other publications. Names used here were taken from I/O supervisor listings and, where differences exist, a non–I/O supervisor program may refer to the field by the other name. (To resolve name differences, compare offsets; if the offsets match, the names represent the same field.)

Usage of the data area fields can be traced in the I/O supervisor listings by first locating the symbolic field names in the cross–reference table at the back of the listings and then noting where the names are used.

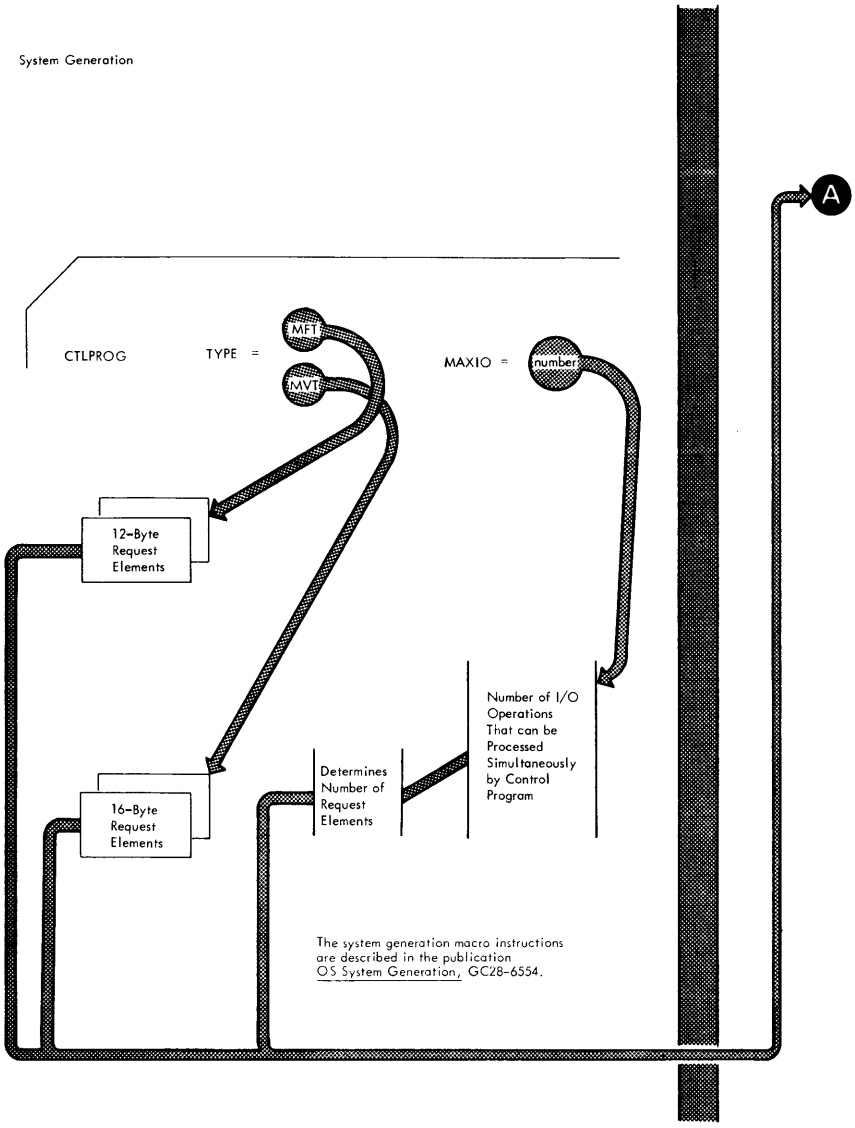
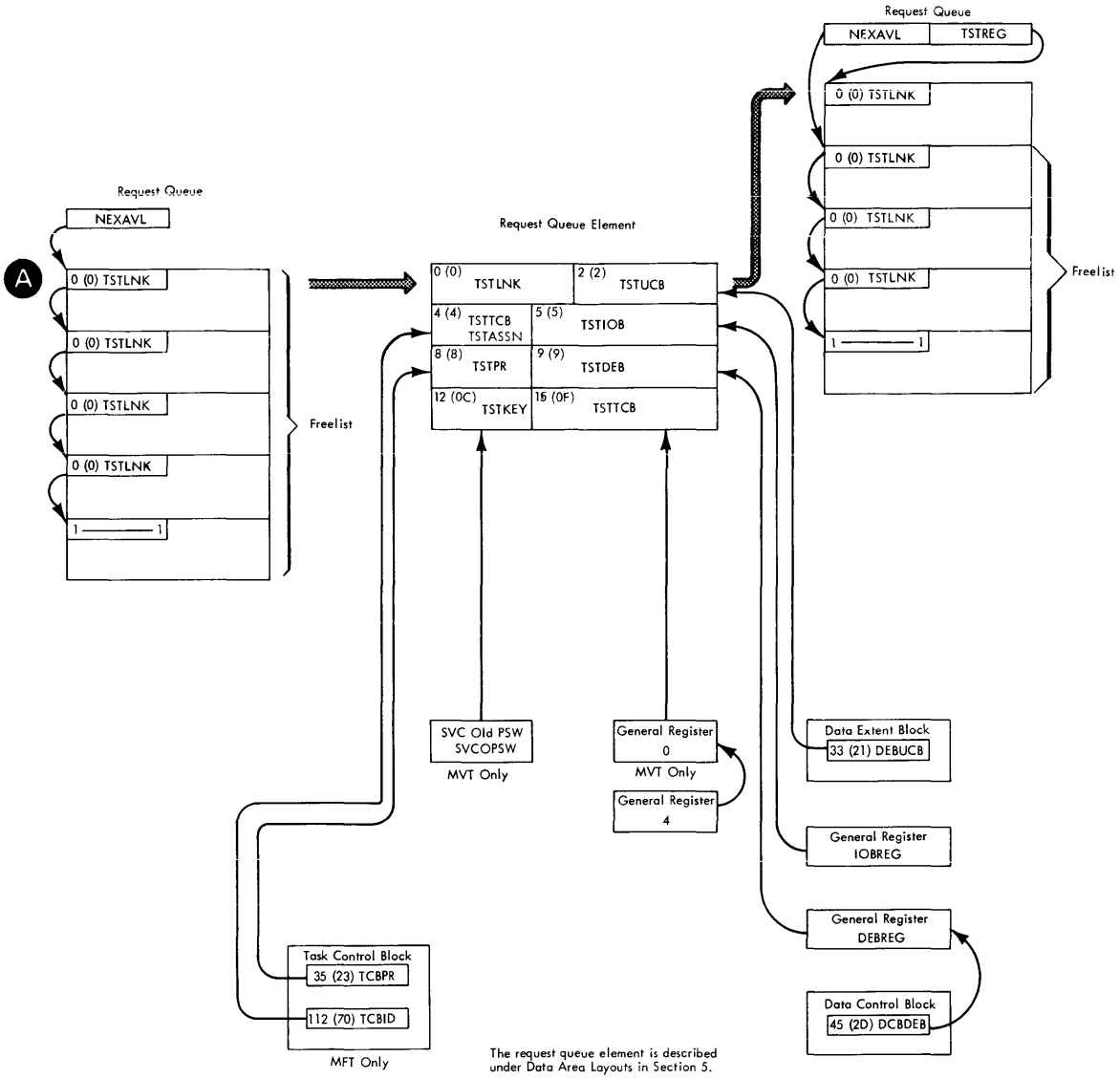


Diagram 1. Creating a Request Queue Element


Request Queue
NEXAVL
TSTREG
0 (0) TSTLNK
0 (0) TSTLNK
0 (0) TSTLNK
0 (0) TSTLNK
1 1
Freelist
Request Queue
NEXAVL
A
0 (0) TSTLNK
0 (0) TSTLNK
0 (0) TSTLNK
0 (0) TSTLNK
1 1
Freelist
Request Queue Element
0 (0) TSTLNK
2 (2) TSTUCB
4 (4) TSTTCB TSTASSN
5 (5) TSTIOB
8 (8) TSTPR
9 (9) TSTDEB
12 (0C) TSTKEY
16 (0F) TSTTCB
SVC Old PSW SVCOPSW
MVT Only
General Register 0
MVT Only
General Register 4
Data Extent Block
33 (21) DEBUCB
General Register IOBREG
General Register DEBREG
Data Control Block
45 (2D) DCBDEB
Task Control Block
35 (23) TCBPR
112 (70) TCBID
MFT Only
The request queue element is described under Data Area Layouts in Section 5.
For additional information, see:
• Chart AB, Get Request Element Routine.
The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes this Diagram.

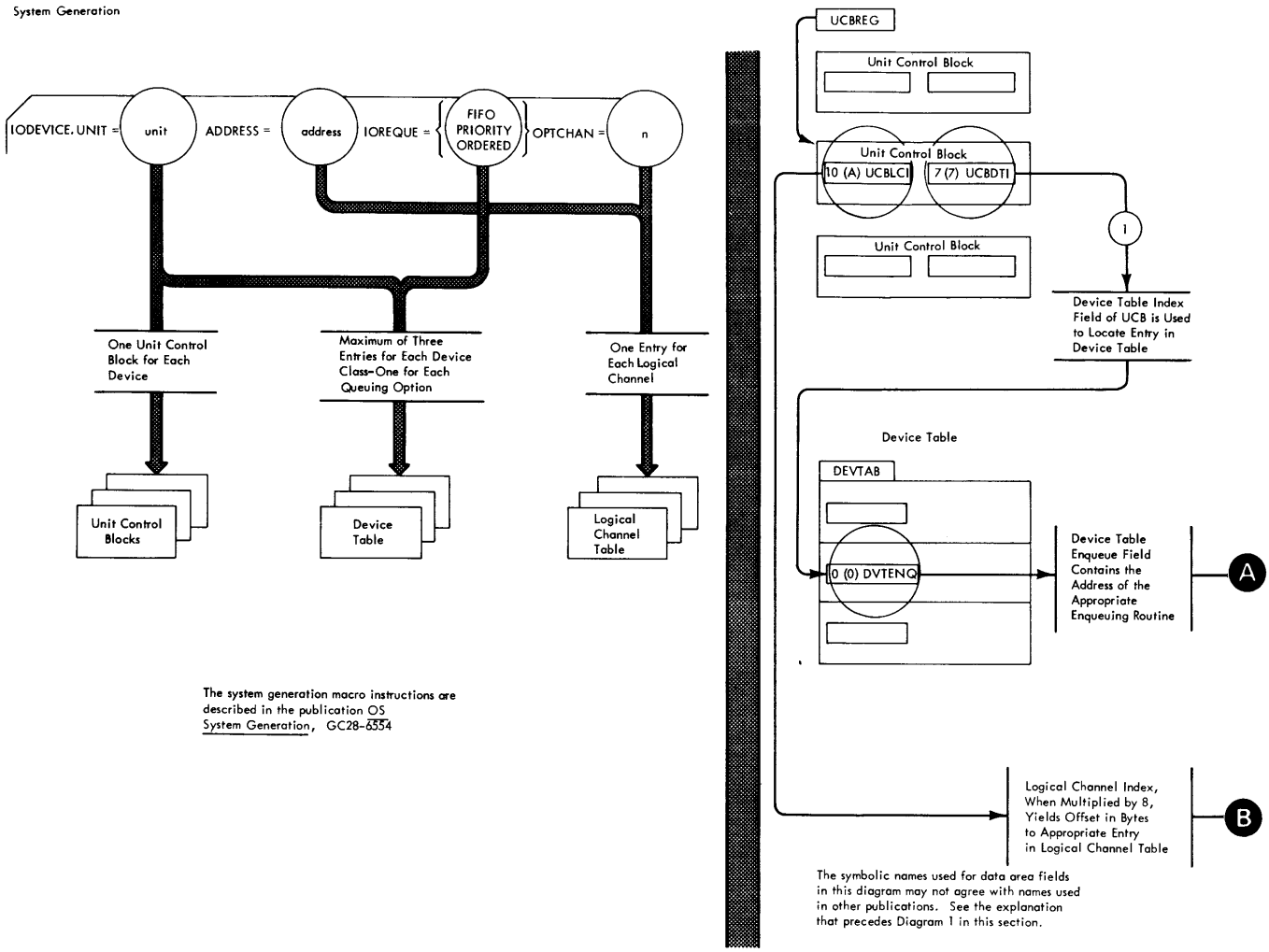
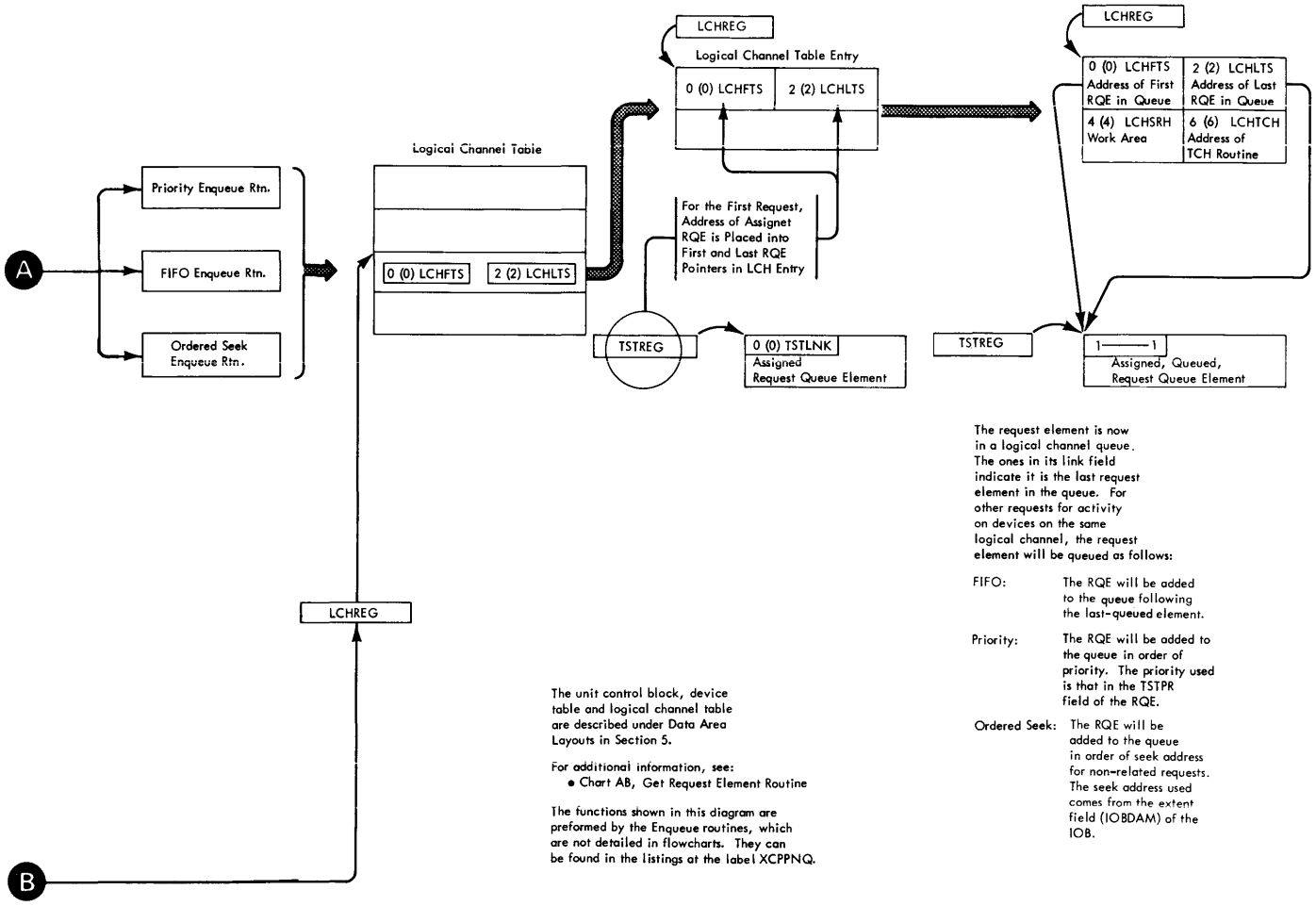


Diagram 2. Queuing a Request Queue Element



The request element is now in a logical channel queue. The ones in its link field indicate it is the last request element in the queue. For other requests for activity on devices on the same logical channel, the request element will be queued as follows:

FIFO: The RQE will be added to the queue following the last-queued element.

Priority: The RQE will be added to the queue in order of priority. The priority used is that in the TSTPR field of the RQE.

Ordered Seek: The RQE will be added to the queue in order of seek address for non-related requests. The seek address used comes from the extent field (IOBDAM) of the IOB.

The unit control block, device table and logical channel table are described under Data Area Layouts in Section 5.

For additional information, see:
- Chart AB, Get Request Element Routine

The functions shown in this diagram are preformed by the Enqueue routines, which are not detailed in flowcharts. They can be found in the listings at the label XCPPNQ.

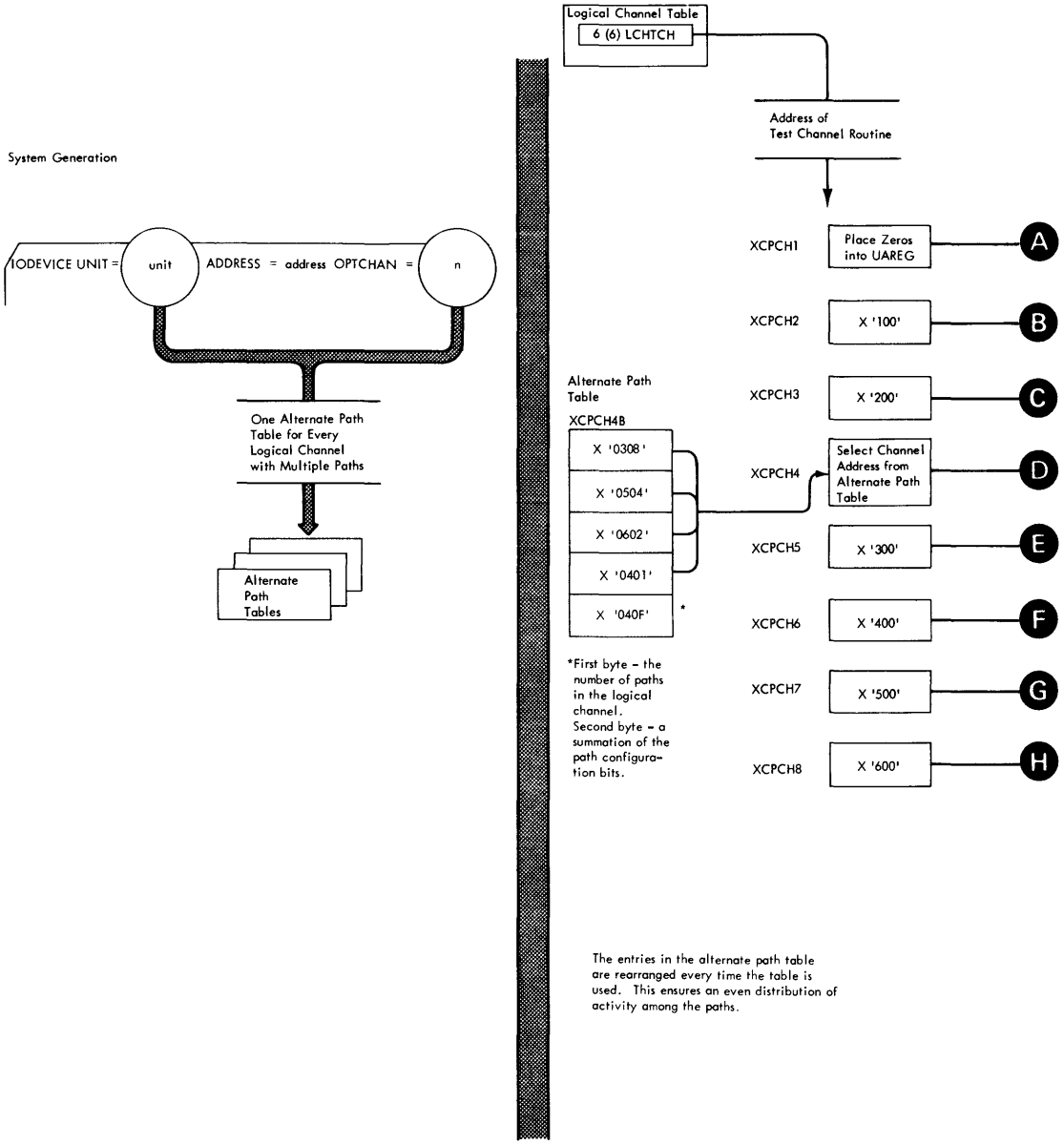
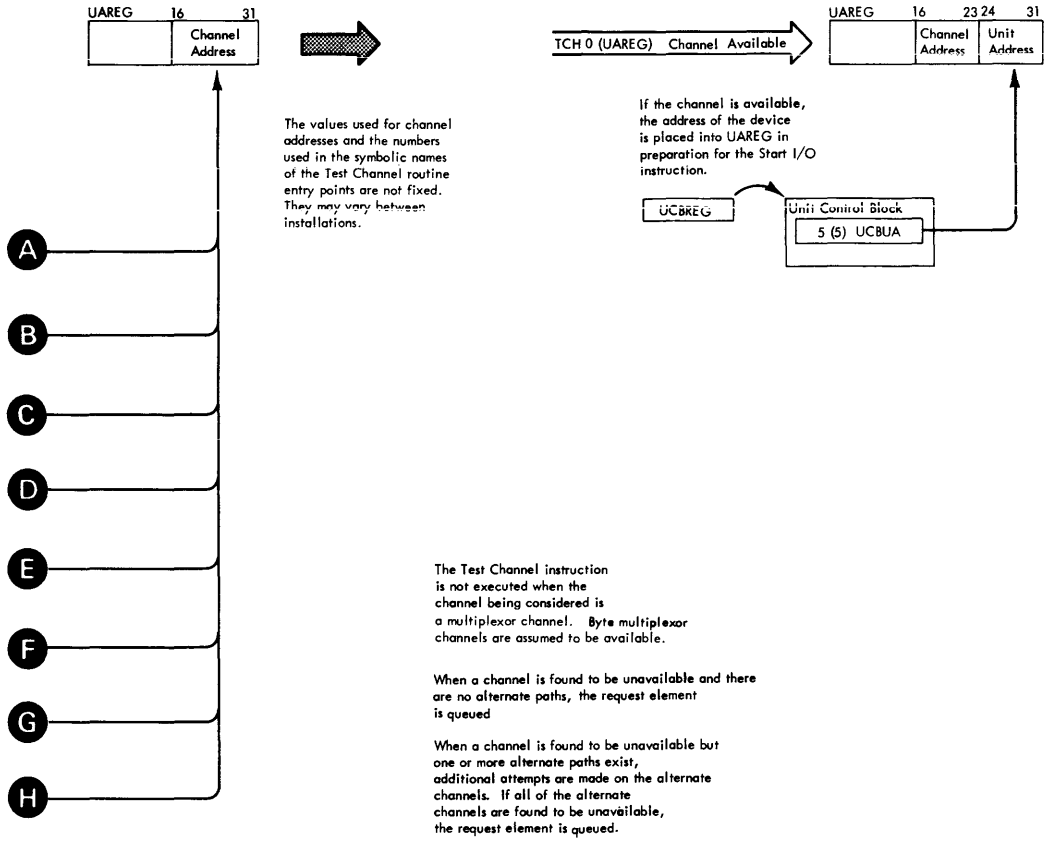


Diagram 3. Testing Channel Availability



The values used for channel addresses and the numbers used in the symbolic names of the Test Channel routine entry points are not fixed. They may vary between installations.

If the channel is available, the address of the device is placed into UAREG in preparation for the Start I/O instruction.

The Test Channel instruction is not executed when the channel being considered is a multiplexor channel. Byte multiplexor channels are assumed to be available.

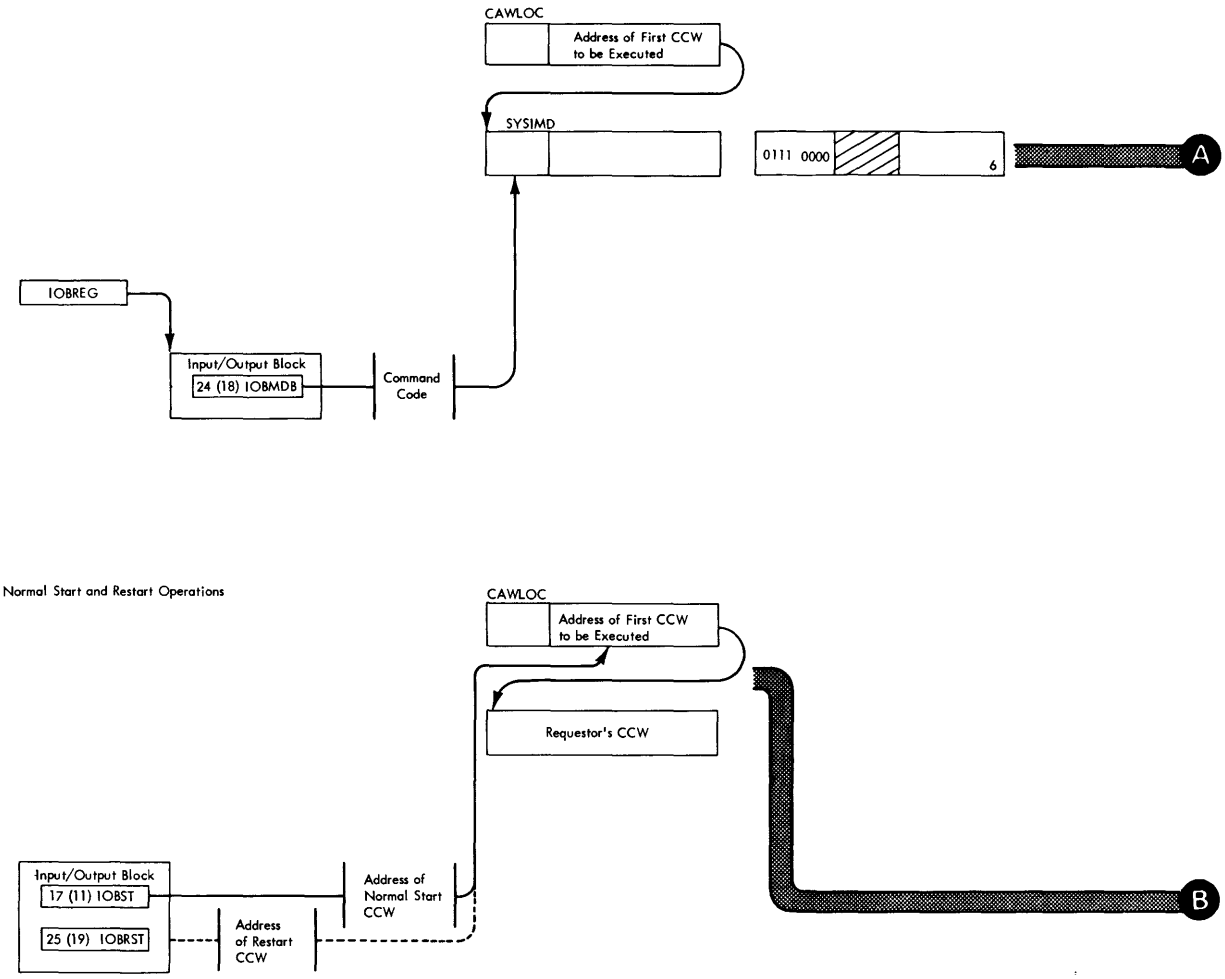
When a channel is found to be unavailable and there are no alternate paths, the request element is queued

When a channel is found to be unavailable but one or more alternate paths exist, additional attempts are made on the alternate channels. If all of the alternate channels are found to be unavailable, the request element is queued.

For additional information, see:

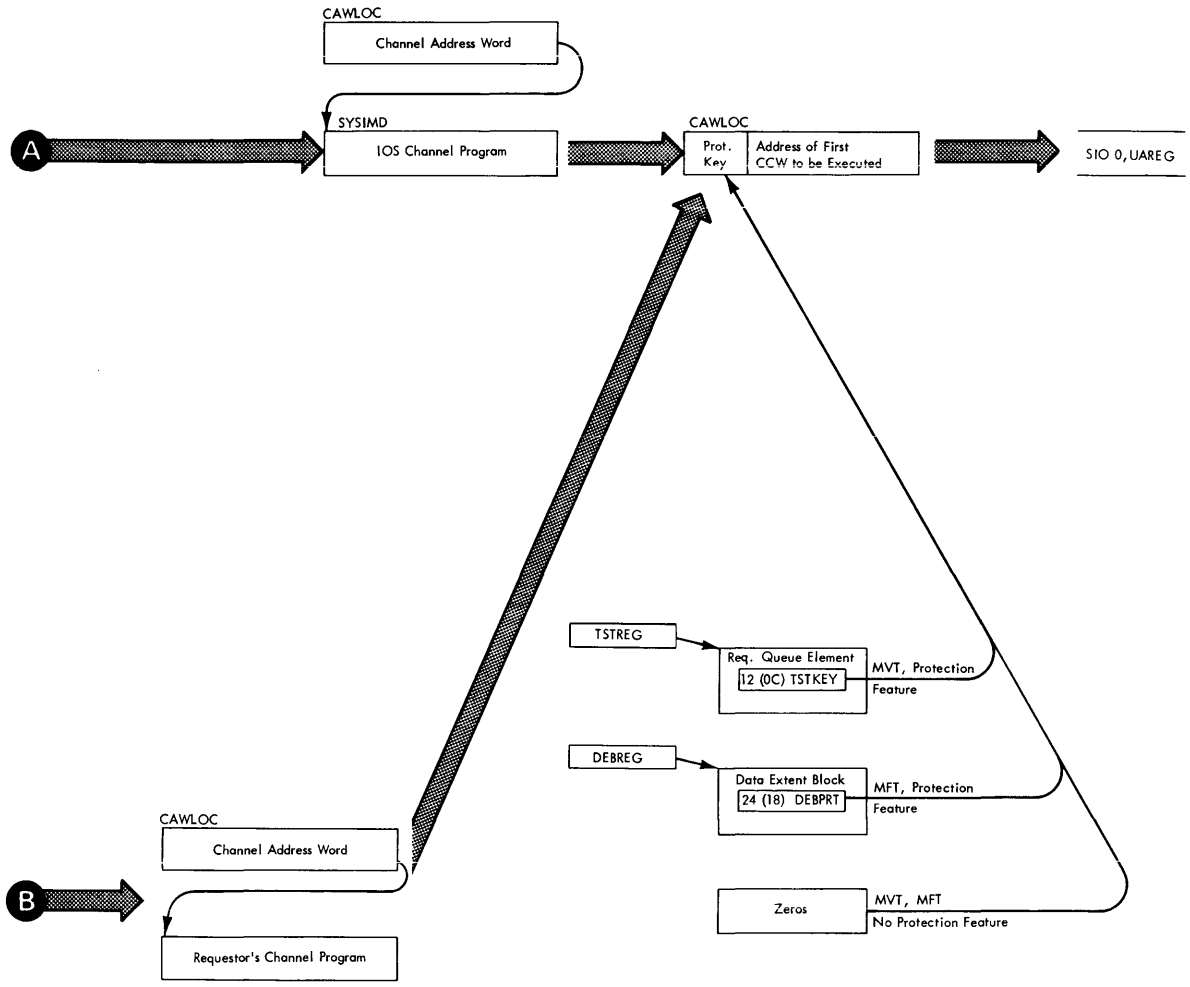
- Chart AC, Test Channel Routines.

The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.



The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.

Diagram 4. Starting Unit–Record, Communications, and Graphics Devices



For additional information, see:

- Chart AD, Start I/O Routine for Unit Record and Communications Devices.
- Chart AK, Start I/O Subroutine.

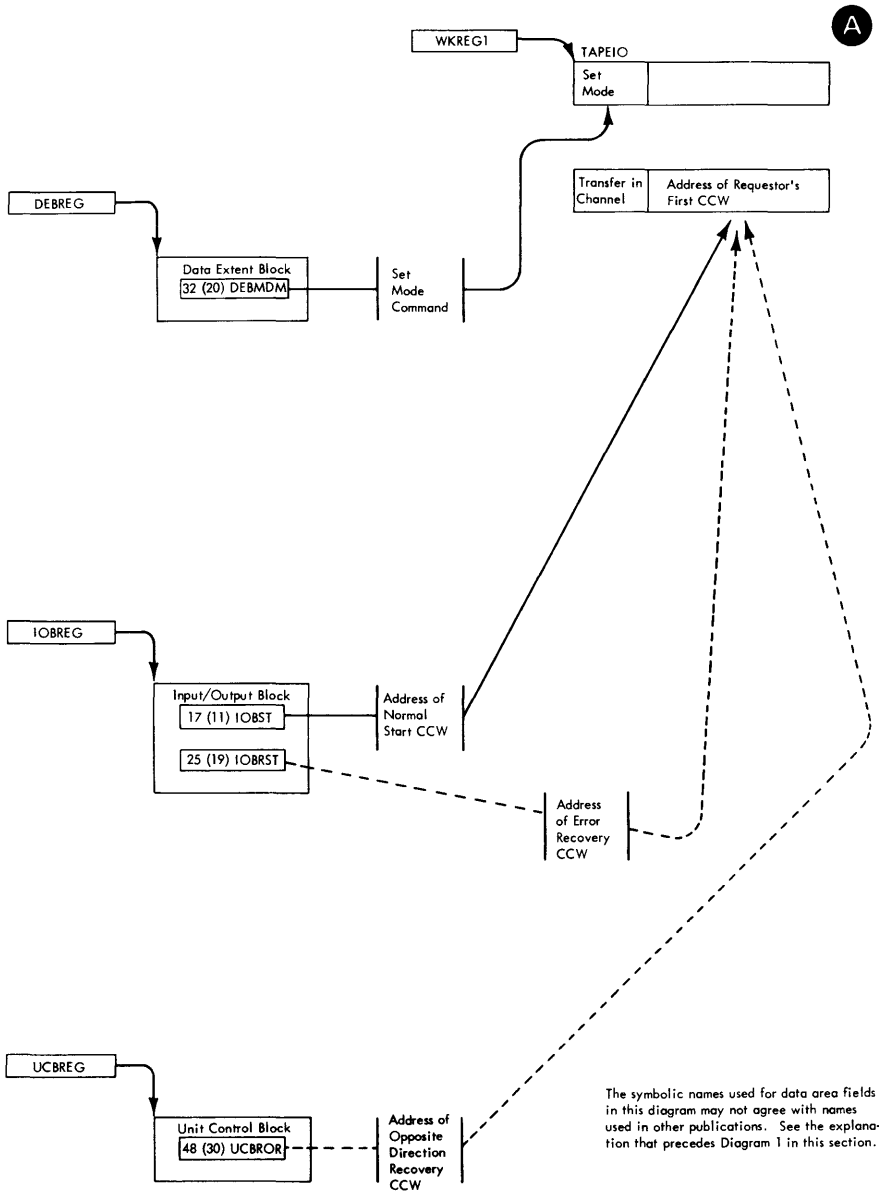
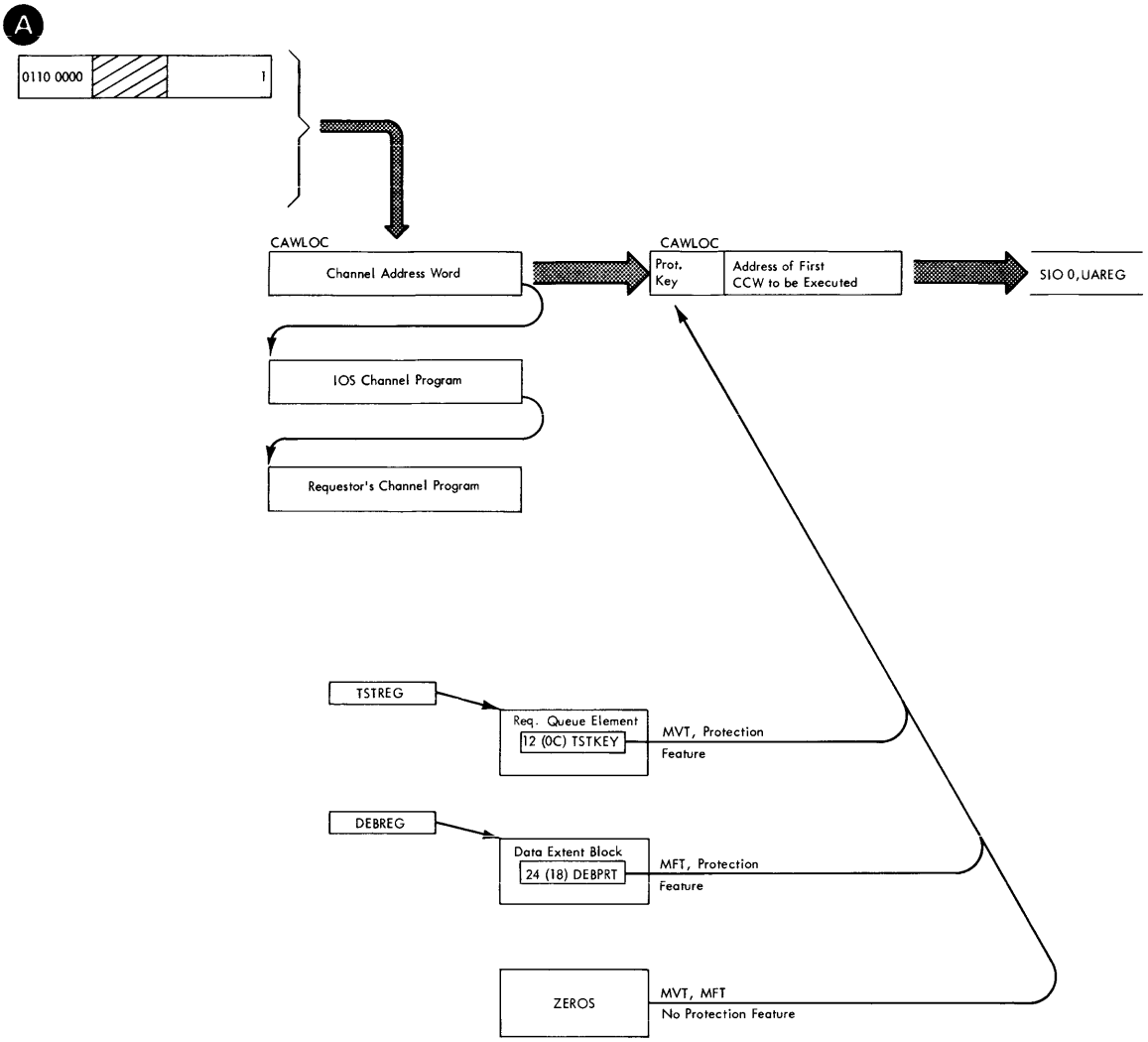
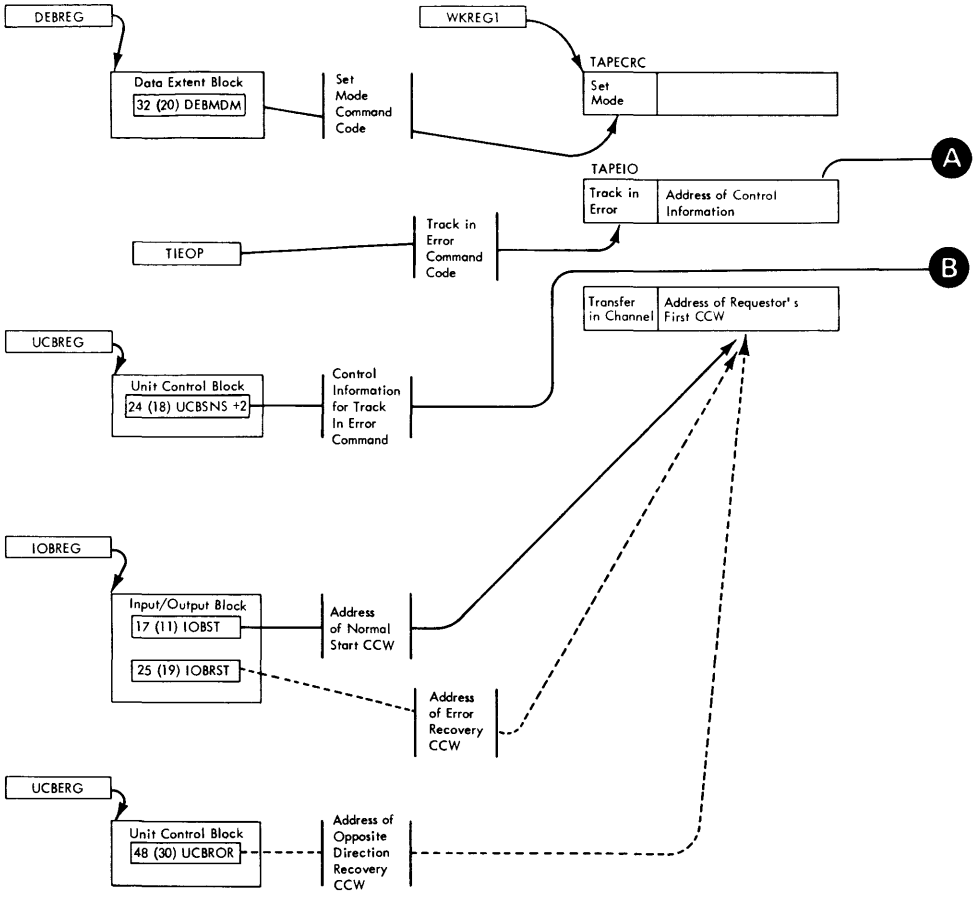


Diagram 5. Starting Magnetic–Tape Devices: Normal Start, Restart, and Opposite Direction Recovery Operations



For additional information, see:

- Chart AE, Start I/O Routine for Magnetic Tape Devices.
- Chart AK, Start I/O Subroutine.

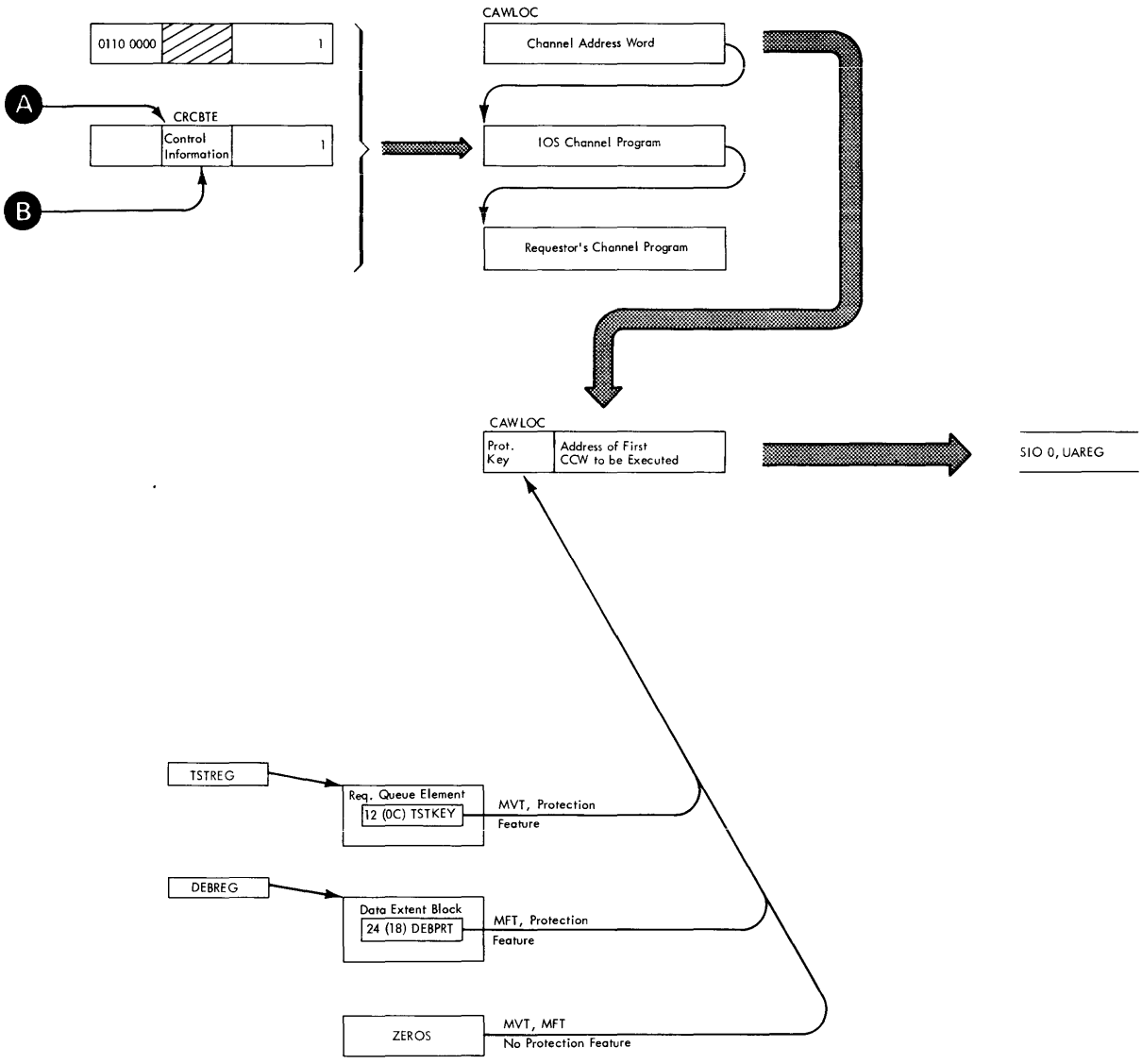


The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.

For additional information, see:

- Chart AE, Start I/O Routine for Magnetic Tape Devices.
- Chart AK, Start I/O Subroutines.

Diagram 6. Starting Magnetic–Tape Devices After a Cyclic Redundancy Check Condition


0110 0000
1
A
CRCBTE
Control Information
1
B
CAWLOC
Channel Address Word
IOS Channel Program
Requestor's Channel Program
CAWLOC
Prot. Key
Address of First CCW to be Executed
SIO 0, UAREG
TSTREG
Req. Queue Element
12 (0C) TSTKEY
MVT, Protection Feature
DEBREG
Data Extent Block
24 (18) DEBPRT
MFT, Protection Feature
ZEROS
MVT, MFT
No Protection Feature

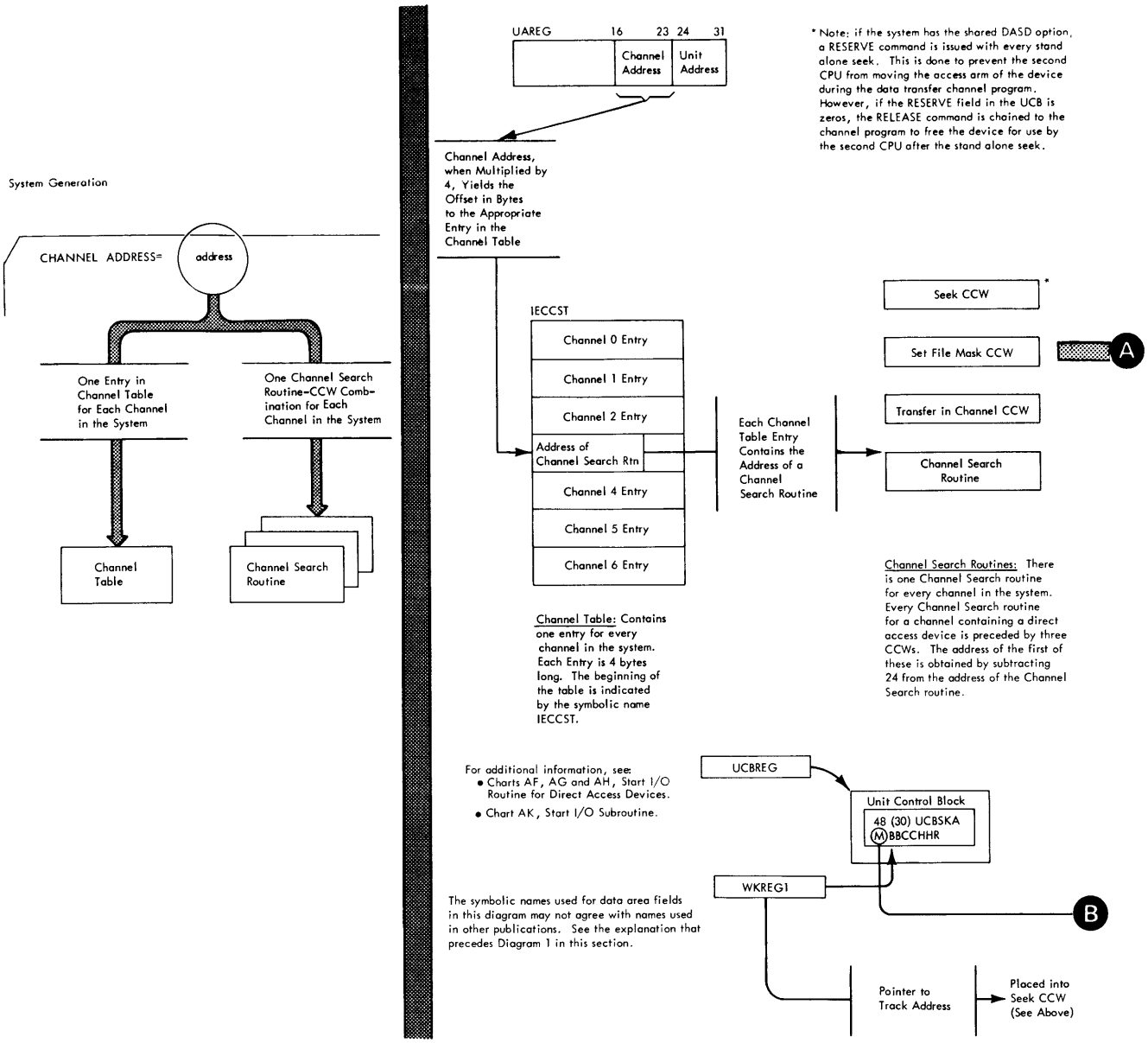
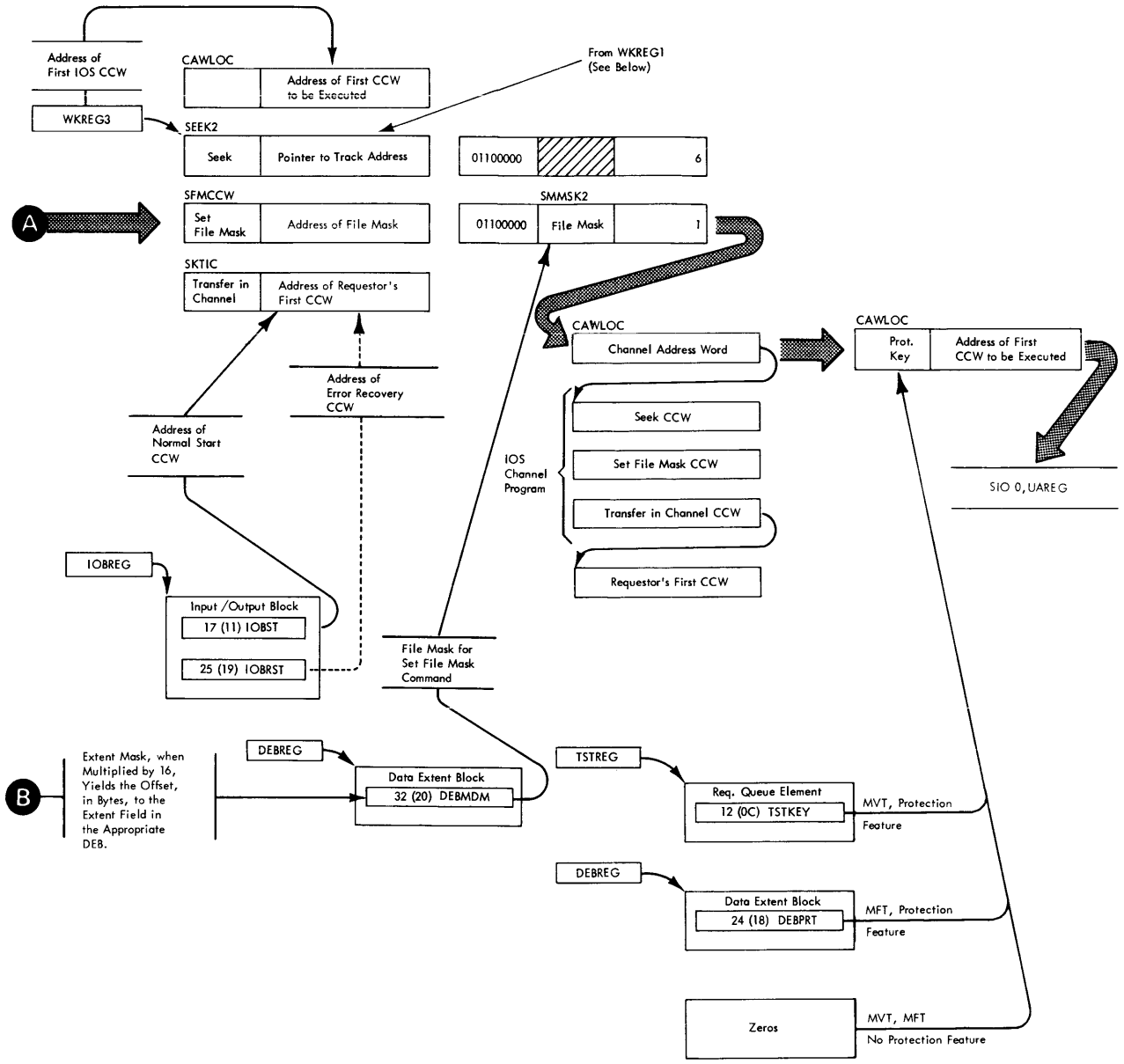
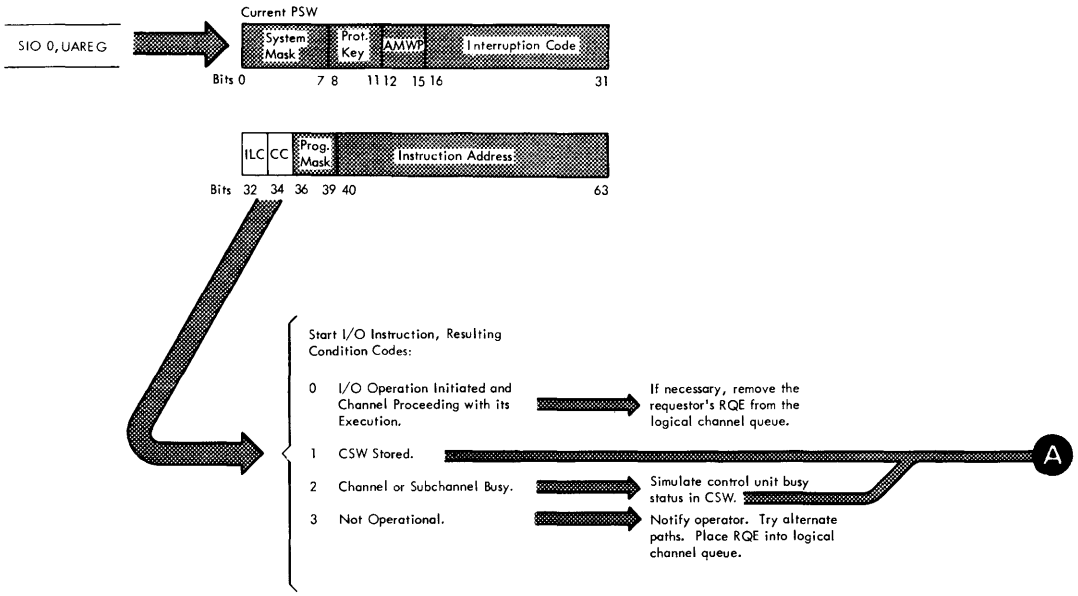


Diagram 7. Starting Direct-Access Devices


Address of First IOS CCW
WKREG3
CAWLOC
Address of First CCW to be Executed
From WKREG1 (See Below)
SEEK2
Seek
Pointer to Track Address
01100000
6
A
SFMCCW
Set File Mask
Address of File Mask
SMMSK2
01100000
File Mask
1
SKTIC
Transfer in Channel
Address of Requestor's First CCW
CAWLOC
Channel Address Word
CAWLOC
Prot. Key
Address of First CCW to be Executed
Address of Error Recovery CCW
Address of Normal Start CCW
IOS Channel Program
Seek CCW
Set File Mask CCW
Transfer in Channel CCW
Requestor's First CCW
SIO 0,UAREG
IOBREG
Input /Output Block
17 (11) IOBST
25 (19) IOBRST
File Mask for Set File Mask Command
B
Extent Mask, when Multiplied by 16, Yields the Offset, in Bytes, to the Extent Field in the Appropriate DEB.
DEBREG
Data Extent Block
32 (20) DEBMDM
TSTREG
Req. Queue Element
12 (0C) TSTKEY
MVT, Protection Feature
DEBREG
Data Extent Block
24 (18) DEBPRT
MFT, Protection Feature
Zeros
MVT, MFT No Protection Feature

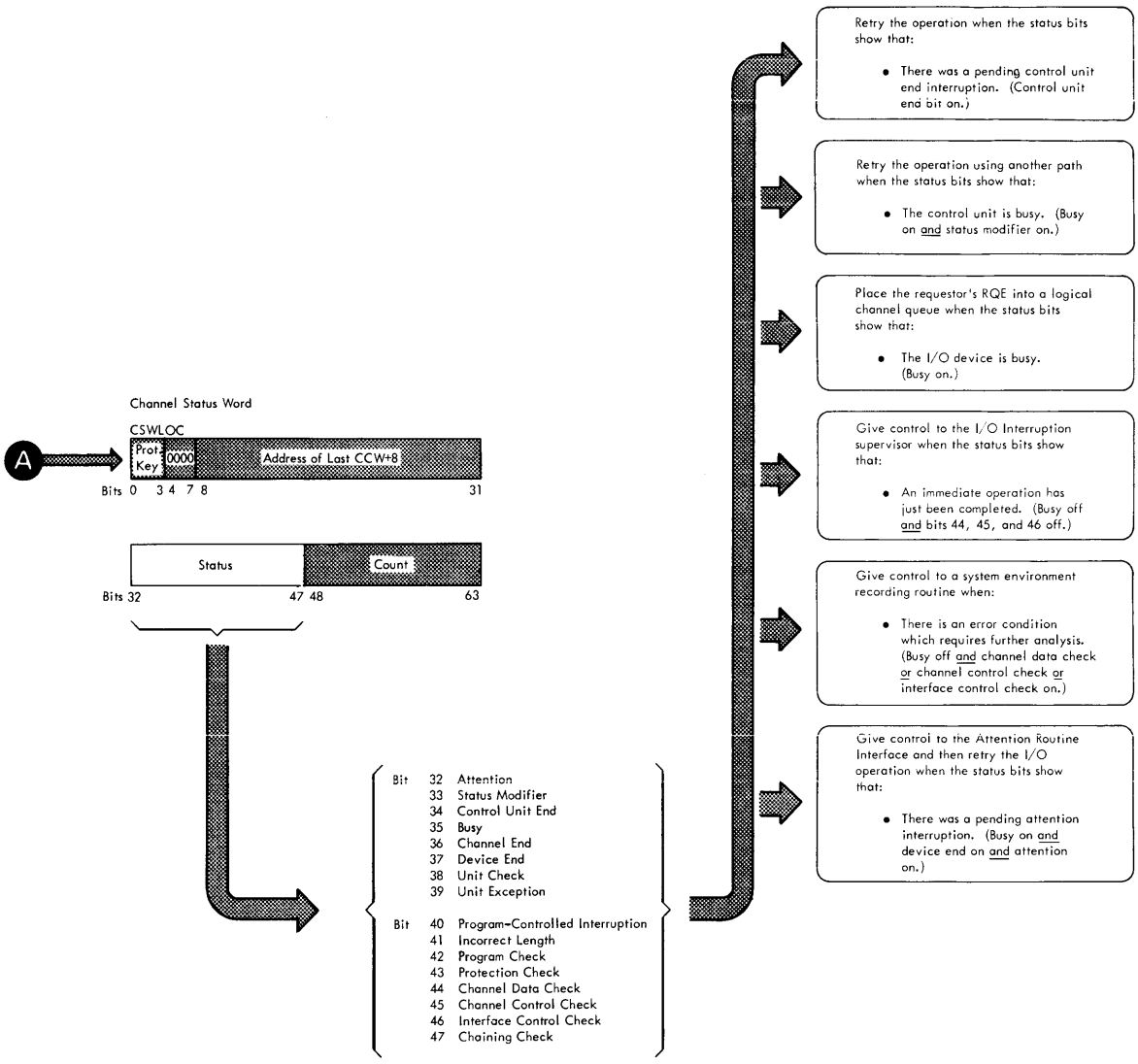


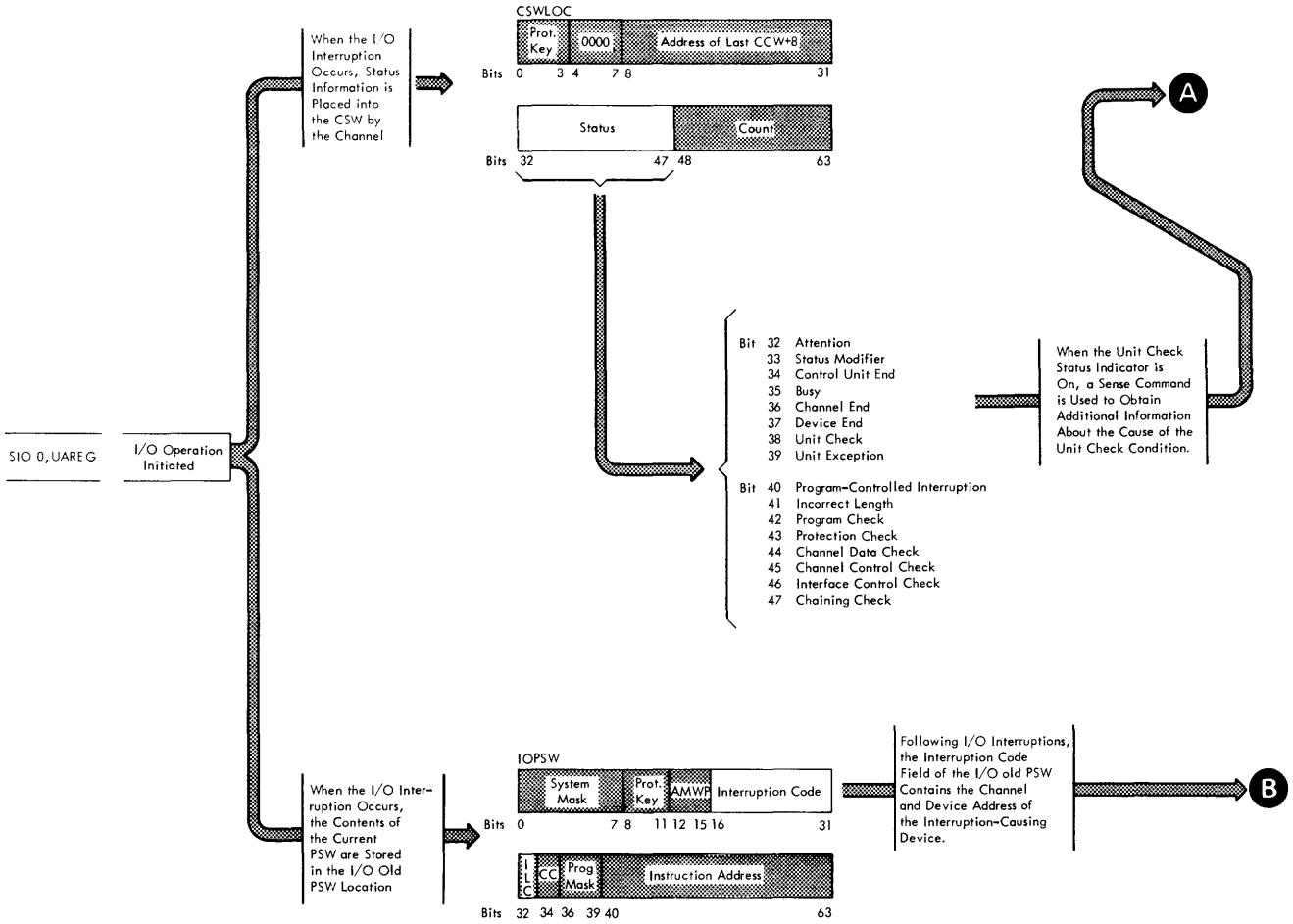
For additional information, see:

- Chart AK, Start I/O Subroutine.
- Chart AL, Post Start I/O Routine.

The flow of control during analysis of CSW status bits is shown in Chart AI, Post Start I/O Routine.

Diagram 8. Checking Condition Codes


Channel Status Word
CSWLOC
A
Prot Key
0000
Address of Last CCW+8
Bits 0 3 4 7 8 31
Status
Count
Bits 32 47 48 63
Bit 32 Attention
33 Status Modifier
34 Control Unit End
35 Busy
36 Channel End
37 Device End
38 Unit Check
39 Unit Exception
Bit 40 Program-Controlled Interruption
41 Incorrect Length
42 Program Check
43 Protection Check
44 Channel Data Check
45 Channel Control Check
46 Interface Control Check
47 Chaining Check
Retry the operation when the status bits show that:
• There was a pending control unit end interruption. (Control unit end bit on.)
Retry the operation using another path when the status bits show that:
• The control unit is busy. (Busy on and status modifier on.)
Place the requestor's RQE into a logical channel queue when the status bits show that:
• The I/O device is busy. (Busy on.)
Give control to the I/O Interruption supervisor when the status bits show that:
• An immediate operation has just been completed. (Busy off and bits 44, 45, and 46 off.)
Give control to a system environment recording routine when:
• There is an error condition which requires further analysis. (Busy off and channel data check or channel control check or interface control check on.)
Give control to the Attention Routine Interface and then retry the I/O operation when the status bits show that:
• There was a pending attention interruption. (Busy on and device end on and attention on.)

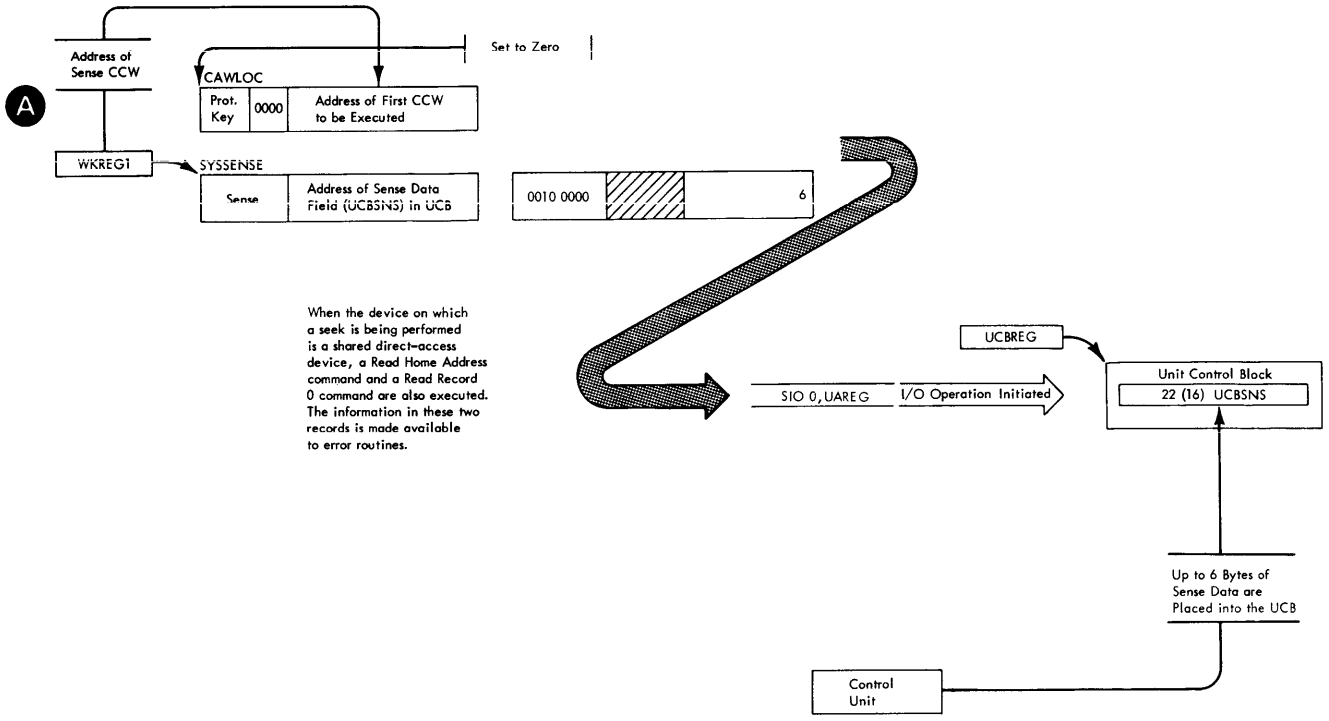


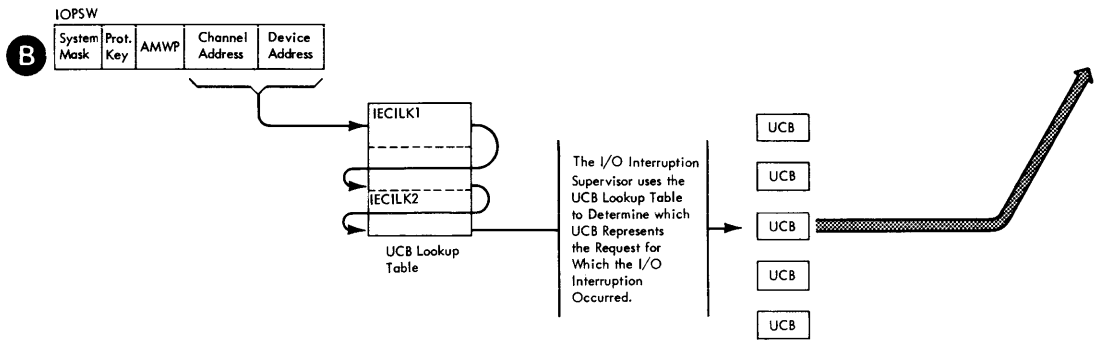
The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.

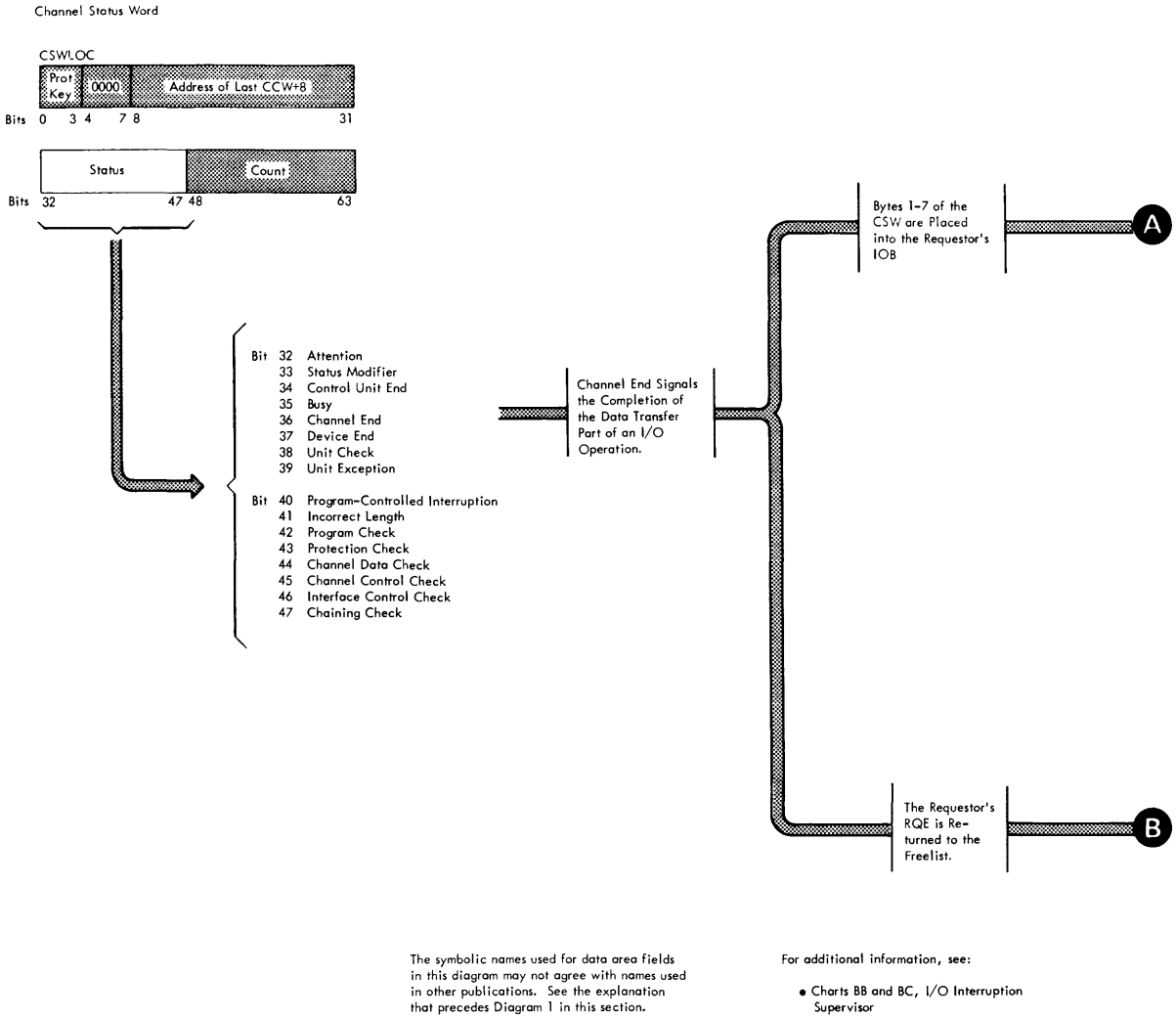
For additional information, see:

- Charts BA to BE, I/O Interruption Supervisor.
- Charts BG and BH, Sense Subroutine.

Diagram 9. Checking Status Indicators (Part 1 of 2)


A
Address of Sense CCW
Set to Zero
CAWLOC
Prot. Key
0000
Address of First CCW to be Executed
WKREG1
SYSSENSE
Sense
Address of Sense Data Field (UCBSNS) in UCB
0010 0000
6
When the device on which a seek is being performed is a shared direct-access device, a Read Home Address command and a Read Record 0 command are also executed. The information in these two records is made available to error routines.
UCBREG
Unit Control Block
22 (16) UCBSNS
SIO 0,UAREG
I/O Operation Initiated
Up to 6 Bytes of Sense Data are Placed into the UCB
Control Unit


B
IOPSW
System Mask
Prot. Key
AMWP
Channel Address
Device Address
IECILK1
IECILK2
UCB Lookup Table
The I/O Interruption Supervisor uses the UCB Lookup Table to Determine which UCB Represents the Request for Which the I/O Interruption Occurred.
UCB
UCB
UCB
UCB
UCB

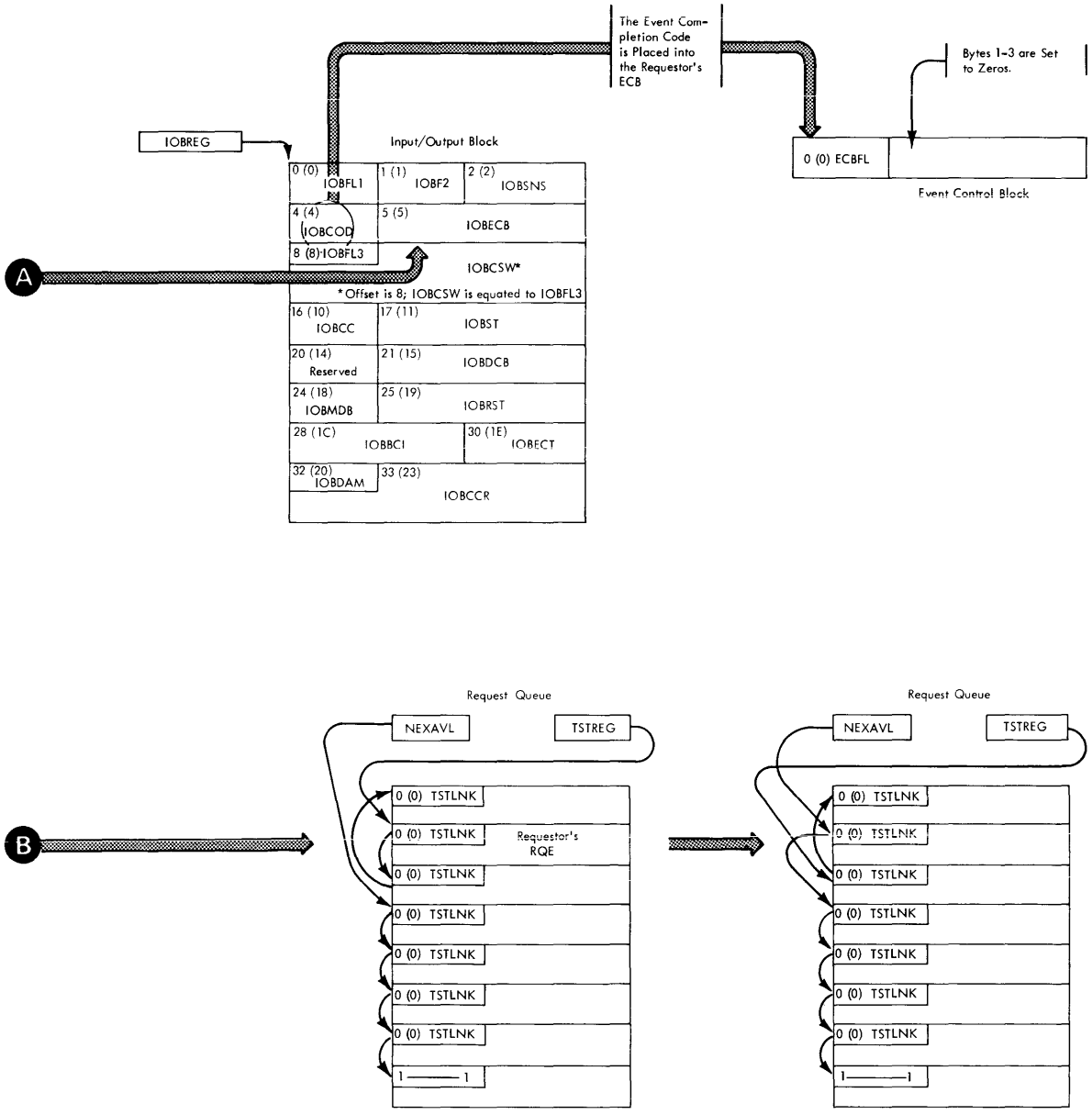


The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.

For additional information, see:

- Charts BB and BC, I/O Interruption Supervisor

Diagram 9. Checking Status Indicators (Part 2 of 2)


The Event Completion Code is Placed into the Requestor's ECB
Bytes 1-3 are Set to Zeros.
IOBREG
Input/Output Block
0 (0) IOBFL1
1 (1) IOBF2
2 (2) IOBSNS
4 (4) IOBCOD
5 (5) IOBECB
8 (8) IOBFL3
IOBCSW*
*Offset is 8; IOBCSW is equated to IOBFL3
16 (10) IOBCC
17 (11) IOBST
20 (14) Reserved
21 (15) IOBDCB
24 (18) IOBMDB
25 (19) IOBRST
28 (1C) IOBBCI
30 (1E) IOBECT
32 (20) IOBDAM
33 (23) IOBCCR
0 (0) ECBFL
Event Control Block
A
B
Request Queue
NEXAVL
TSTREG
0 (0) TSTLNK
Requestor's RQE
1 1
Request Queue
NEXAVL
TSTREG
0 (0) TSTLNK
1 1

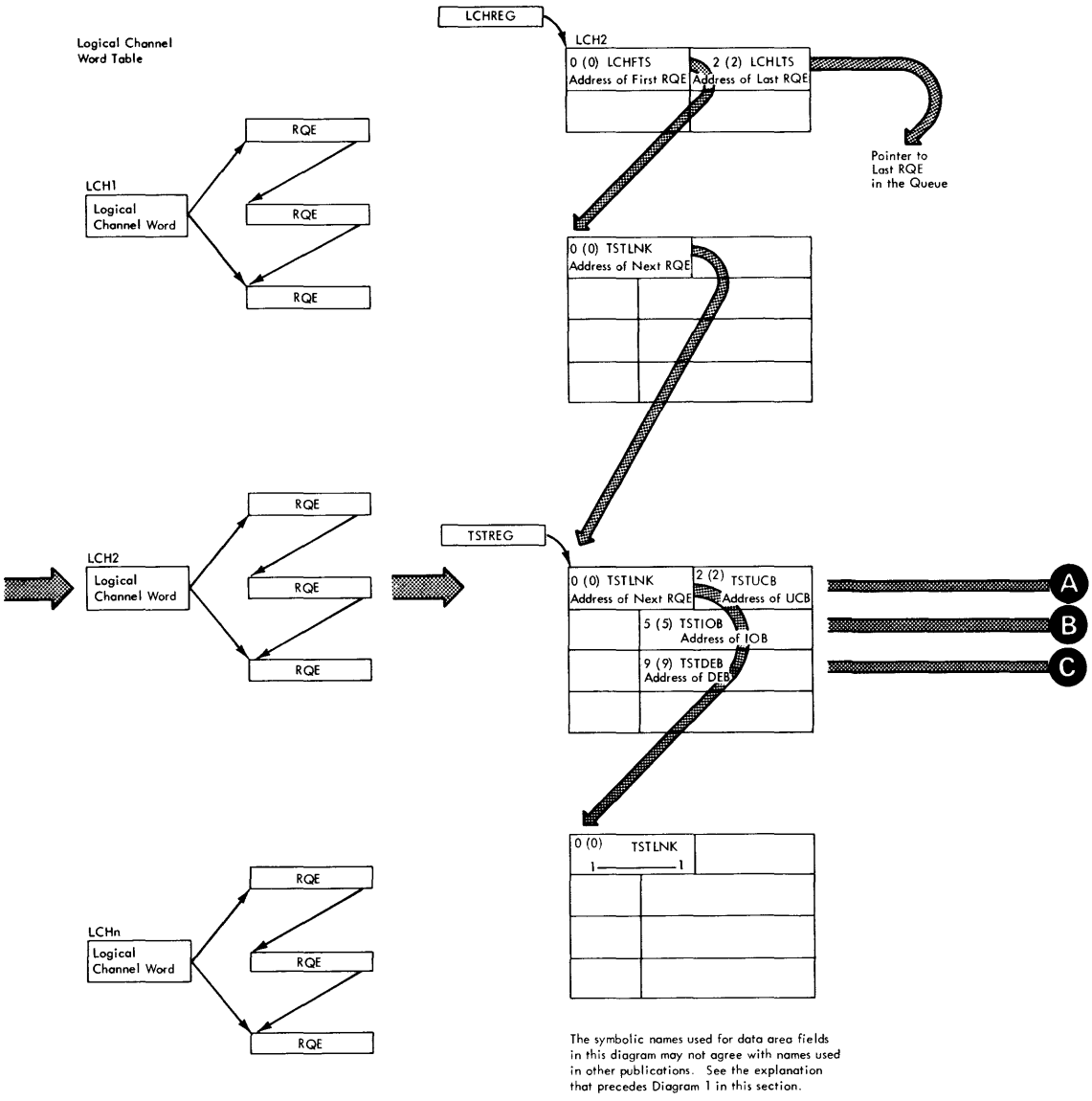
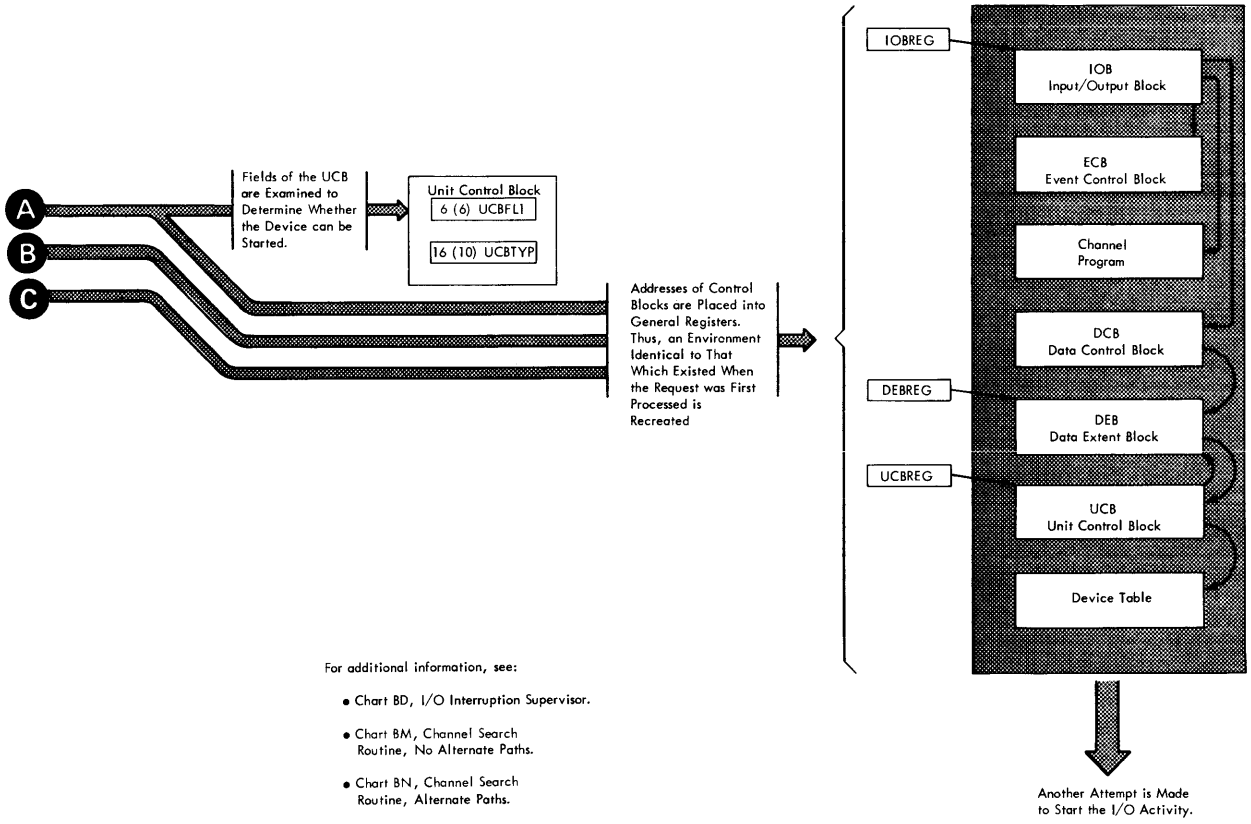


Diagram 10. Starting Scheduled I/O Operations



For additional information, see:

- Chart BD, I/O Interruption Supervisor.
- Chart BM, Channel Search Routine, No Alternate Paths.
- Chart BN, Channel Search Routine, Alternate Paths.
- Charts BO and BP, Channel Search Routine, Multiplexor Channel.

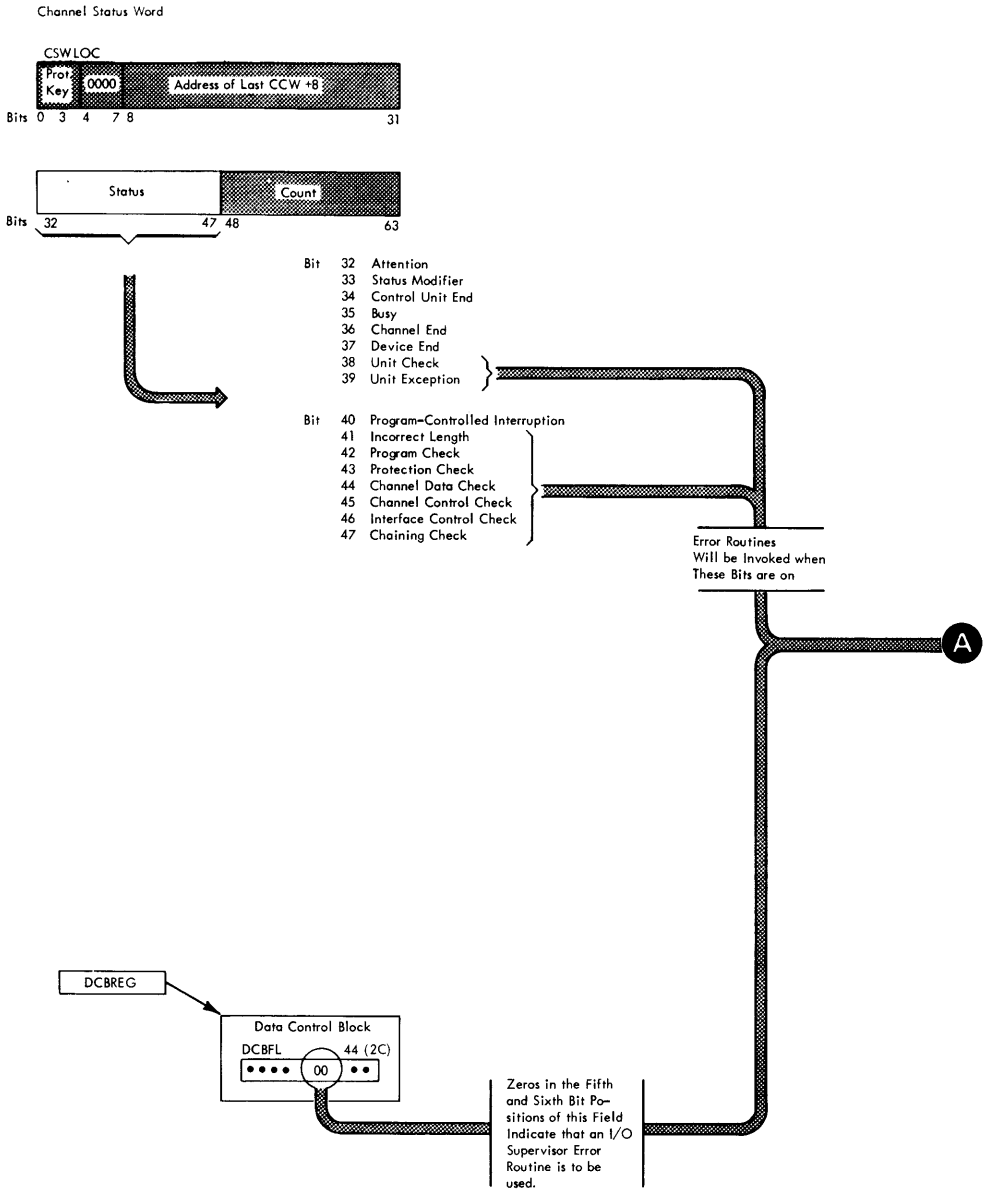
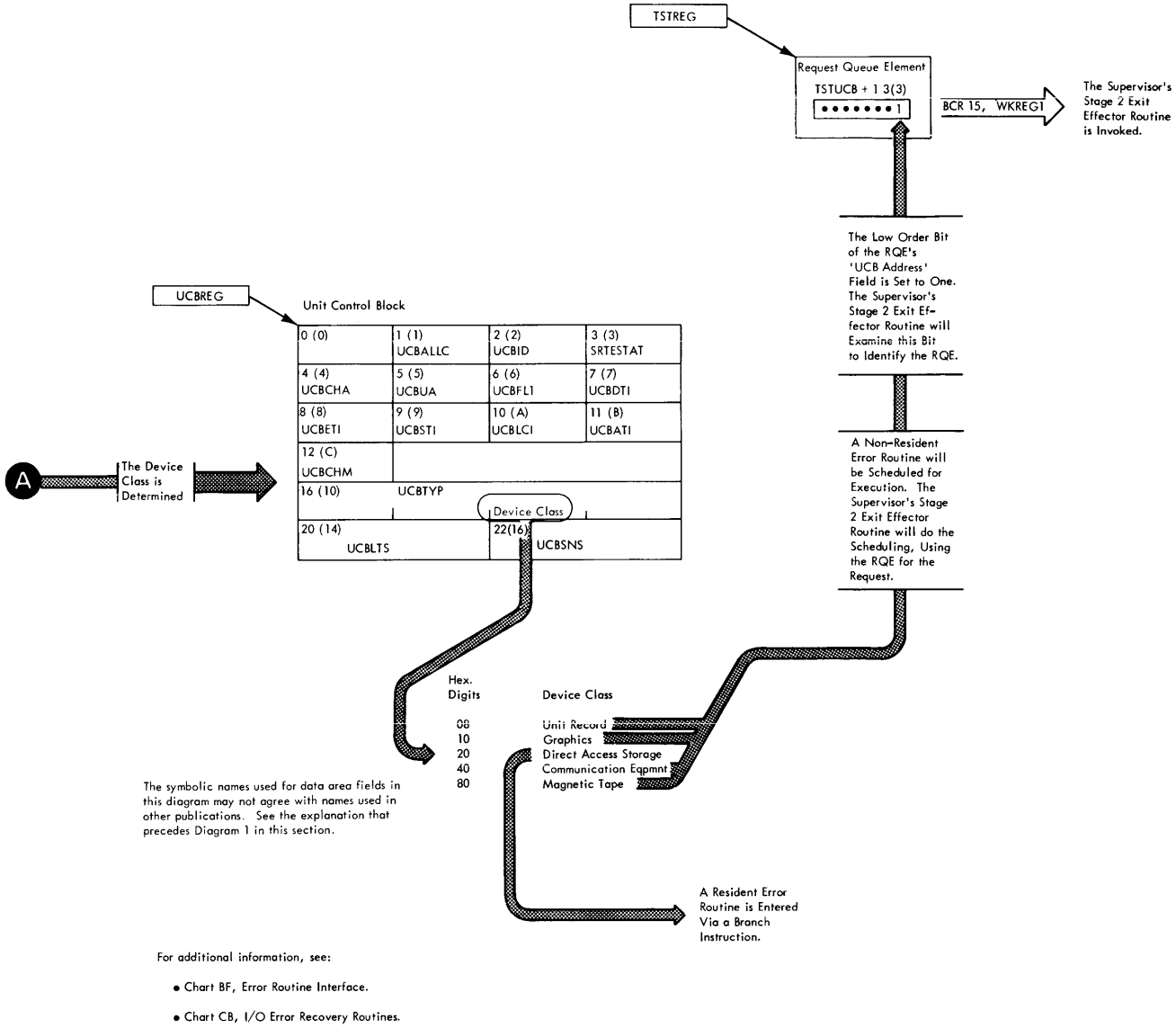


Diagram 11. Invoking Error Routines (Part 1 of 2)



For additional information, see:

- Chart BF, Error Routine Interface.
- Chart CB, I/O Error Recovery Routines.

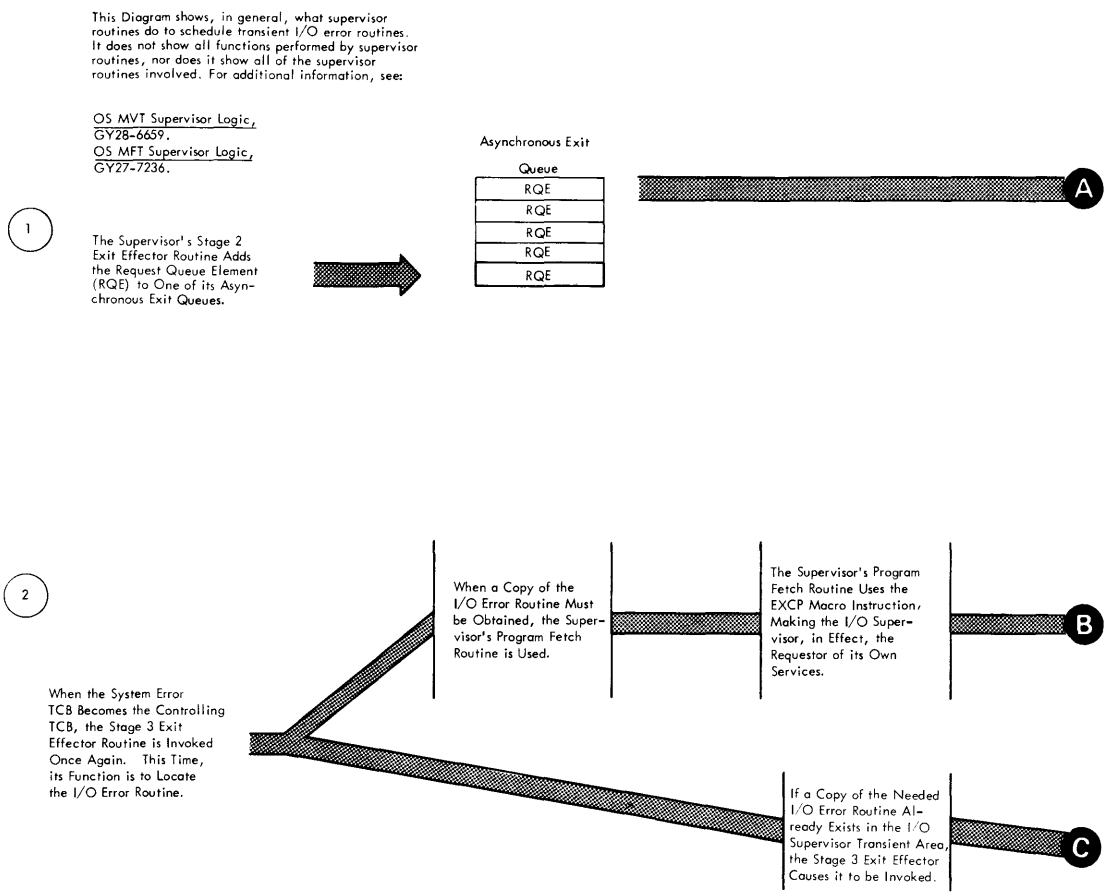
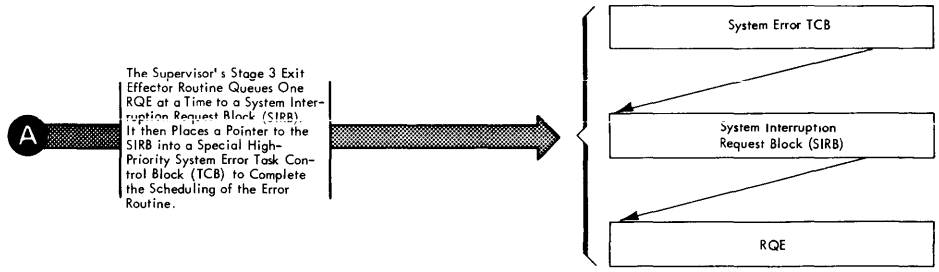
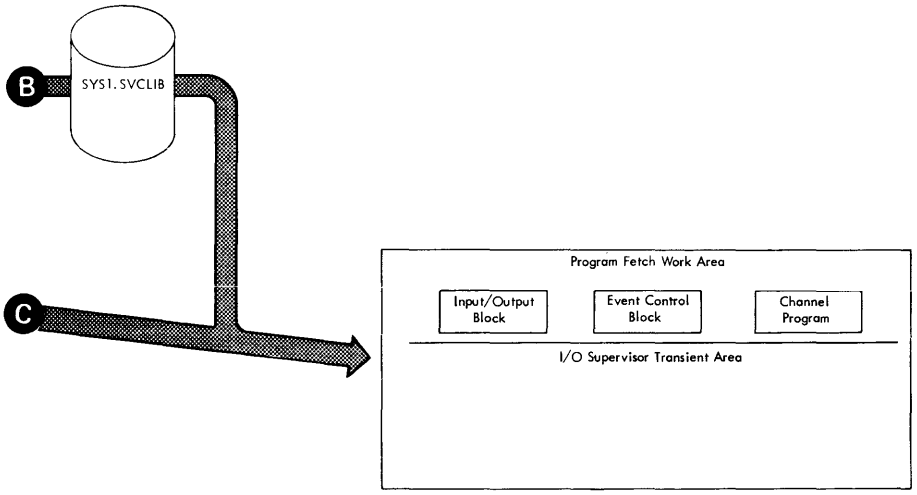


Diagram 11. Invoking Error Routines (Part 2 of 2)





The input/output block (IOB), event control block (ECB), and the channel program used in obtaining the I/O error routine are contained in a 68-byte program fetch work area which immediately precedes the I/O supervisor transient area.

When a message is to be written to the operator, the error recovery routine sets a message type flag in the input/output block and invokes the Write-to-Operator routine.

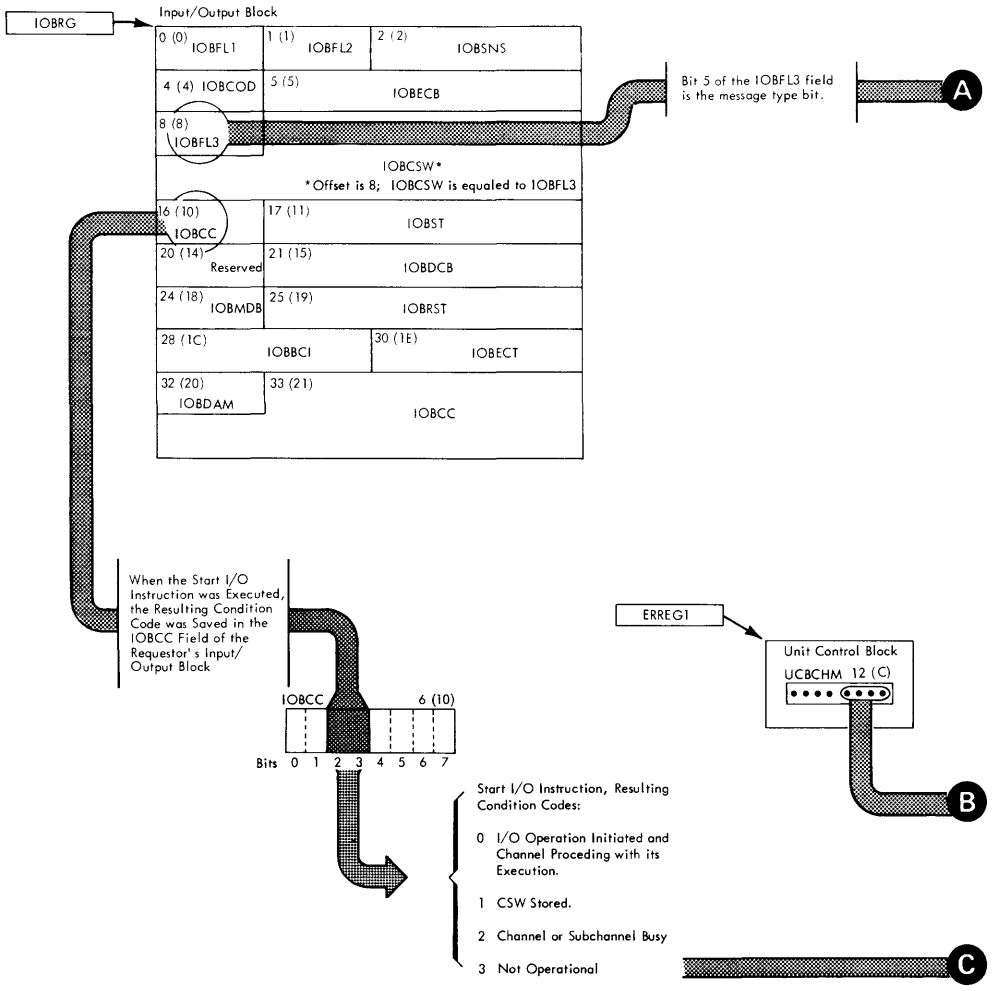
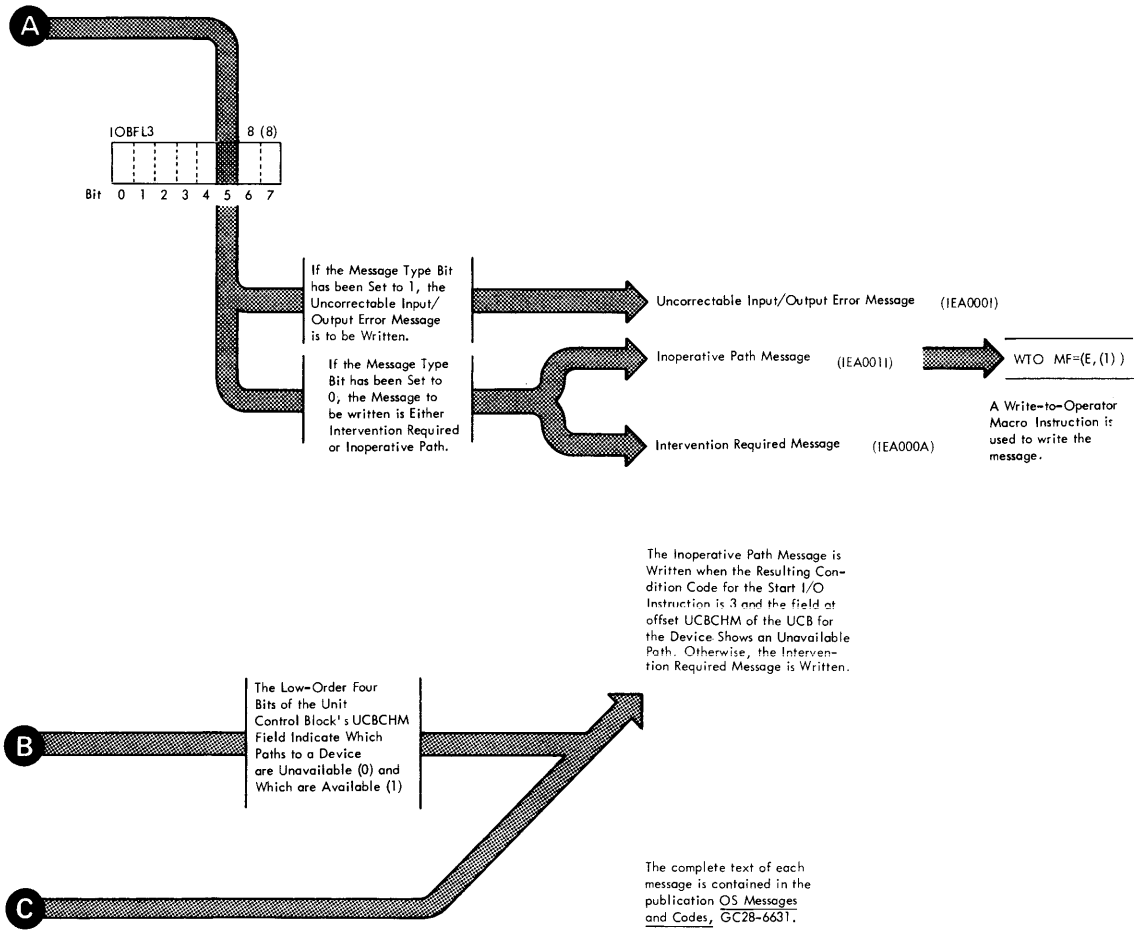


Diagram 12. Writing Error Recovery Messages to the Operator


A
IOBFL3
8 (8)
Bit 0 1 2 3 4 5 6 7
If the Message Type Bit has been Set to 1, the Uncorrectable Input/ Output Error Message is to be Written.
If the Message Type Bit has been Set to 0, the Message to be written is Either Intervention Required or Inoperative Path.
Uncorrectable Input/Output Error Message (IEA000I)
Inoperative Path Message (IEA001I)
Intervention Required Message (IEA000A)
WTO MF=(E,(1))
A Write-to-Operator Macro Instruction it used to write the message.
The Inoperative Path Message is Written when the Resulting Condition Code for the Start I/O Instruction is 3 and the field at offset UCBCHM of the UCB for the Device Shows an Unavailable Path. Otherwise, the Intervention Required Message is Written.
B
The Low-Order Four Bits of the Unit Control Block's UCBCHM Field Indicate Which Paths to a Device are Unavailable (0) and Which are Available (1)
C
The complete text of each message is contained in the publication OS Messages and Codes, GC28-6631.
The symbolic names used for data area fields in this diagram may not agree with names used in other publications. See the explanation that precedes Diagram 1 in this section.

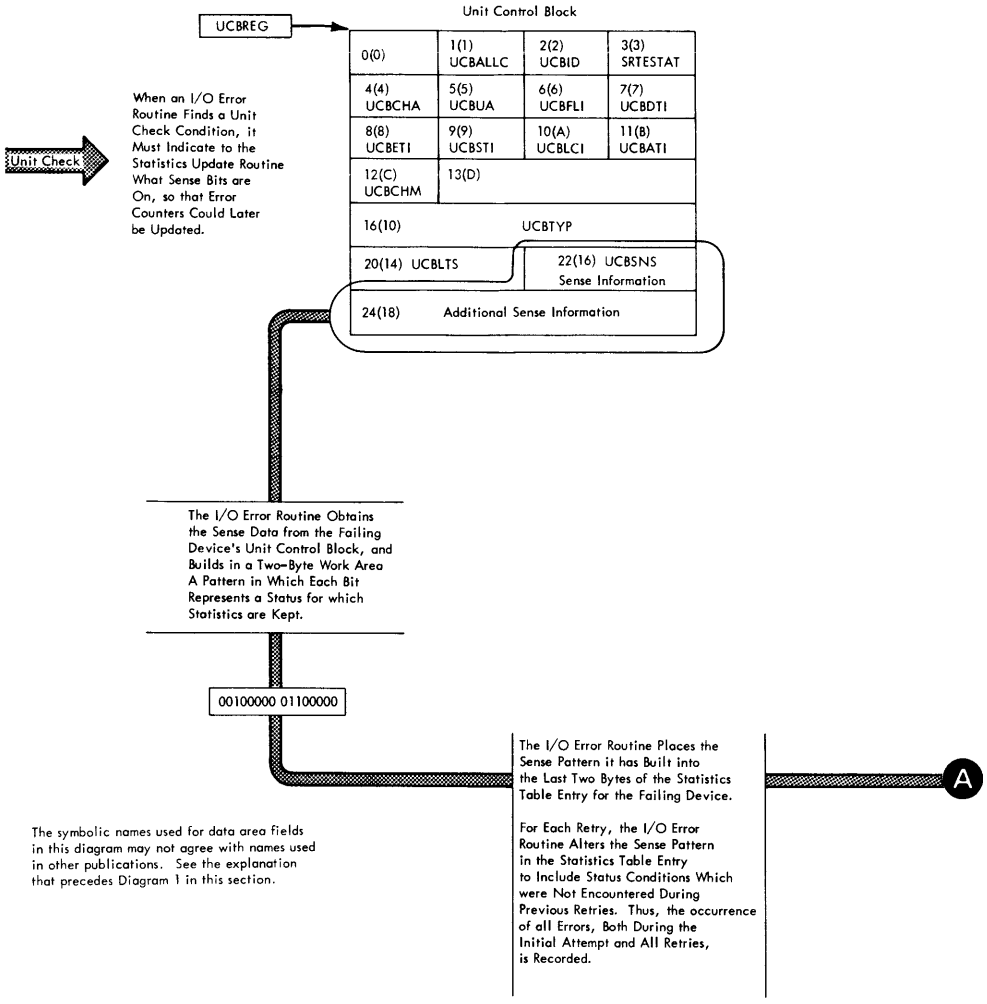
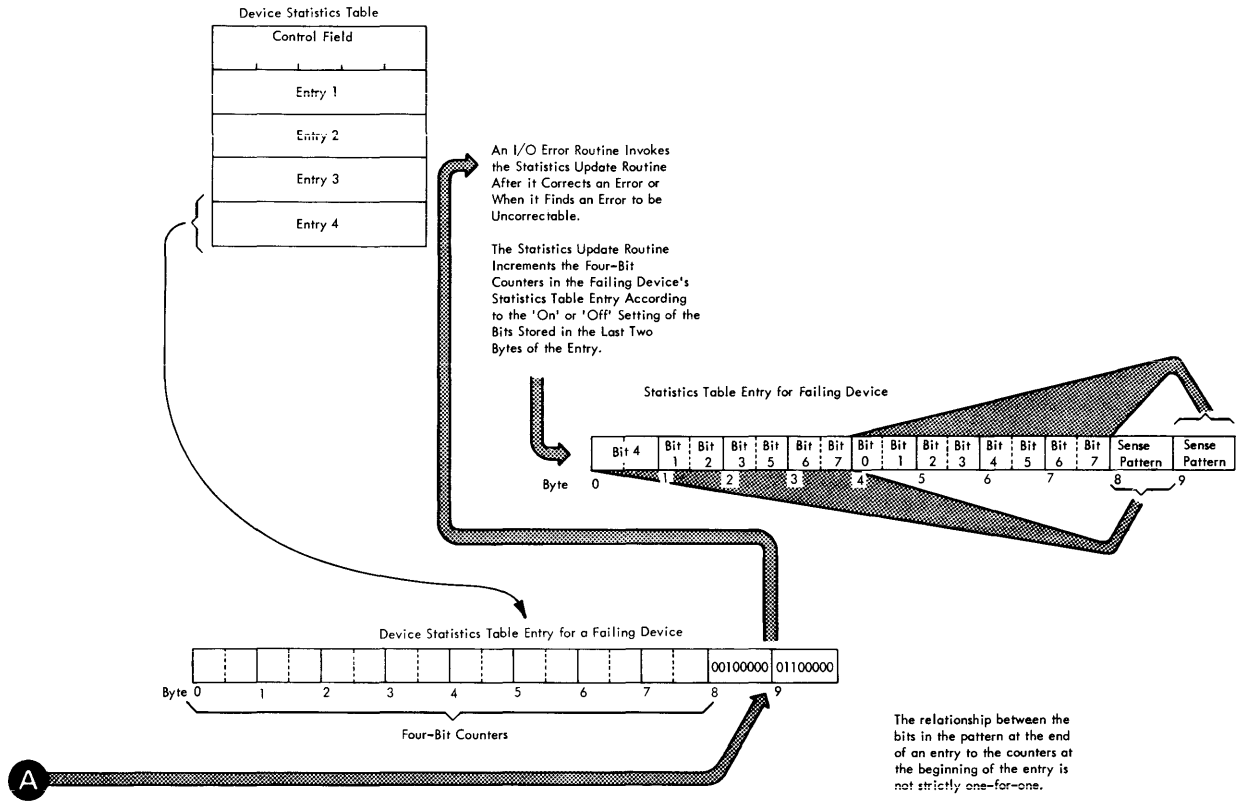


Diagram 13. Updating the Device Statistics Table (except for 2305 and 3330)


Device Statistics Table
Control Field
Entry 1
Entry 2
Entry 3
Entry 4
An I/O Error Routine Invokes the Statistics Update Routine After it Corrects an Error or When it Finds an Error to be Uncorrectable.
The Statistics Update Routine Increments the Four-Bit Counters in the Failing Device's Statistics Table Entry According to the 'On' or 'Off' Setting of the Bits Stored in the Last Two Bytes of the Entry.
Statistics Table Entry for Failing Device
Bit 4
Bit 1
Bit 2
Bit 3
Bit 5
Bit 6
Bit 7
Bit 0
Bit 1
Bit 2
Bit 3
Bit 4
Bit 5
Bit 6
Bit 7
Sense Pattern
Sense Pattern
Byte
0
1
2
3
4
5
6
7
8
9
Device Statistics Table Entry for a Failing Device
00100000
01100000
Byte 0
1
2
3
4
5
6
7
8
9
Four-Bit Counters
A
Note: In the sense pattern, only one bit is set for each type of error, regardless of how many times the error recurs during retries of a request.
The relationship between the bits in the pattern at the end of an entry to the counters at the beginning of the entry is not strictly one-for-one.
Bit 0 of the first sense pattern byte is not used; bit 4 is used to increment one of the first two counters (temporary read failures, temporary write failures); the remaining counters correspond to the remaining bits.

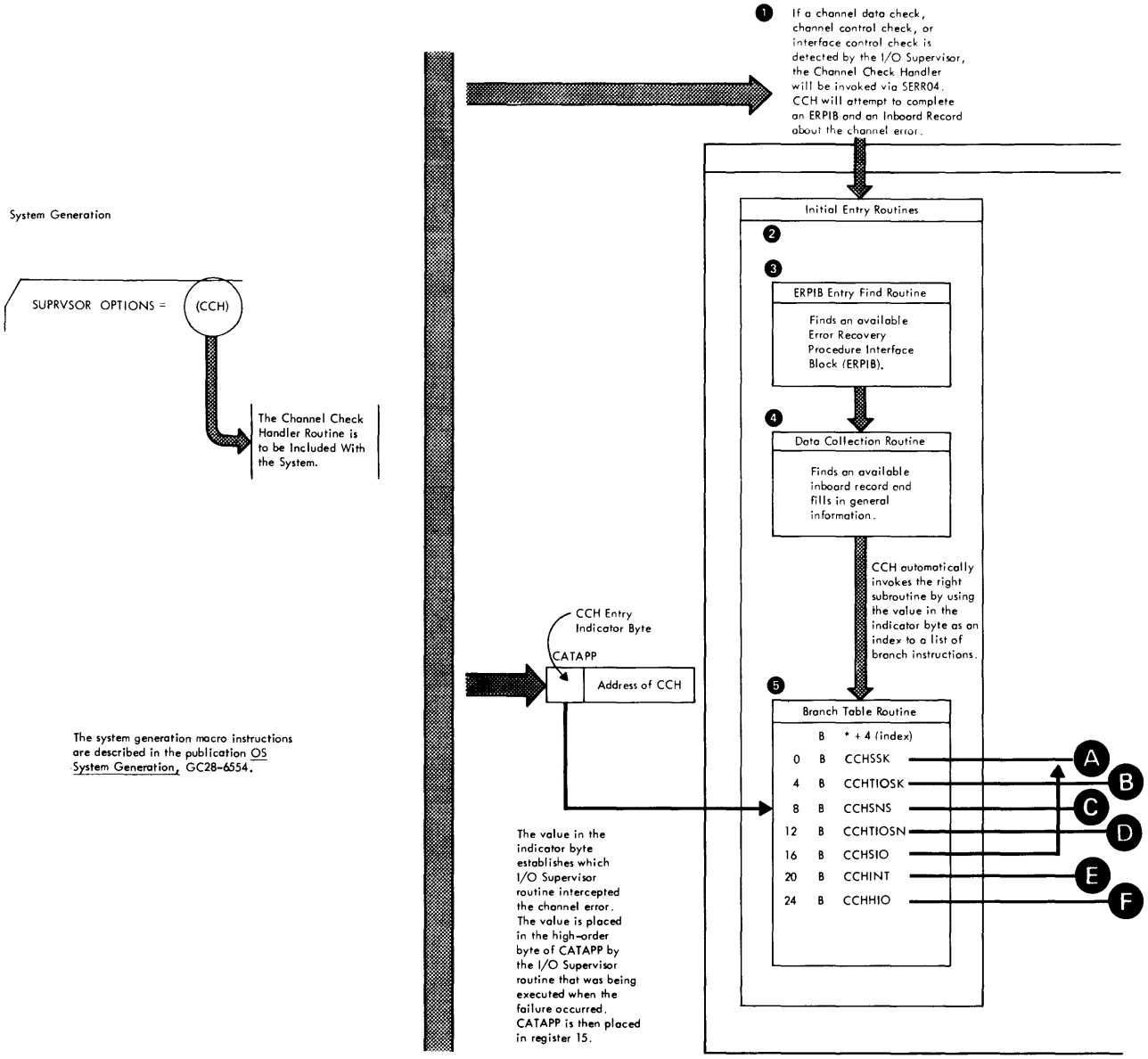
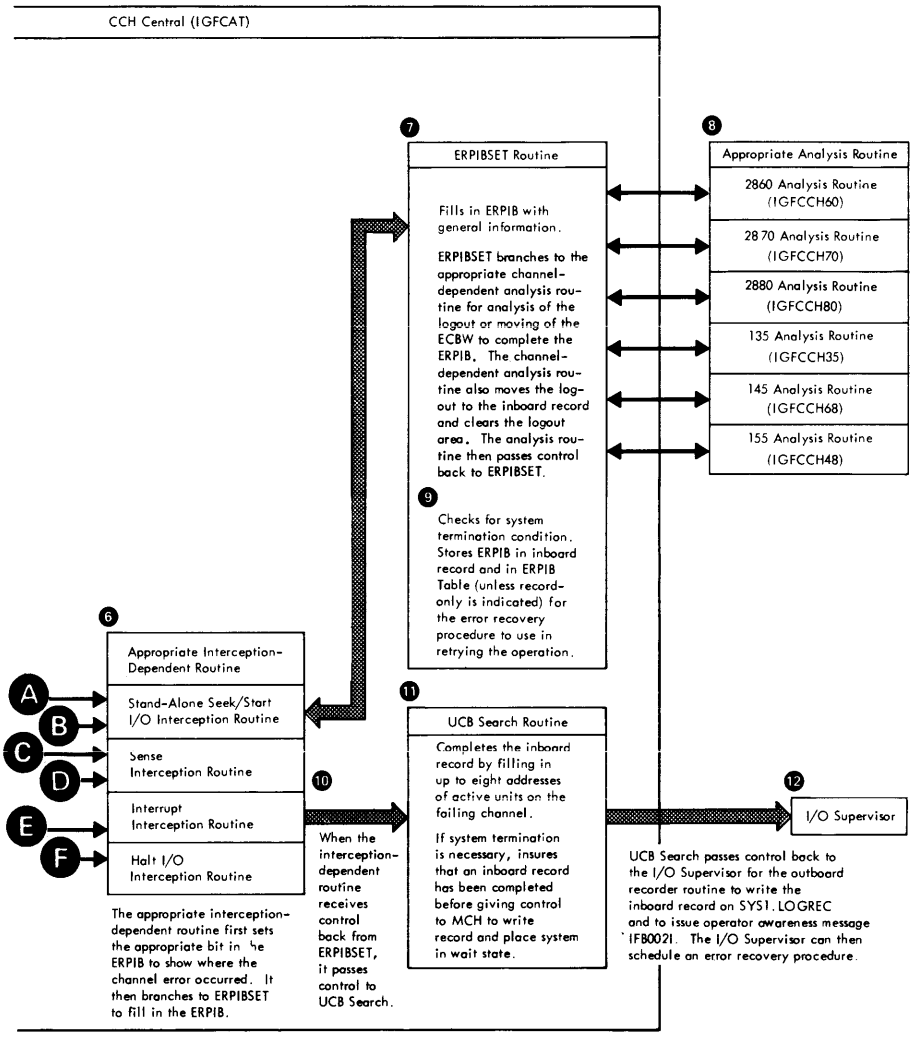


Diagram 14. Channel Check Handler


CCH Central (IGFCAT)
7
ERPIBSET Routine
Fills in ERPIB with general information.
ERPIBSET branches to the appropriate channel-dependent analysis routine for analysis of the logout or moving of the ECBW to complete the ERPIB. The channel-dependent analysis routine also moves the logout to the inboard record and clears the logout area. The analysis routine then passes control back to ERPIBSET.
9
Checks for system termination condition. Stores ERPIB in inboard record and in ERPIB Table (unless record-only is indicated) for the error recovery procedure to use in retrying the operation.
8
Appropriate Analysis Routine
2860 Analysis Routine (IGFCCH60)
2870 Analysis Routine (IGFCCH70)
2880 Analysis Routine (IGFCCH80)
135 Analysis Routine (IGFCCH35)
145 Analysis Routine (IGFCCH68)
155 Analysis Routine (IGFCCH48)
6
Appropriate Interception-Dependent Routine
A
B
C
D
E
F
Stand-Alone Seek/Start I/O Interception Routine
Sense Interception Routine
Interrupt Interception Routine
Halt I/O Interception Routine
The appropriate interception-dependent routine first sets the appropriate bit in the ERPIB to show where the channel error occurred. It then branches to ERPIBSET to fill in the ERPIB.
10
When the interception-dependent routine receives control back from ERPIBSET, it passes control to UCB Search.
11
UCB Search Routine
Completes the inboard record by filling in up to eight addresses of active units on the failing channel.
If system termination is necessary, insures that an inboard record has been completed before giving control to MCH to write record and place system in wait state.
12
I/O Supervisor
UCB Search passes control back to the I/O Supervisor for the outboard recorder routine to write the inboard record on SYS1.LOGREC and to issue operator awareness message IFB002I. The I/O Supervisor can then schedule an error recovery procedure.

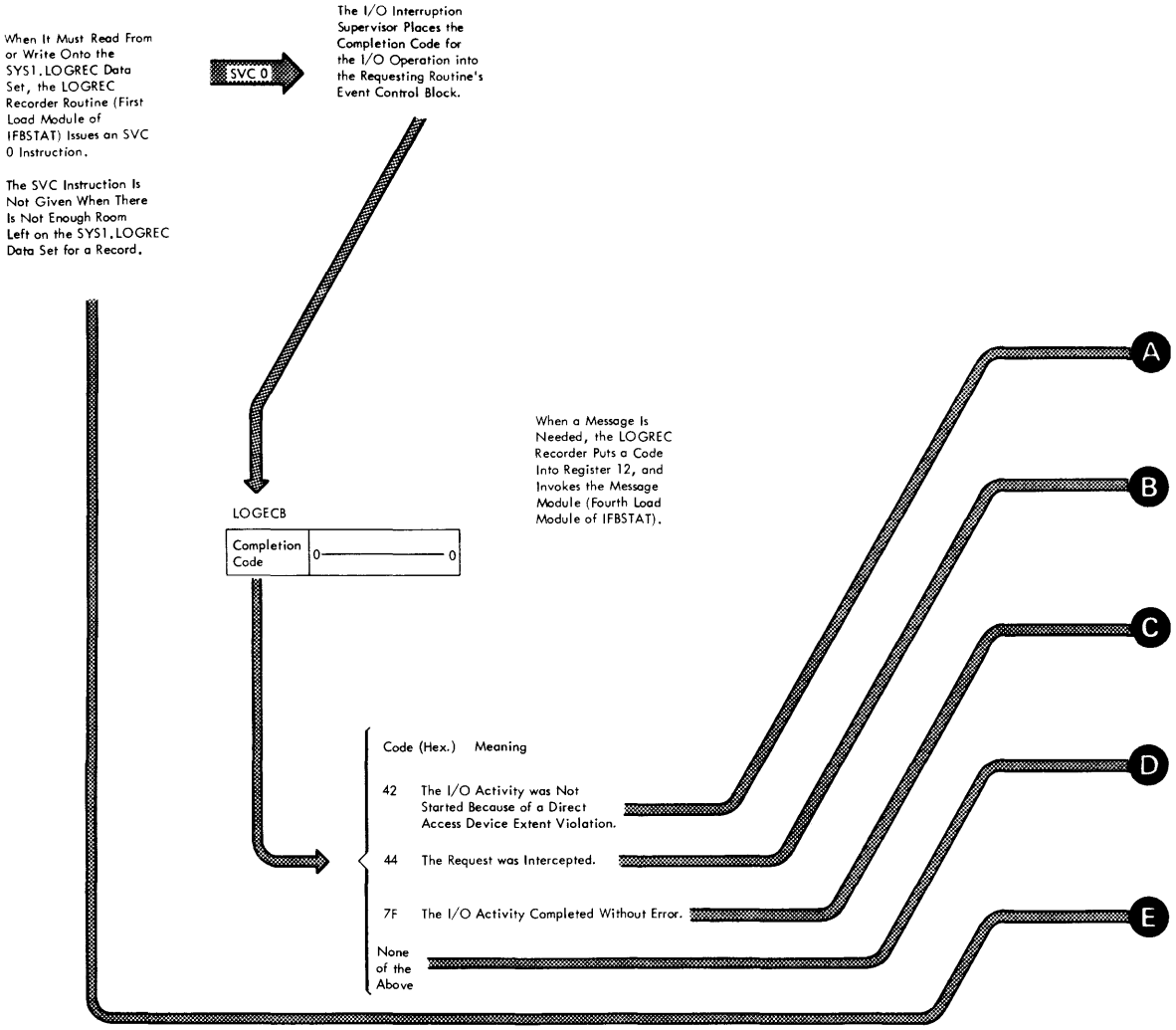
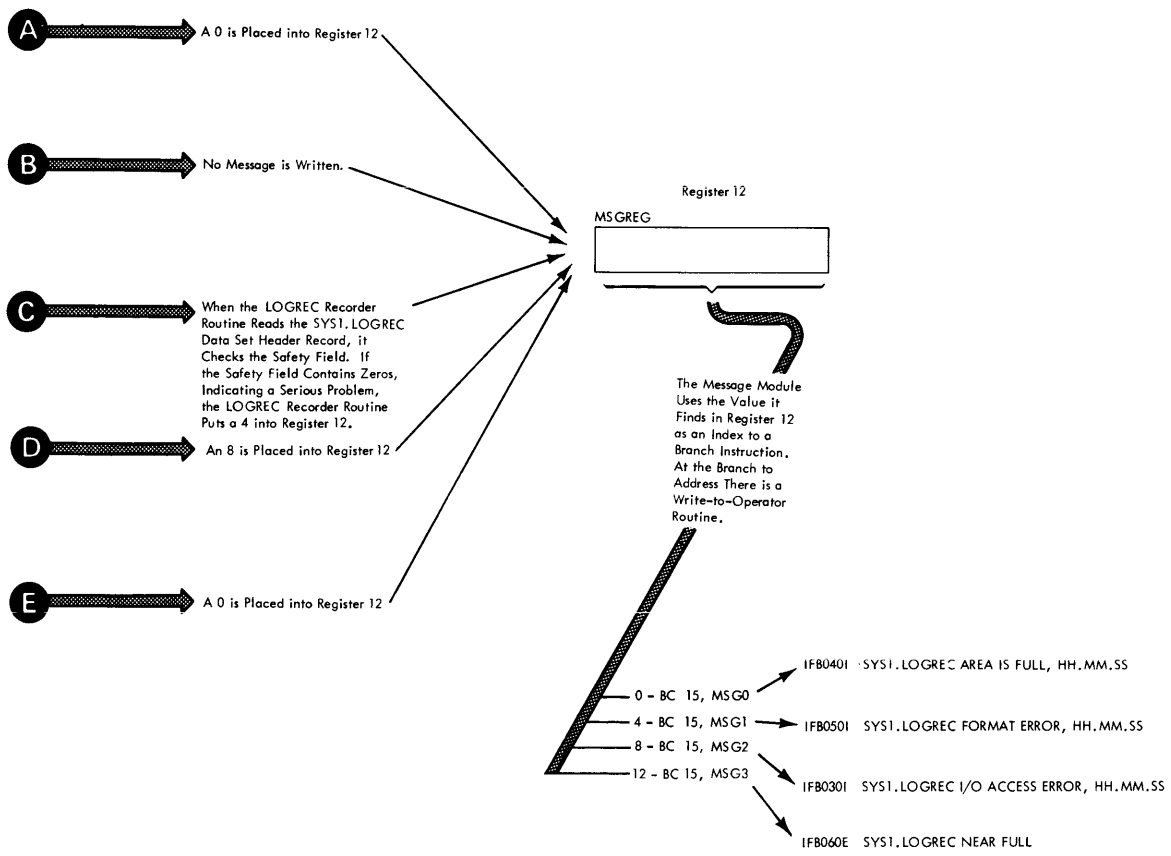


Diagram 15. Writing Environment Recording Error Messages to the Operator


A
A 0 is Placed into Register 12
B
No Message is Written.
C
When the LOGREC Recorder Routine Reads the SYS1.LOGREC Data Set Header Record, it Checks the Safety Field. If the Safety Field Contains Zeros, Indicating a Serious Problem, the LOGREC Recorder Routine Puts a 4 into Register 12.
D
An 8 is Placed into Register 12
E
A 0 is Placed into Register 12
Register 12
MSGREG
The Message Module Uses the Value it Finds in Register 12 as an Index to a Branch Instruction. At the Branch to Address There is a Write-to-Operator Routine.
0 - BC 15, MSG0
4 - BC 15, MSG1
8 - BC 15, MSG2
12 - BC 15, MSG3
IFB040I SYS1.LOGREC AREA IS FULL, HH.MM.SS
IFB050I SYS1.LOGREC FORMAT ERROR, HH.MM.SS
IFB030I SYS1.LOGREC I/O ACCESS ERROR, HH.MM.SS
IFB060E SYS1.LOGREC NEAR FULL

SECTION 3: PROGRAM ORGANIZATION

Functional Organization Chart

Flowcharts

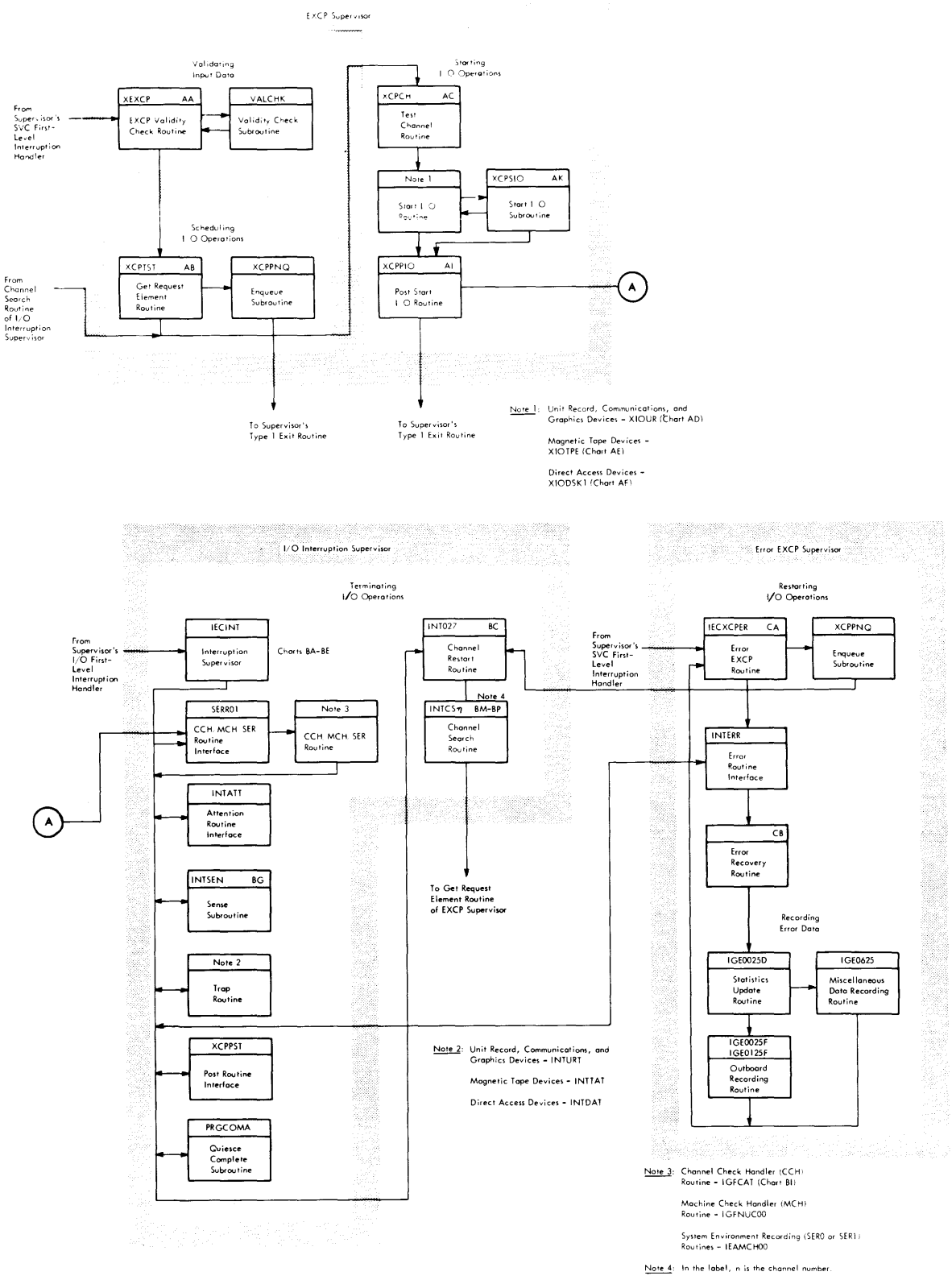


Figure 12. Functional Organization of the I/O Supervisor

Functional Organization Chart

In Figure 12, the major I/O supervisor routines are grouped according to the functions that they perform. Brief descriptions of the routines shown in the figure follow.

Abnormal end appendage: Optional user–written appendage to which the I/O interruption supervisor exits when there is an error associated with the processing of I/O.

Attention Routine Interface: Determines the address of the appropriate Attention routine; invokes the Attention routine.

Channel Check Handler routine: Builds error recovery procedure interface block to indicate cause of channel failure; builds inboard record to describe environment at time of failure.

Channel Check Handler Routine Interface (Channel Check Handler only): Places a code into register 15 that indicates which IOS routine intercepted the channel failure and branches to the Channel Check Handler routine.

Channel end appendage: Optional user–written appendage to which the I/O interruption supervisor exits after a channel end interruption before indicating to the user how his I/O request ended. Also entered when channel end interruption is accompanied by either a wrong length indicator or a unit exception, or by both conditions.

Channel Restart routine: Scans logical channel queues. Selects RQEs representing requests for I/O activity that can be started. Starts the I/O activity. For direct access devices, first starts all seeks, then starts the data transfer.

Channel Search routines: One for every physical channel. "Driver" type routines consisting mostly of branch instructions. Direct the search of logical channel queues and the starting of I/O activity.

Dequeue subroutine: Locates an RQE in a logical channel queue, removes it from the queue, and returns it to the freelist.

End–of–extent appendage: Optional user–written appendage to which the EXCP supervisor exits when the execution of I/O request will violate the extent limits of a direct–access device.

Enqueue subroutine: Places an RQE into a logical channel queue. Normally queues by order of arrival. Optionally queues by requestor's priority or by seek address.

Error Recovery routine: Determines if I/O activity can be retried. Supervises retry attempts.

Error Routine Interface: Prepares for and invokes, or schedules the execution of, an error recovery routine.

EXCP Validity Check routine: Does most of the housekeeping for the EXCP supervisor. Checks for a valid DCB, DEB, IOB, and UCB. With Protection feature and MVT option, uses Validity Check subroutine to check storage keys of input data areas.

Get Request Element routine: Obtains an RQE from the freelist and initializes it. If device is unavailable, causes the RQE to be queued.

Miscellaneous Data Recording routine: Generates miscellaneous error environment records for buffered log devices 2305, 3211, and 3330, and for 2715 error data.

Outboard Recorder routine: Builds outboard record to describe environment at time of I/O device failure. Writes outboard record onto SYS1.LOGREC data set.

Program–controlled interruption appendage: Optional user–written appendage to which I/O interruption supervisor exits whenever a program--controlled interruption (PCI) is indicated. Returns control to I/O interruption supervisor where normal processing continues.

Post Routine Interface: Invokes the supervisor's Post routine, passing to it an event completion code and the address of the requestor's ECB. The Post routine posts the requestor's ECB.

Post Start I/O routine: Routes control, depending upon resulting condition codes of the Start I/O instruction and status bits in the CSW (if the CSW was stored).

Quiesce Complete subroutine: Invokes the supervisor's Post routine, passing to it an event completion code and the address of the purge parameter list. The Post routine posts the Purge routine ECB.

Sense subroutine: Issues a Start I/O instruction to cause a Sense command to be executed. Places the first two bytes of sense data in the requestor's IOB.

SER Routine Interface: Places an error code into the machine check new PSW. Uses a Load PSW instruction to invoke the SER0 or SER1 routine. For the Model 65, invokes the Machine Check Handler routine.

Start I/O appendage: Optional user–written routine to which the EXCP supervisor exits before the execution of the Start I/O (SIO) instruction for a requested I/O operation.

Start I/O routine for direct–access devices: Prepares an I/O supervisor channel program consisting of three CCWs: a Seek command, a Set File Mask command, and a Transfer–in–Channel command. Uses the Start I/O subroutine twice, once to perform the seek and once to perform the data transfer.

Start I/O routine for magnetic–tape devices: Prepares an I/O supervisor channel program that may consist of two CCWs (normal start, restart, or opposite direction recovery), or three CCWs (operations following a cyclic redundancy check condition). The last CCW contains a Transfer–in–Channel command containing the address of the requestor's first CCW. Uses the Start I/O subroutine.

Start I/O routine for unit record and communications devices: Prepares a one–CCW channel program consisting of a Transfer–in–Channel command containing the address of the requestor's first CCW. Uses the Start I/O subroutine.

Start I/O subroutine: Prepares the CAW and issues a Start I/O instruction. Does some checking of resulting condition codes.

Statistics Update routine: Updates counters in statistics table entry for failing device.

Test Channel routine: For selector channels, issues a Test Channel instruction. Causes the RQE to be queued if the channel is unavailable. Tries all channels of multiple–path arrangements. Does not issue a Test Channel instruction for byte–multiplexor channels.

Trap routines: One for each device class. Perform device–dependent functions following channel end and device end interruptions.

Validity Check subroutine: MVT only. Checks storage keys of areas containing IOB, DCB, and ECB against the requestor's protection key; checks that DEB storage key is 0.

Flowcharts

This section contains flowcharts of I/O supervisor routines. In general, the flowcharts have the following characteristics:

- Normal, 'no–error' type processing is shown vertically. To follow normal processing, read down a flowchart.
- Symbols, or labels, are used where possible to aid readers in locating instruction sequences in listings. However, in cases where an instruction sequence does not have an associated label, a nearby label is sometimes used in the chart to indicate *approximately* where in the listing the function is performed.
- Optional features are outlined to make them stand out. Where an option was not included in a generated system, read through the optional feature blocks; the corresponding instructions will most likely not appear in the program listings.
- Where CPU control passes from one routine or subroutine to another, terminal blocks are always used. Offpage connectors are used only when a single routine or subroutine extends over two or more pages.
- Redundancy is sometimes used to avoid excessive cross referencing; the same function may sometimes be shown in two or more flowcharts, even though in each case it is performed with the same set of instructions.

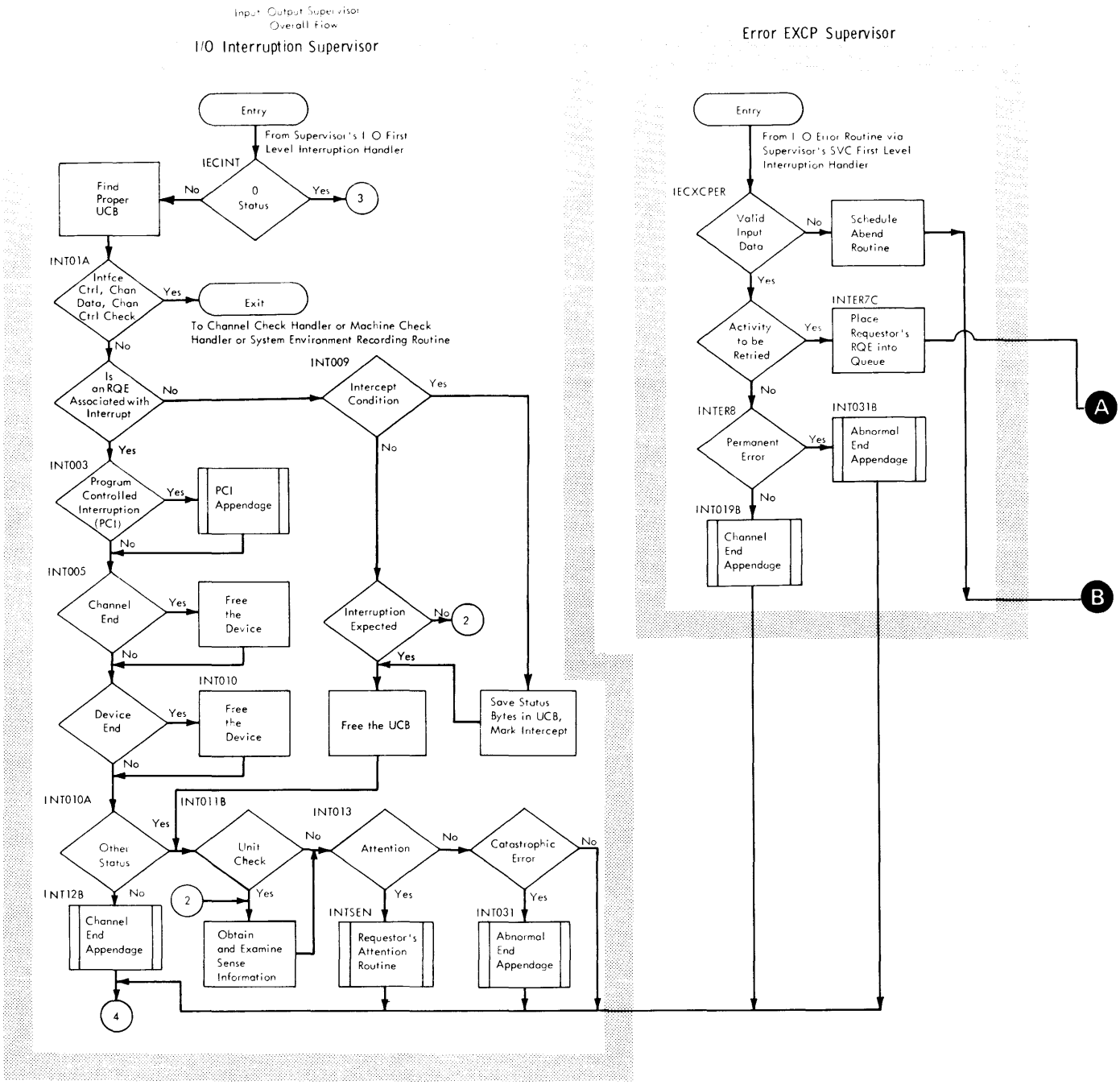
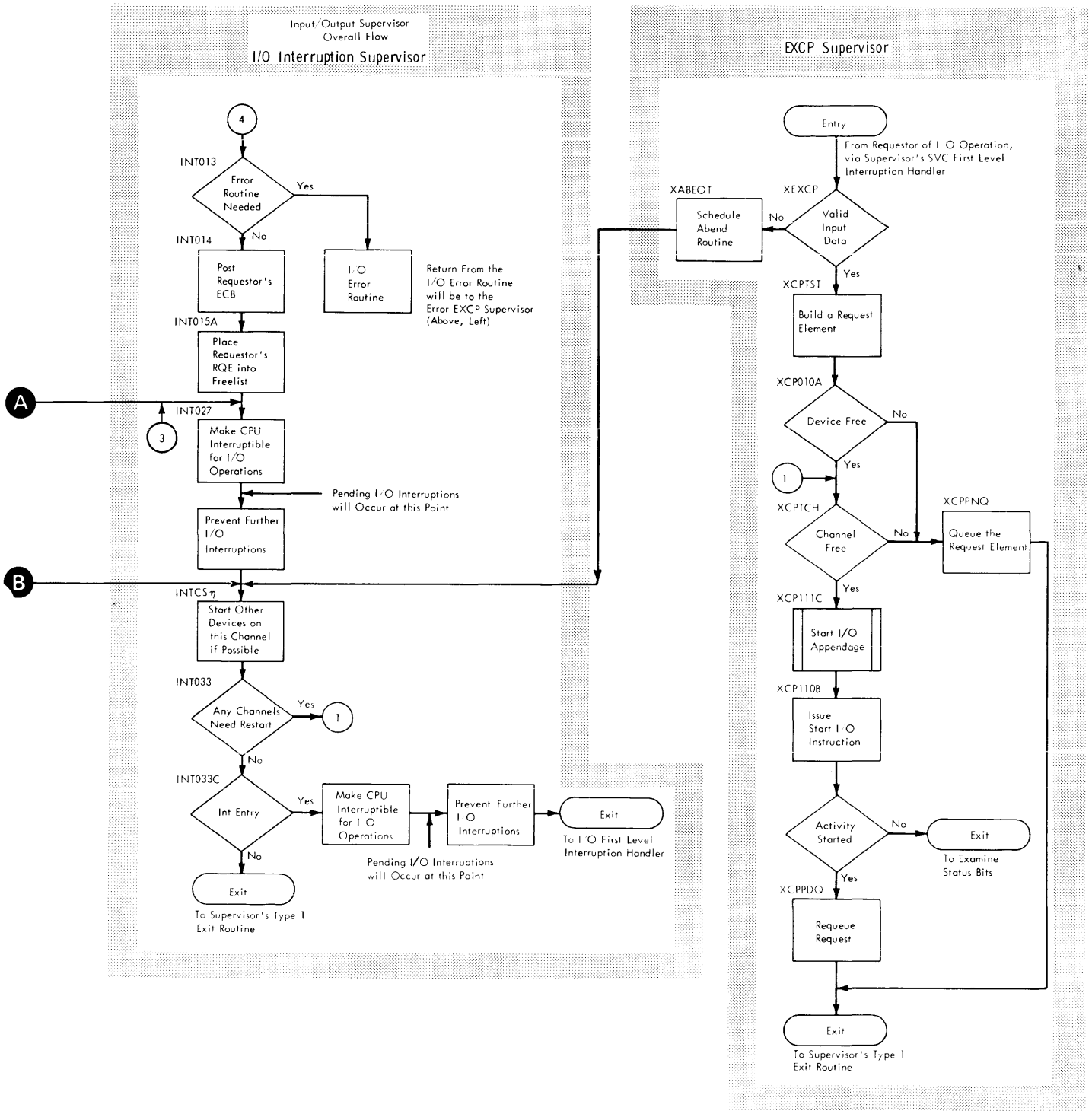


Chart 00. Input/Output Supervisor Overall Flow


Input/Output Supervisor
Overall Flow
I/O Interruption Supervisor
EXCP Supervisor
4
INT013
Error Routine Needed
Yes
No
INT014
Post Requestor's ECB
I/O Error Routine
Return From the I/O Error Routine will be to the Error EXCP Supervisor (Above, Left)
INT015A
Place Requestor's RQE into Freelist
A
INT027
3
Make CPU Interruptible for I/O Operations
Pending I/O Interruptions will Occur at this Point
Prevent Further I/O Interruptions
B
INTCSη
Start Other Devices on this Channel if Possible
INT033
Any Channels Need Restart
Yes
1
No
INT033C
Int Entry
Yes
Make CPU Interruptible for I/O Operations
Prevent Further I/O Interruptions
Exit
To I/O First Level Interruption Handler
Pending I/O Interruptions will Occur at this Point
No
Exit
To Supervisor's Type 1 Exit Routine
Entry
From Requestor of I/O Operation, via Supervisor's SVC First Level Interruption Handler
XABEOT
Schedule Abend Routine
XEXCP
Valid Input Data
No
Yes
XCPTST
Build a Request Element
XCP010A
Device Free
No
Yes
1
XCPTCH
Channel Free
No
XCPPNQ
Queue the Request Element
Yes
XCP111C
Start I/O Appendage
XCP110B
Issue Start I/O Instruction
Activity Started
No
Exit
To Examine Status Bits
Yes
XCPPDQ
Requeue Request
Exit
To Supervisor's Type 1 Exit Routine

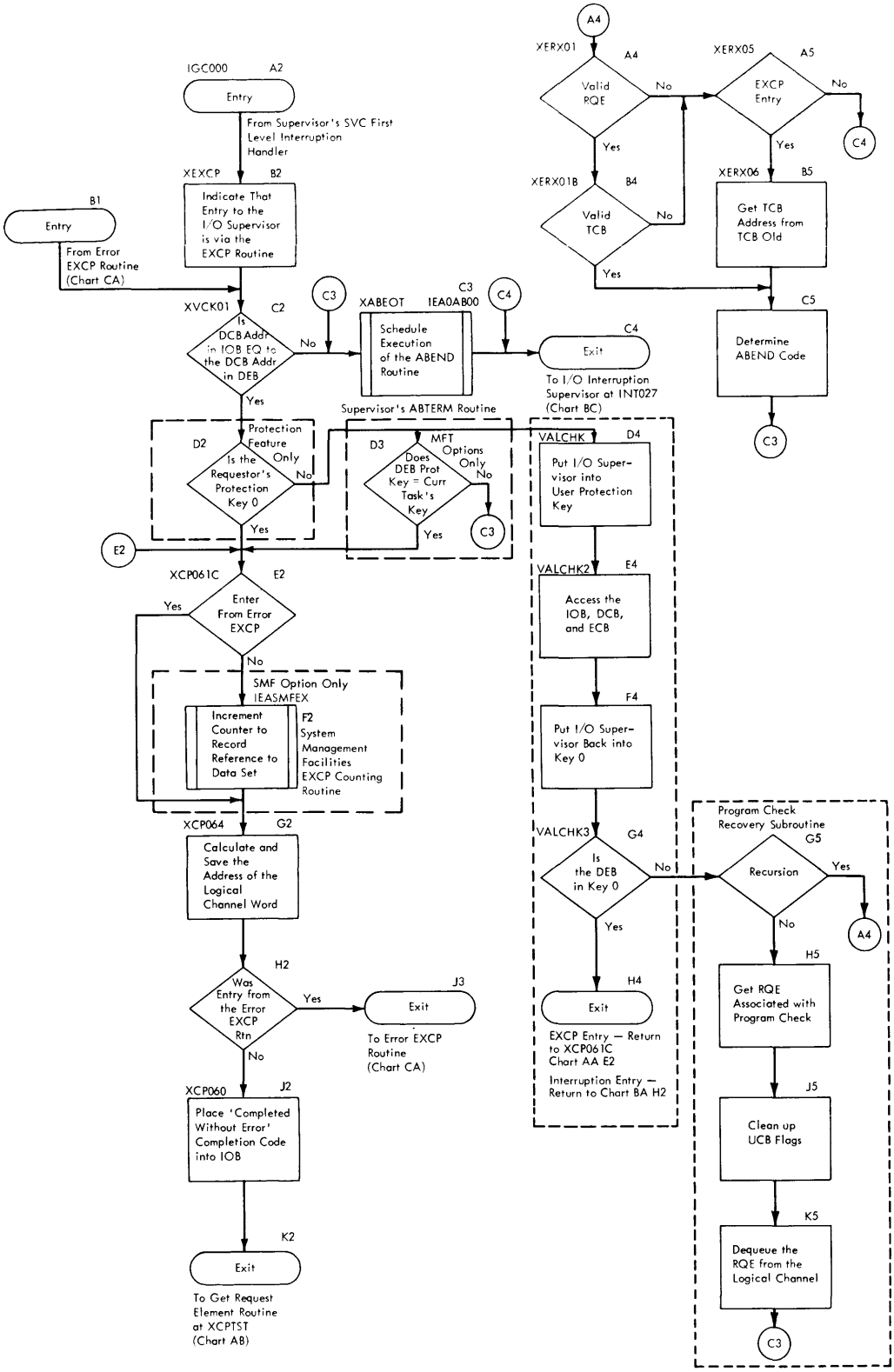


Chart AA. EXCP Validity Check Routine

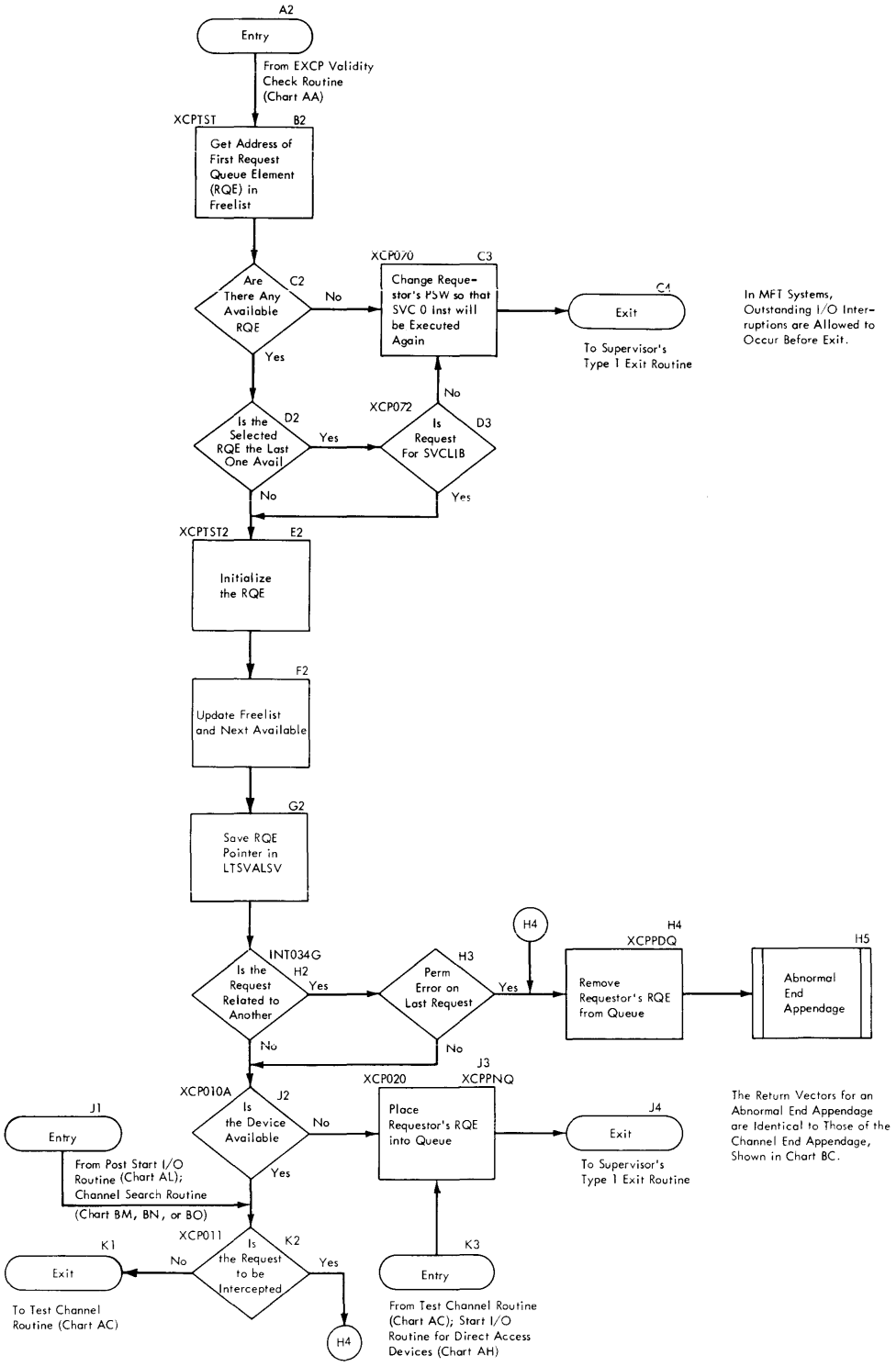


Chart AB. Get Request Element Routine

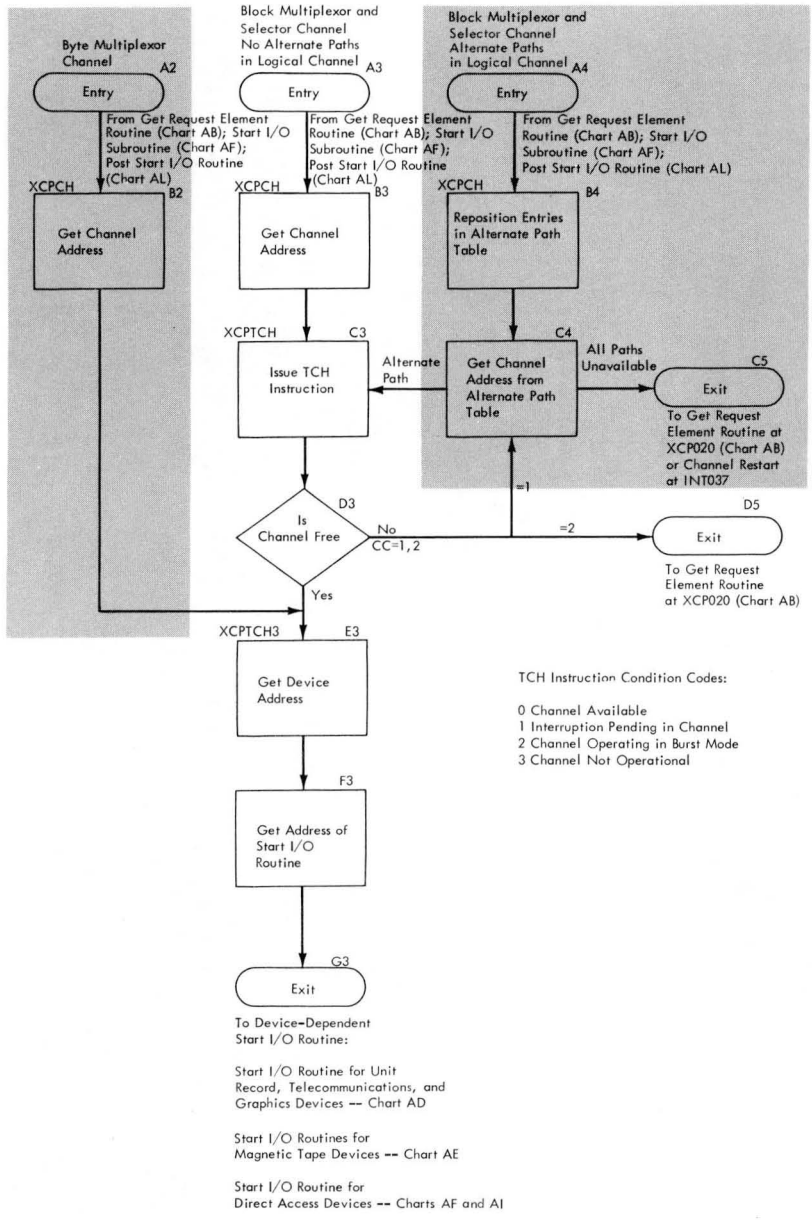


Chart AC. Test Channel Routines

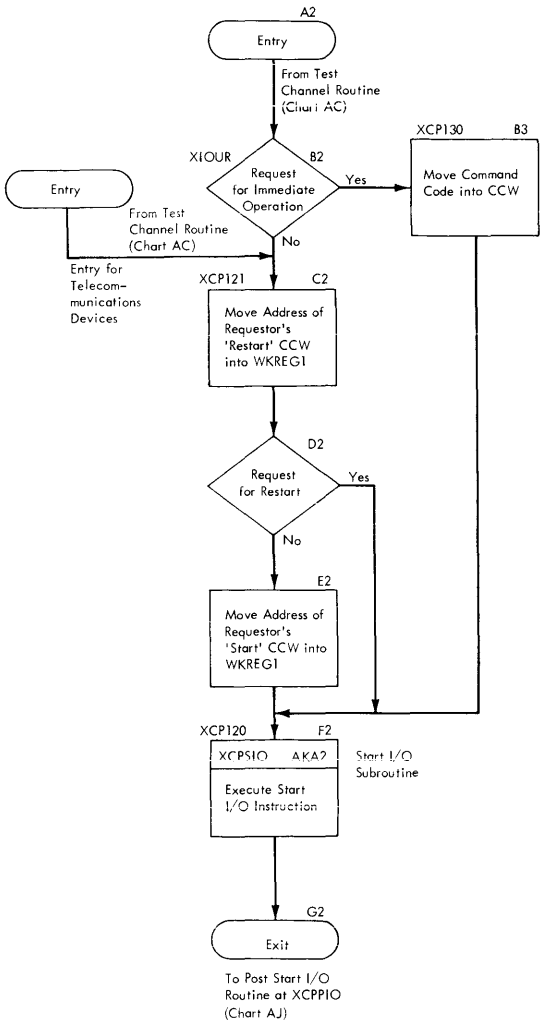


Chart AD. Start I/O Routine for Unit Record, Communications and Graphics Devices

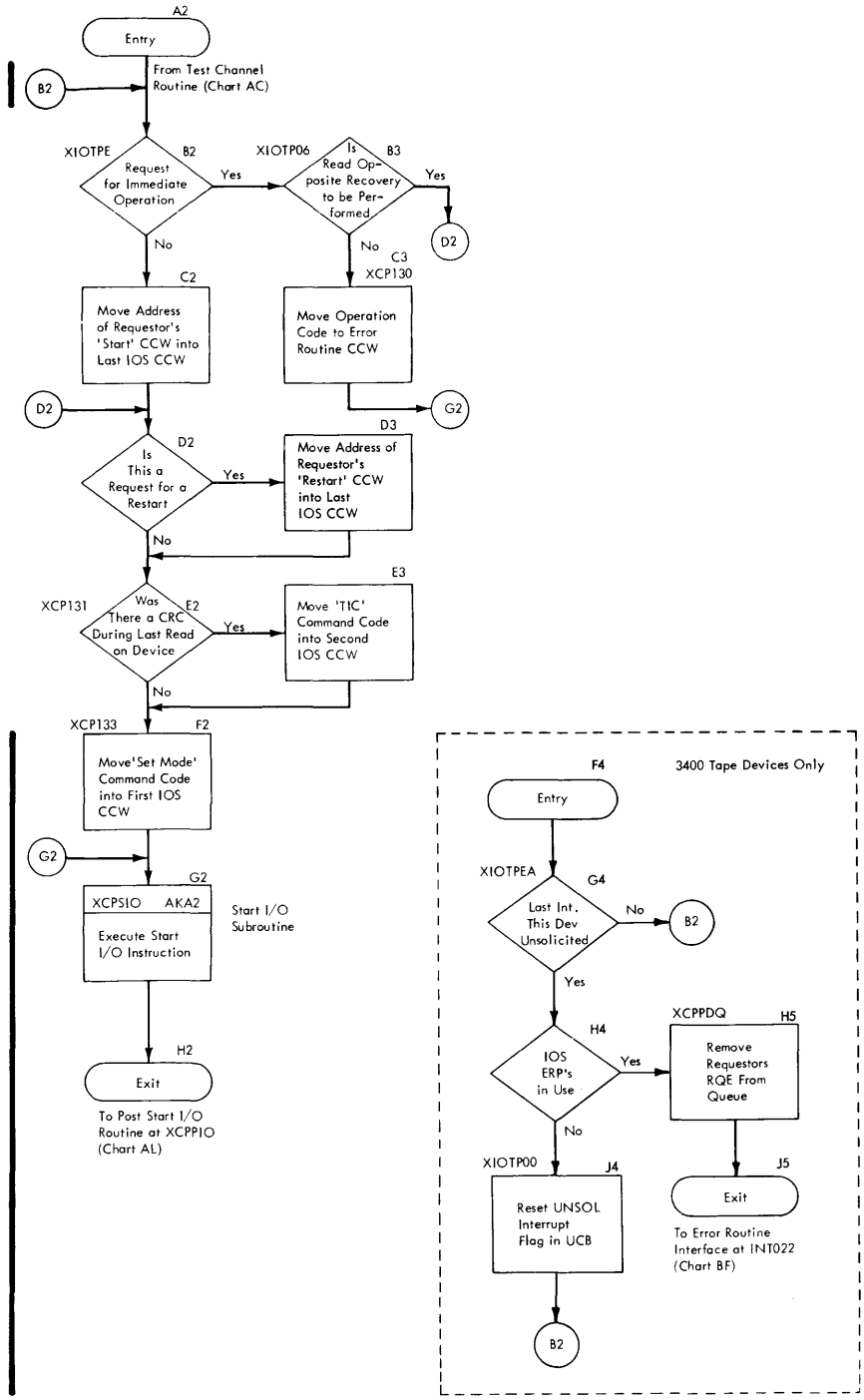


Chart AE. Start I/O Routine for Magnetic Tape Devices

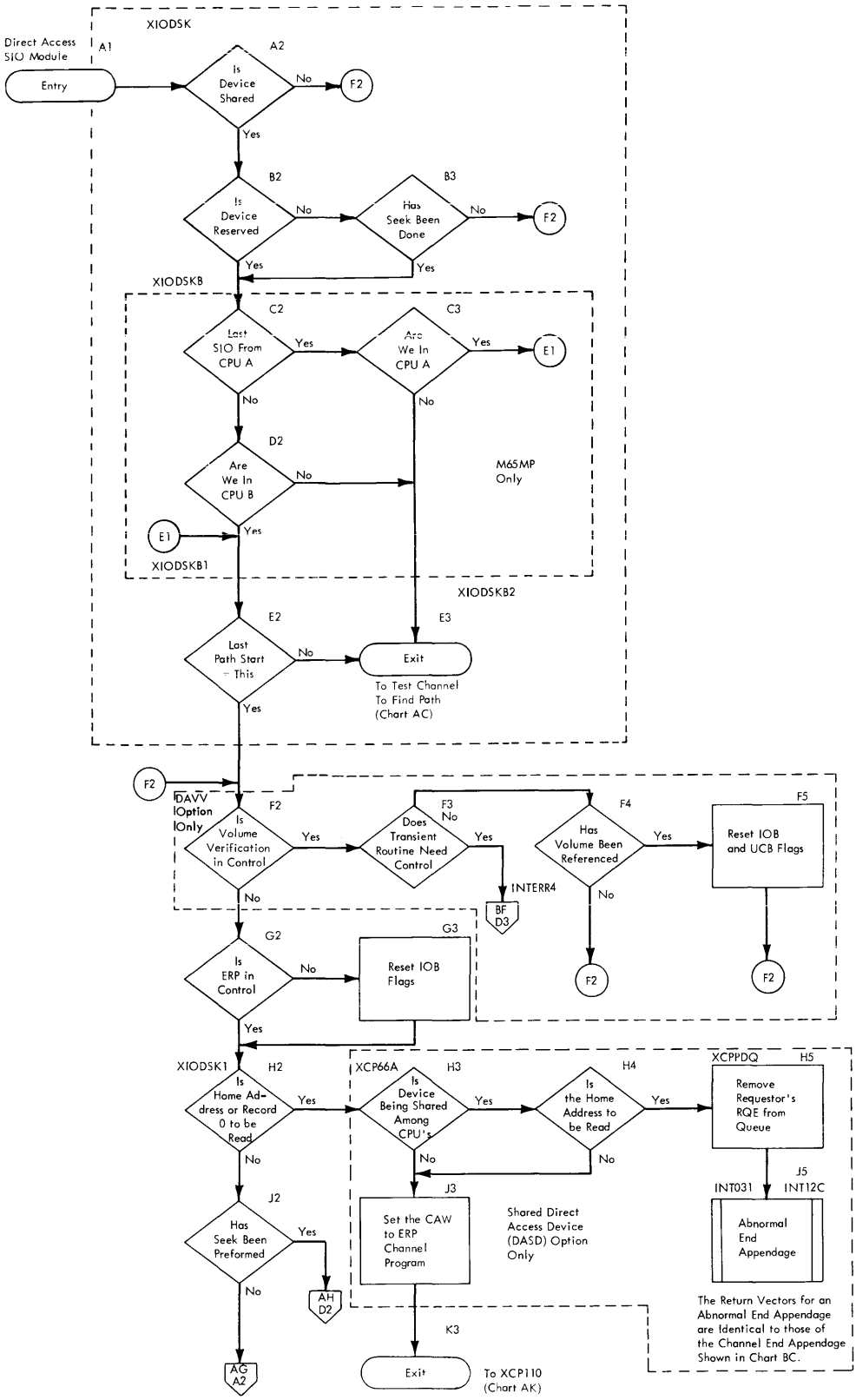


Chart AF (Part 1 of 3). Start I/O Routine for Direct–Access Device

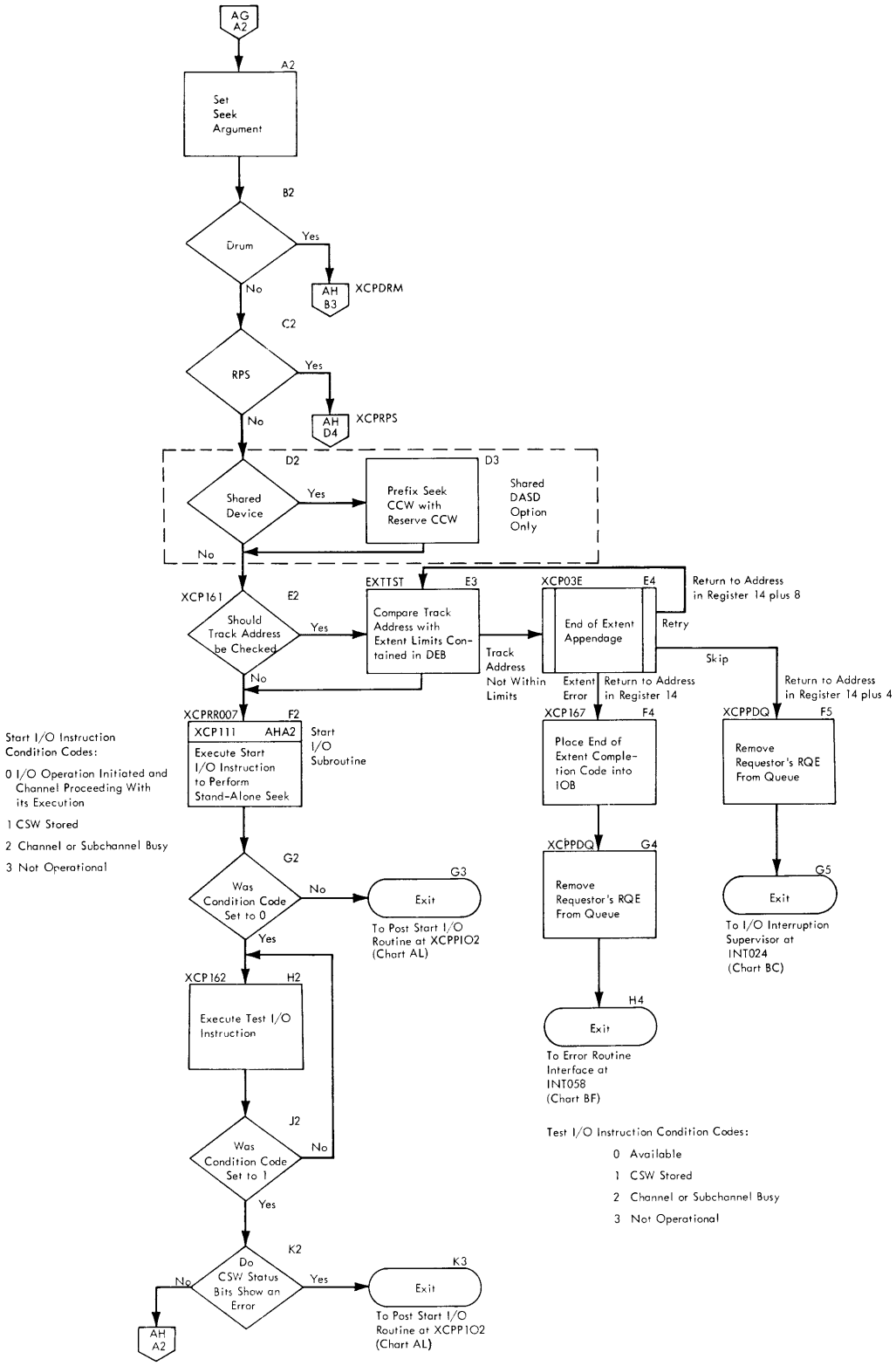


Chart AG (Part 2 of 3). Start I/O Routine for Direct–Access Device

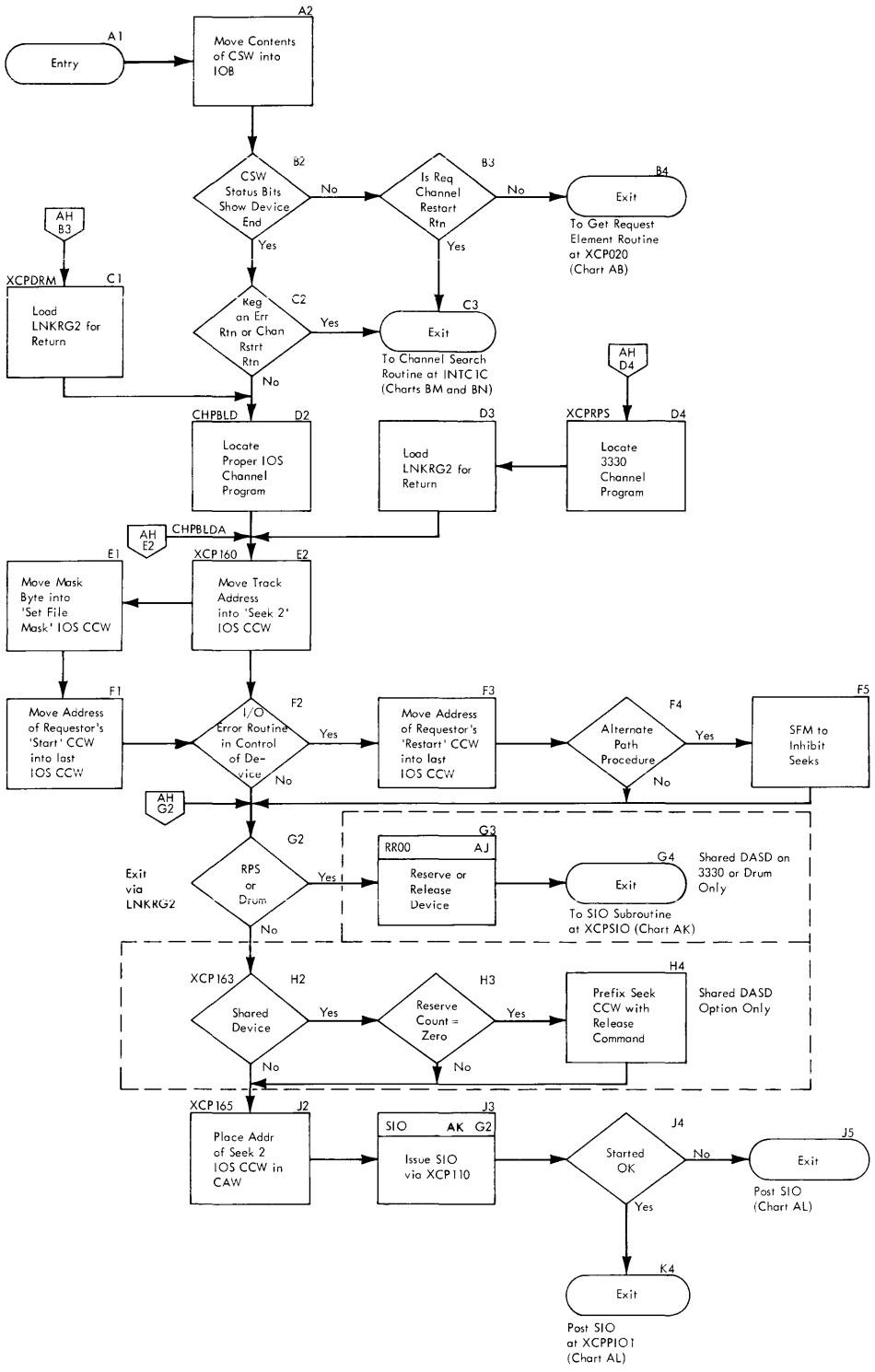


Chart AH (Part 3 of 3). Start I/O Routine for Direct-Access Devices

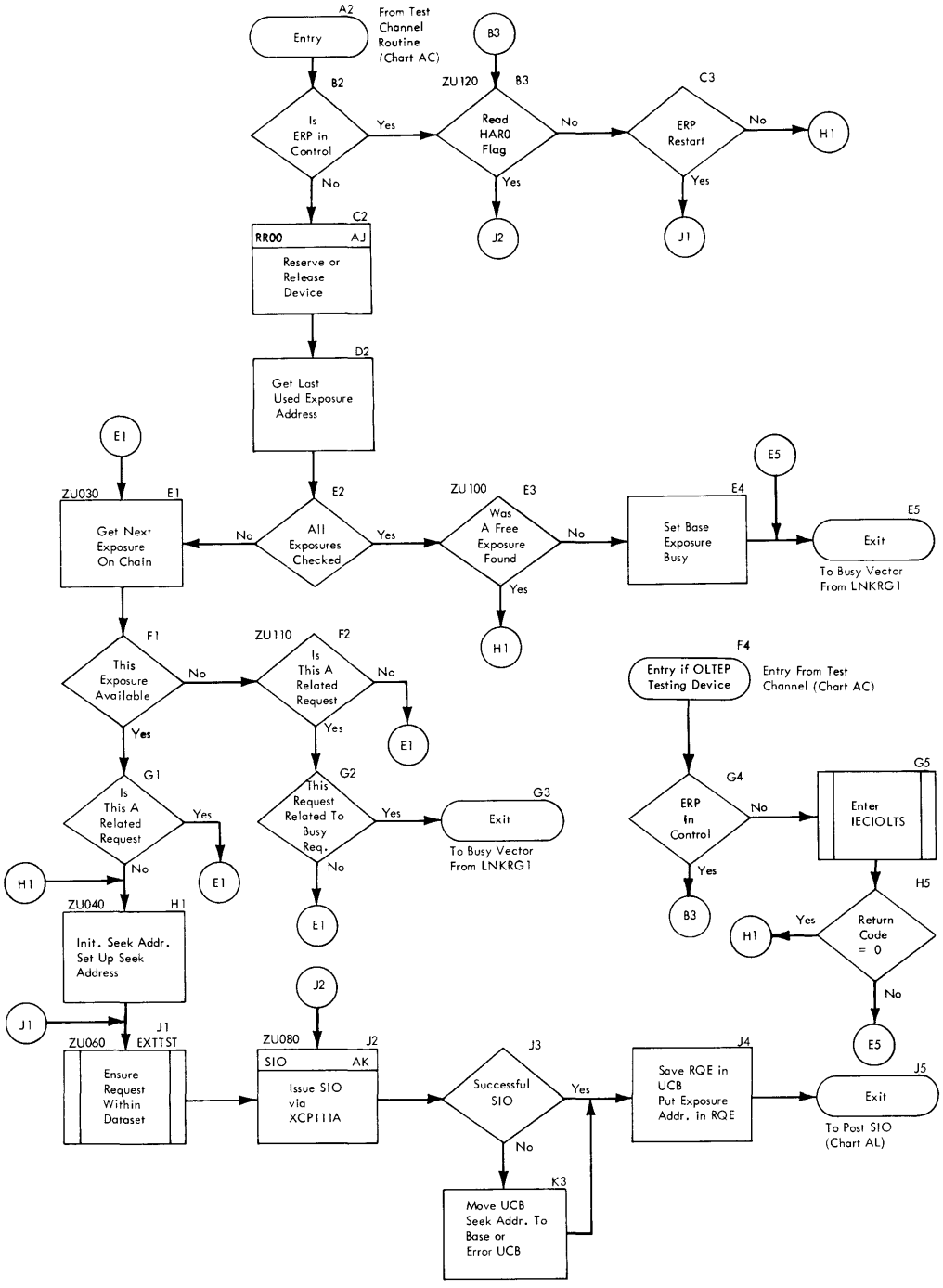


Chart AI. Start I/O Subroutine for 2305

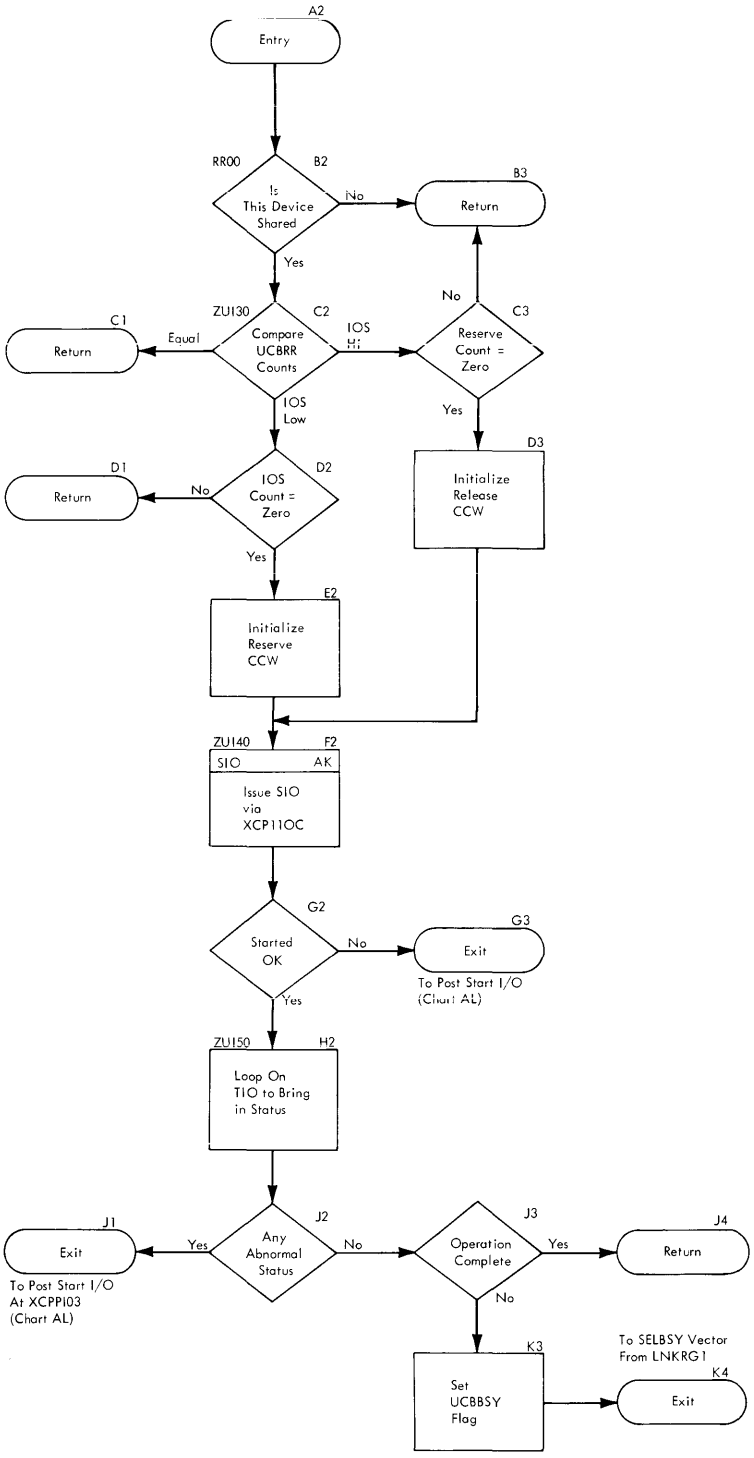


Chart AJ. Shared DASD for Drums and RPS Devices

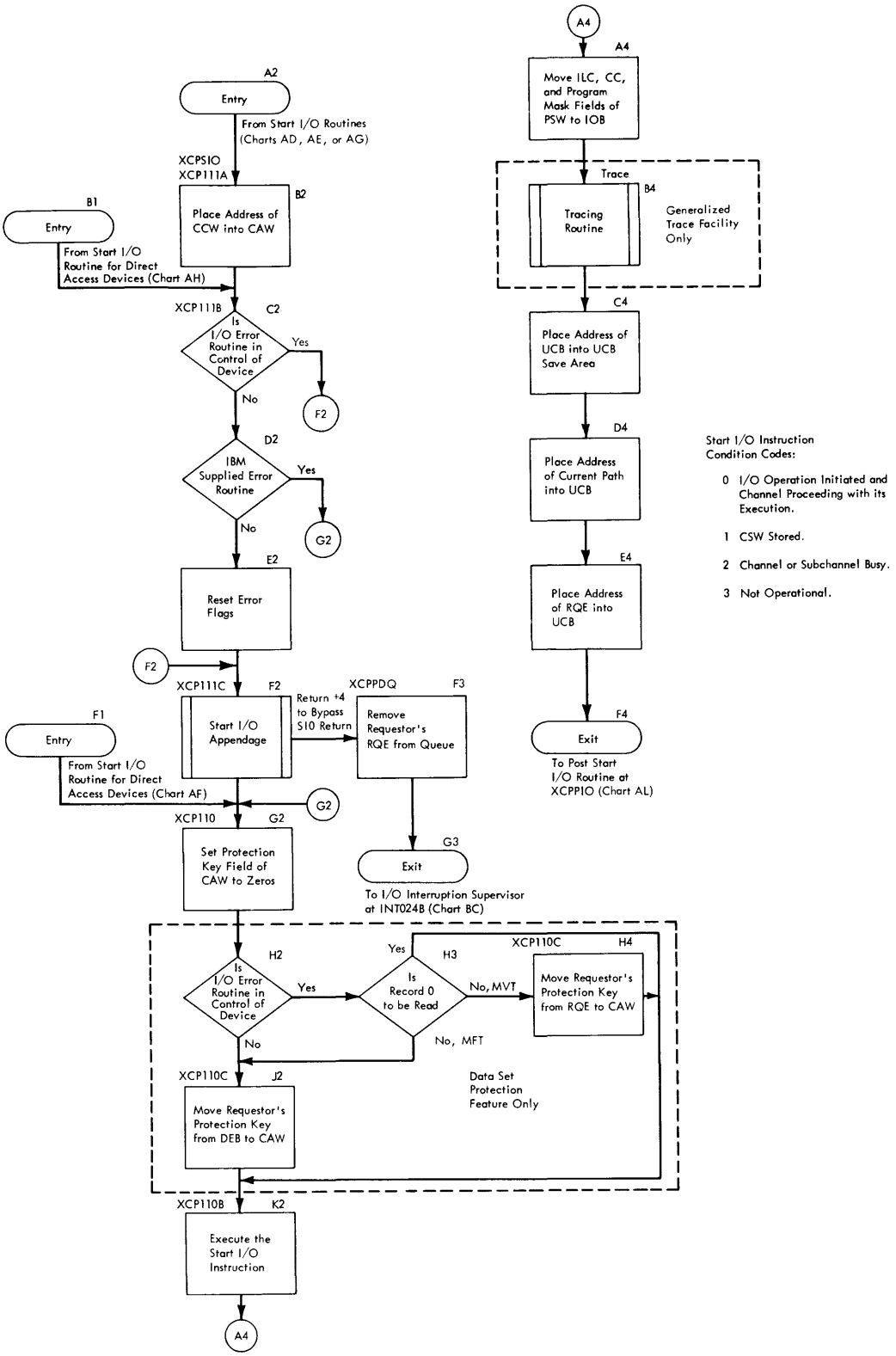


Chart AK. Start I/O Subroutine

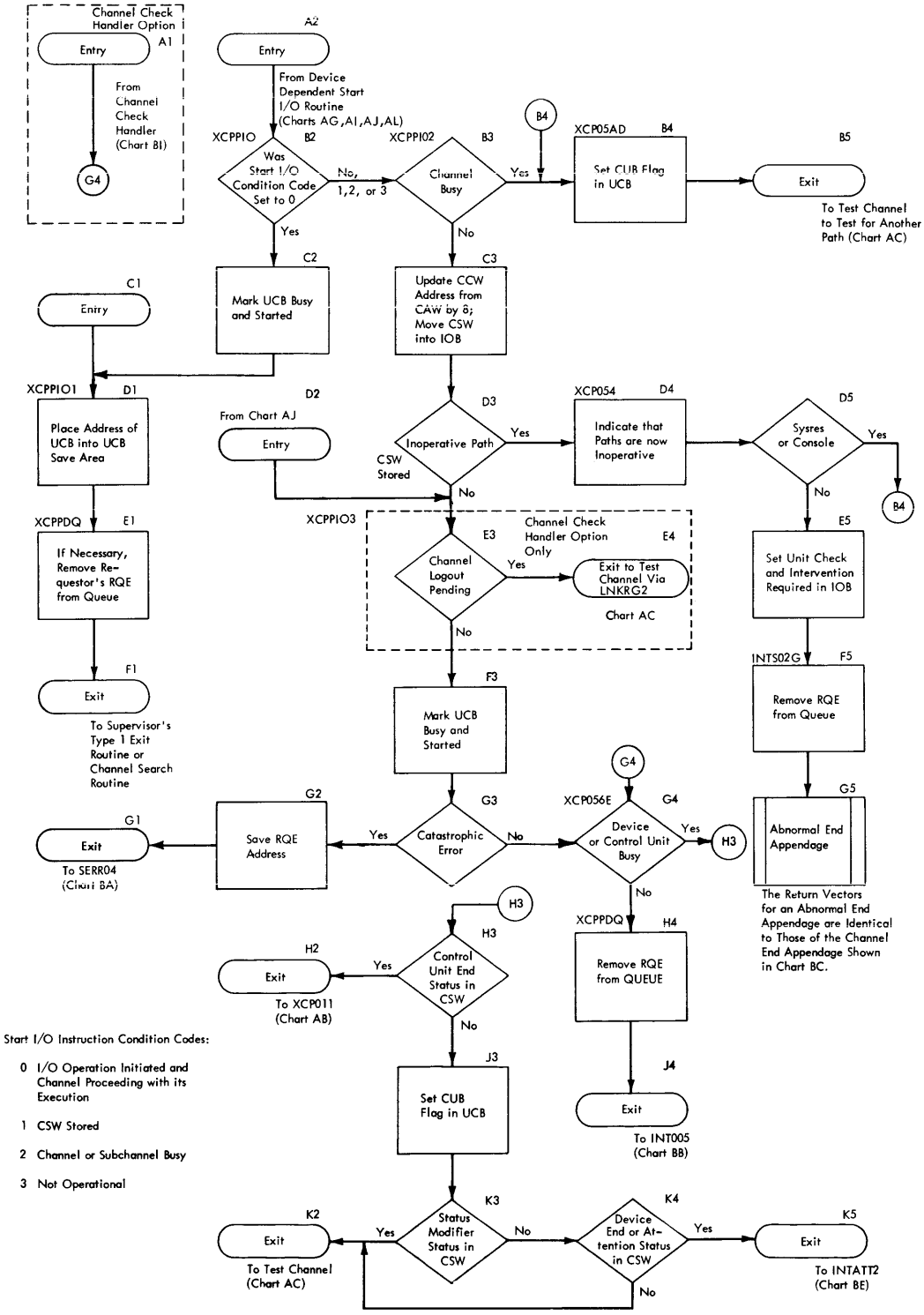


Chart AL. Post Start I/O Routine

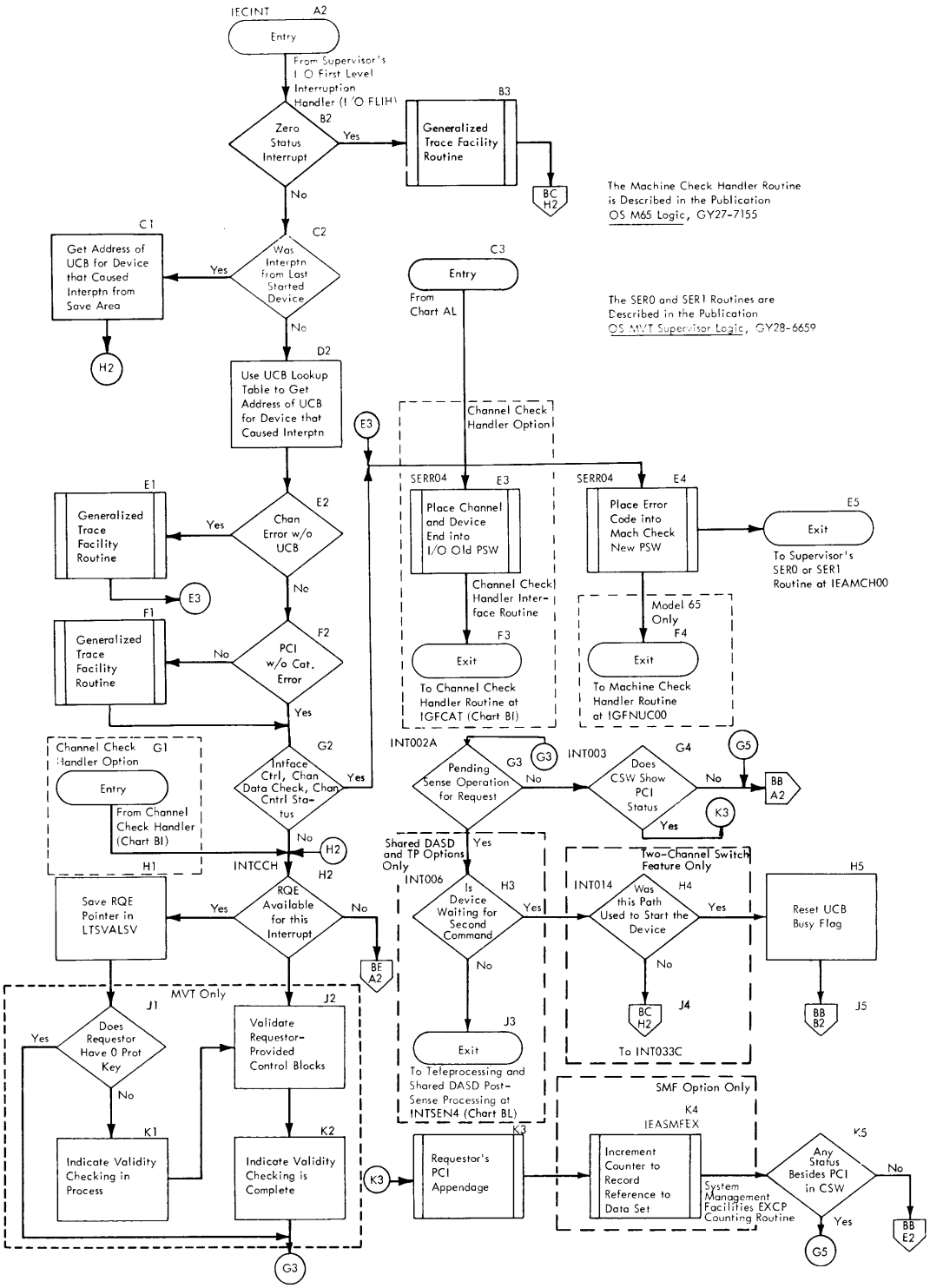


Chart BA (Part 1 of 5). I/O Interruption Supervisor

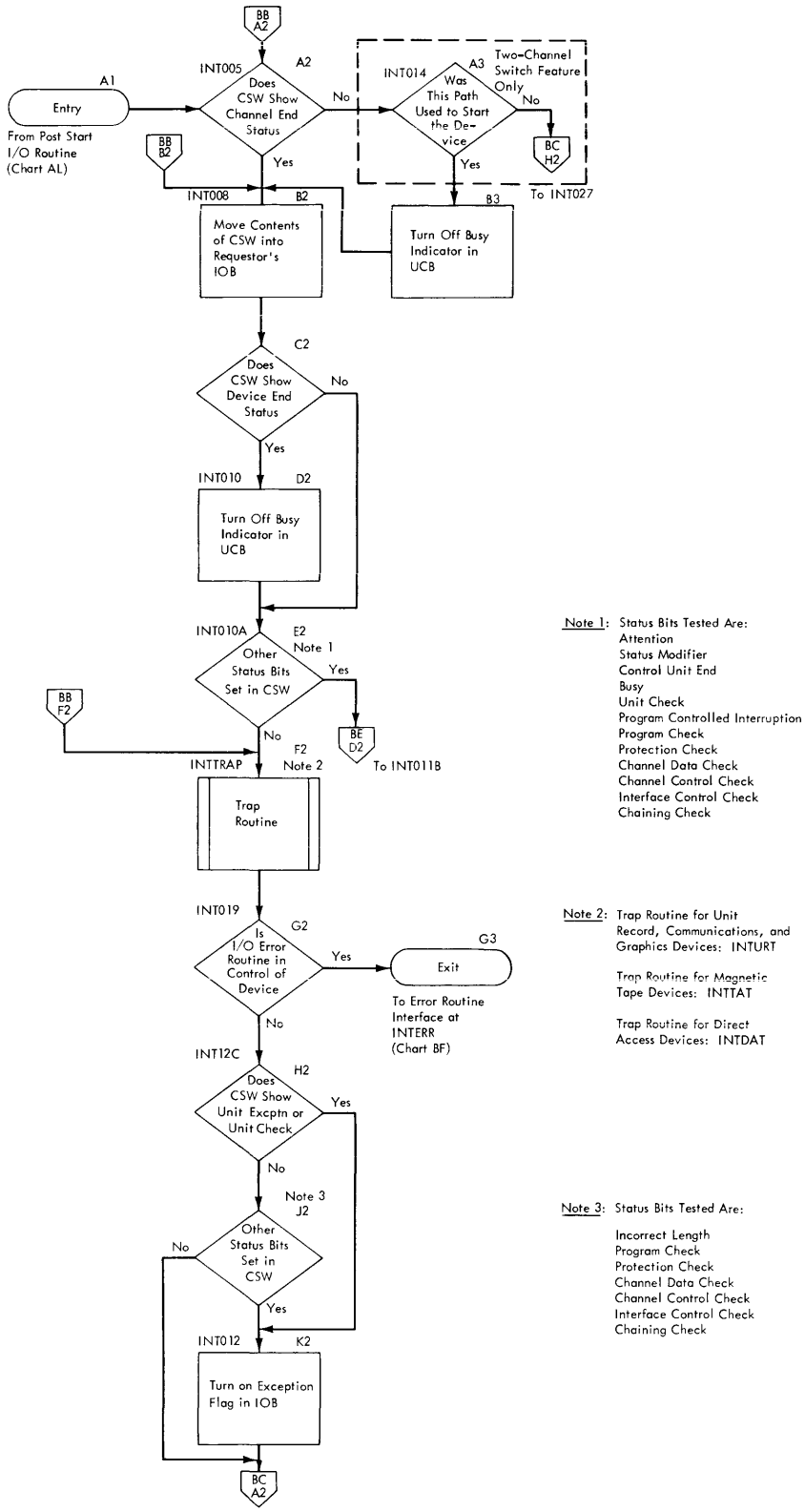


Chart BB (Part 2 of 5). I/O Interruption Supervisor

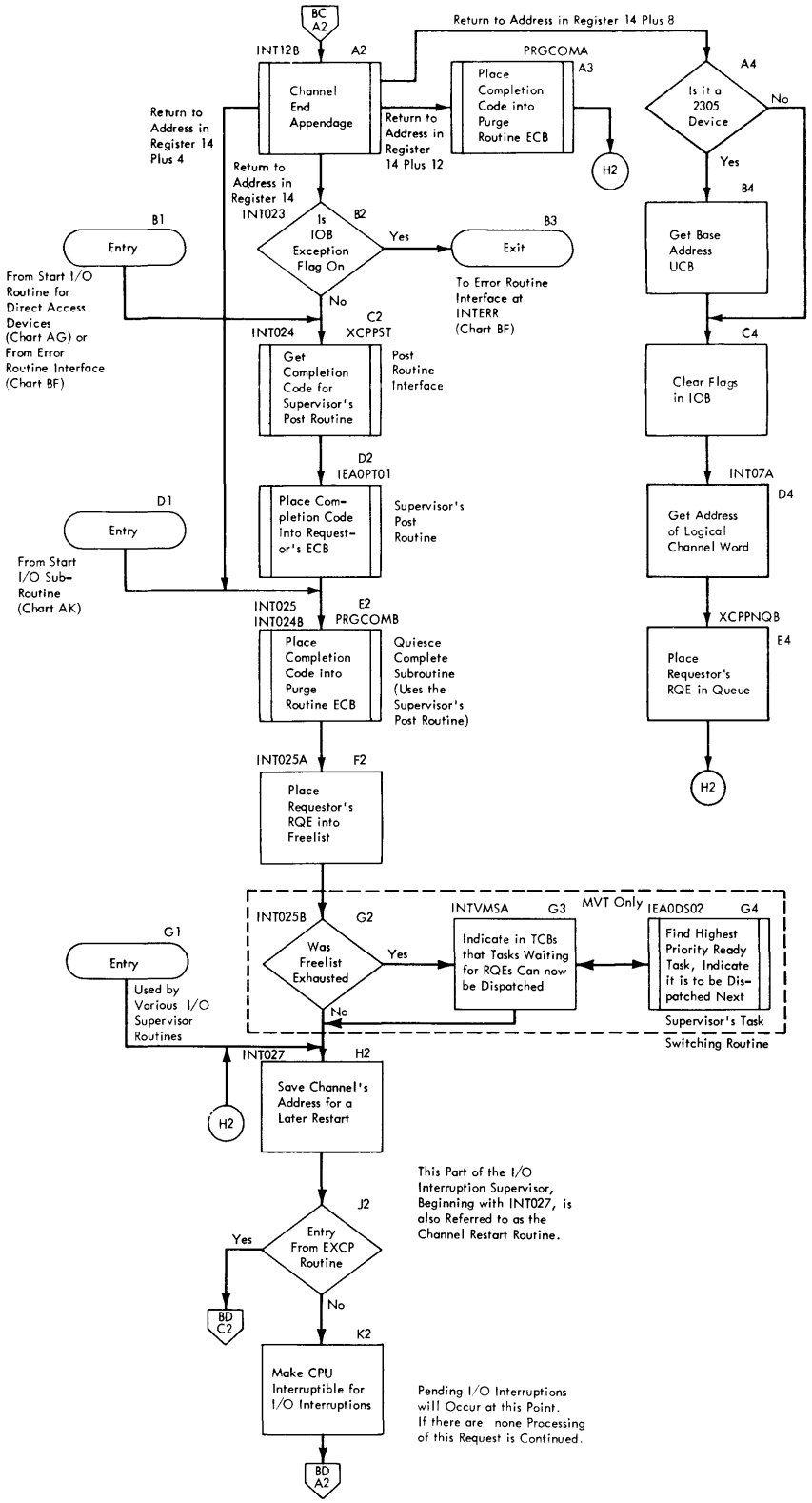


Chart BC (Part 3 of 5). I/O Interruption Supervisor

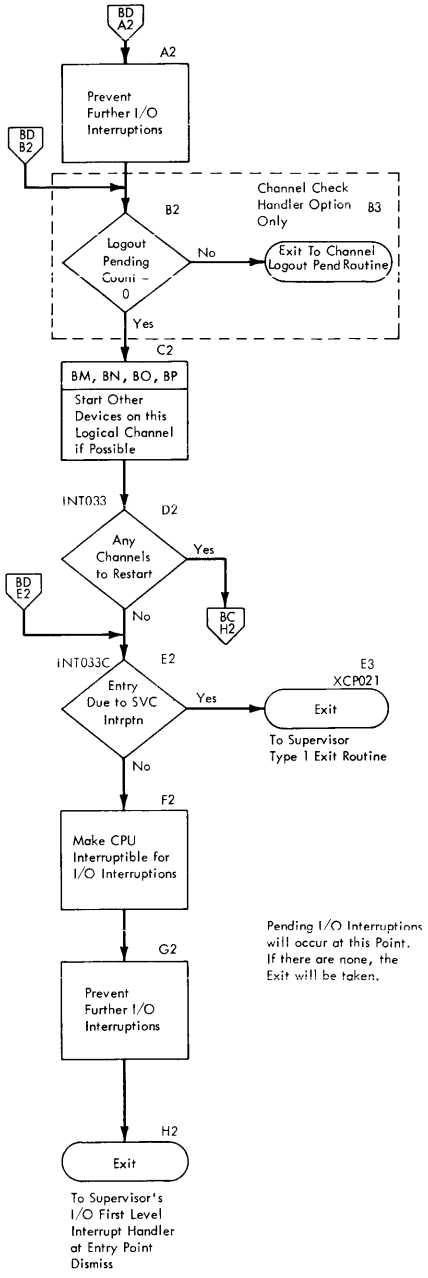


Chart BD (Part 4 of 5). I/O Interruption Supervisor

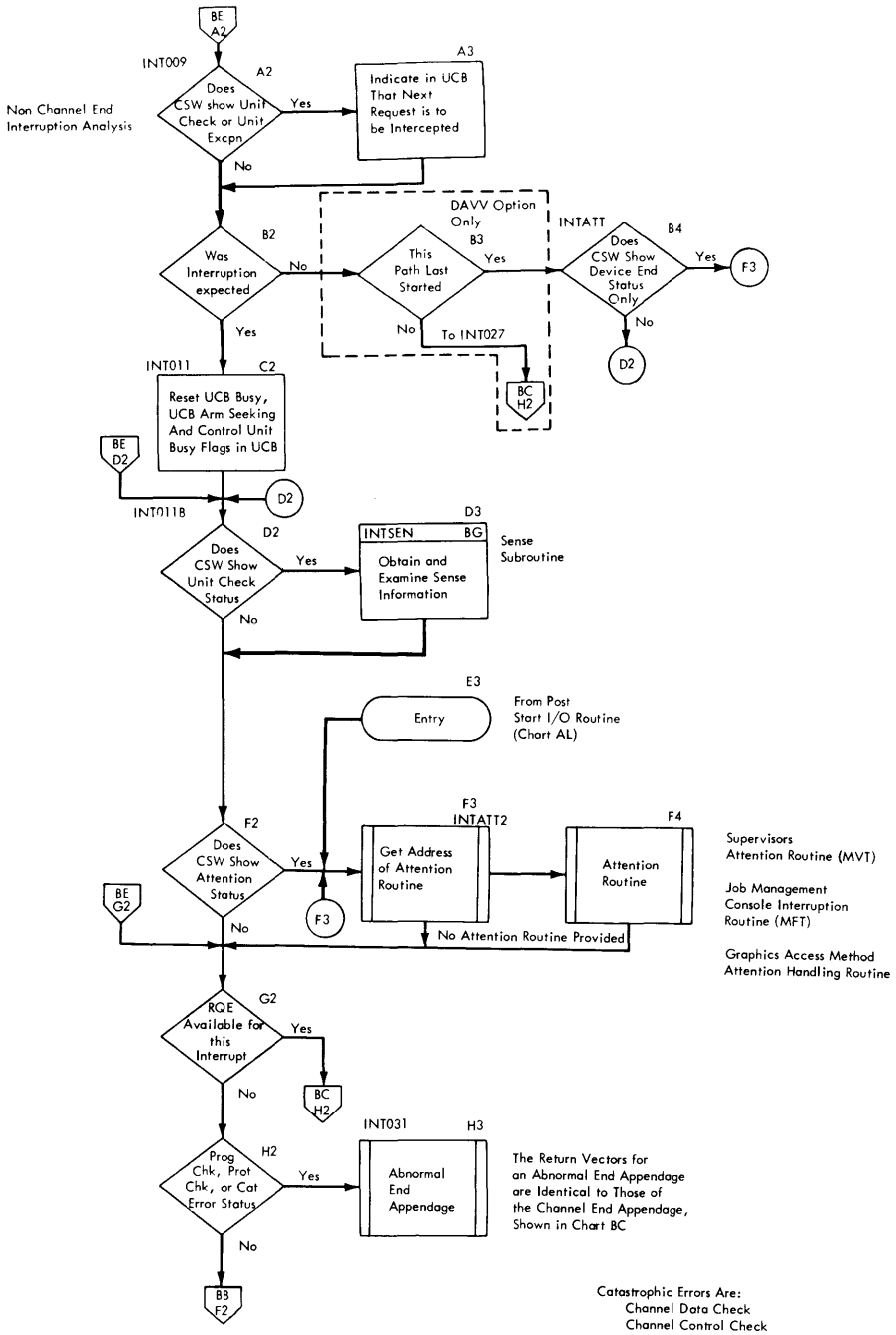


Chart BE (Part 5 of 5). I/O Interruption Supervisor

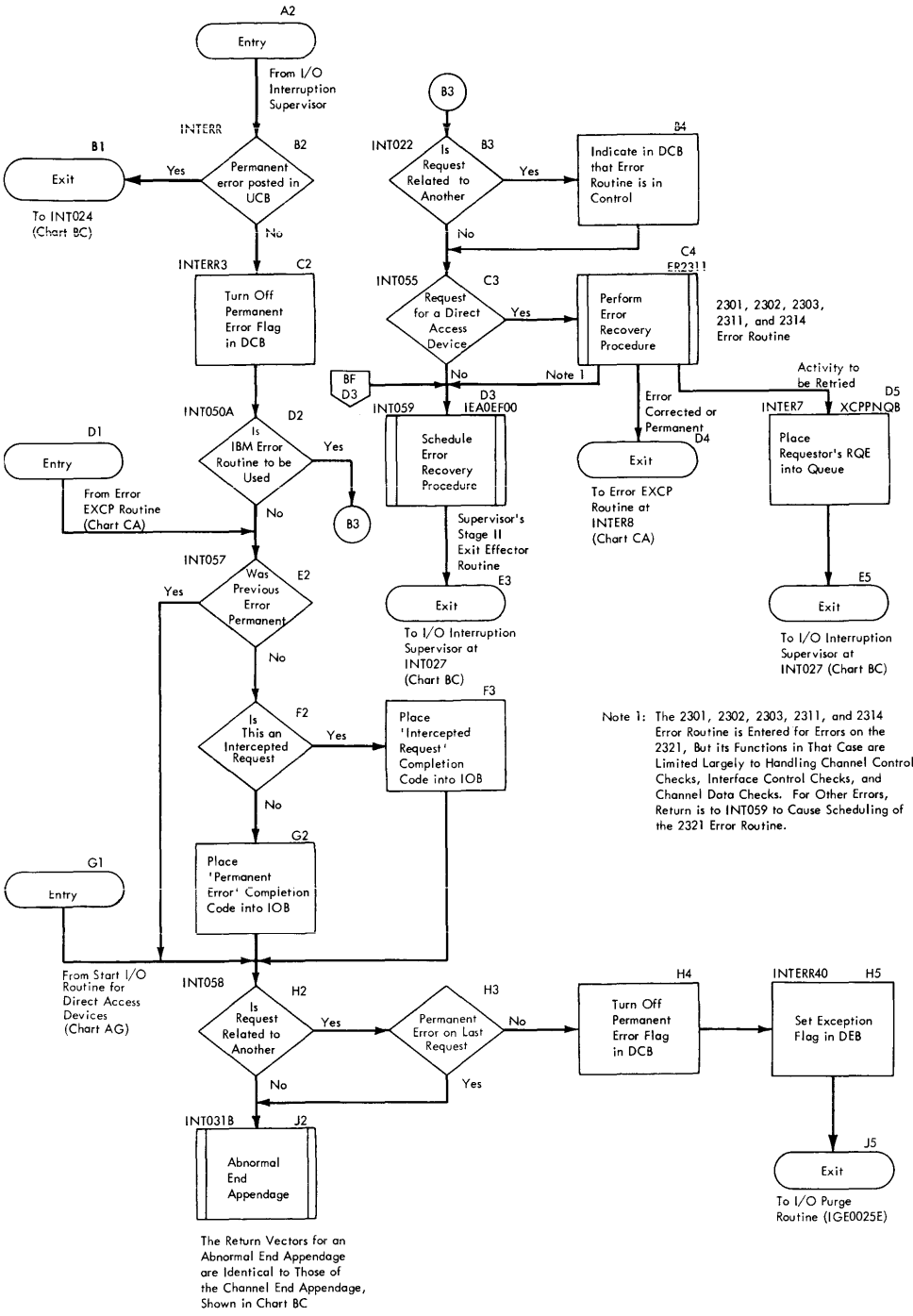


Chart BF. Error Routine Interface

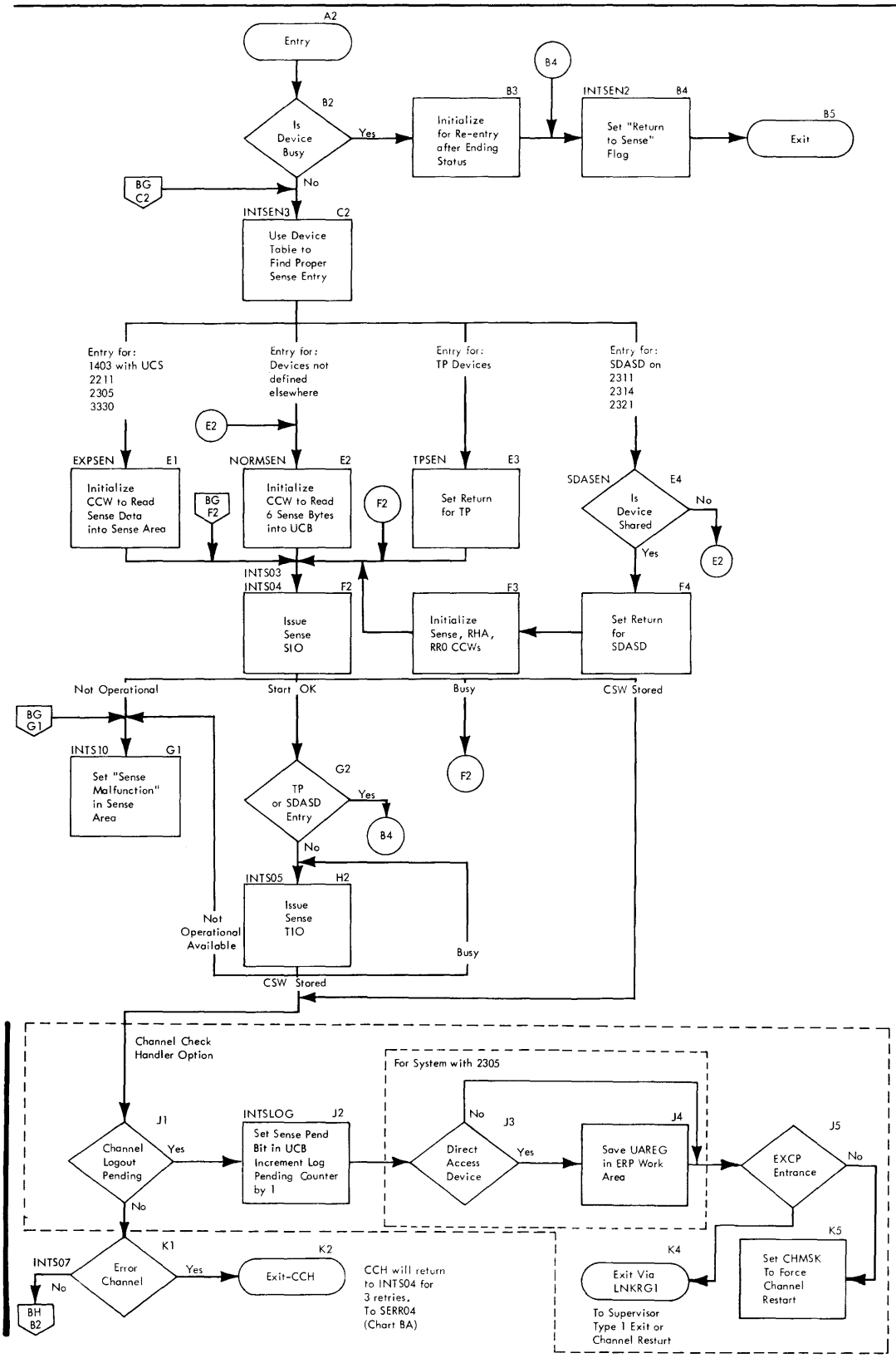


Chart BG (Part 1 of 2). Sense Subroutine

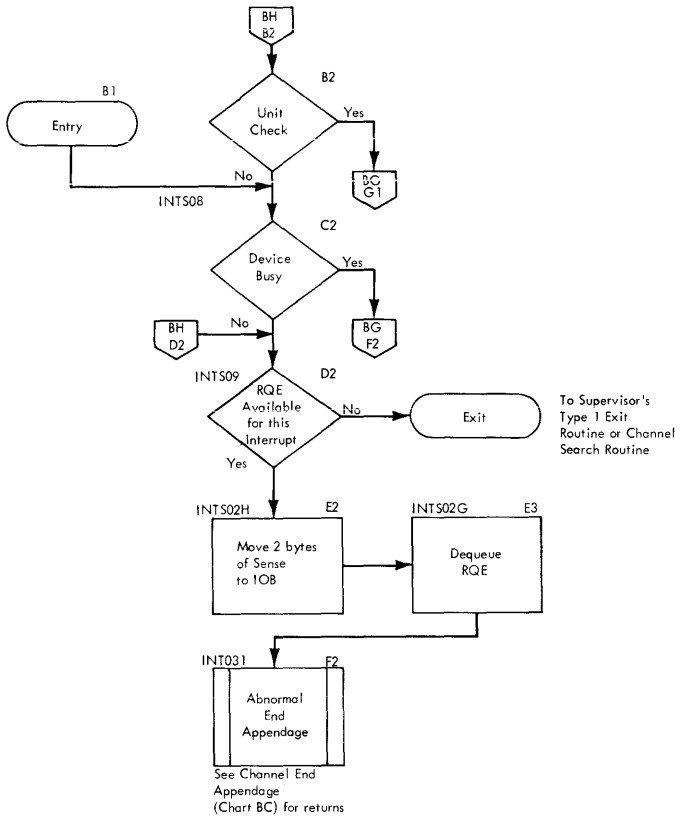


Chart BH (Part 2 of 2). Sense Subroutine

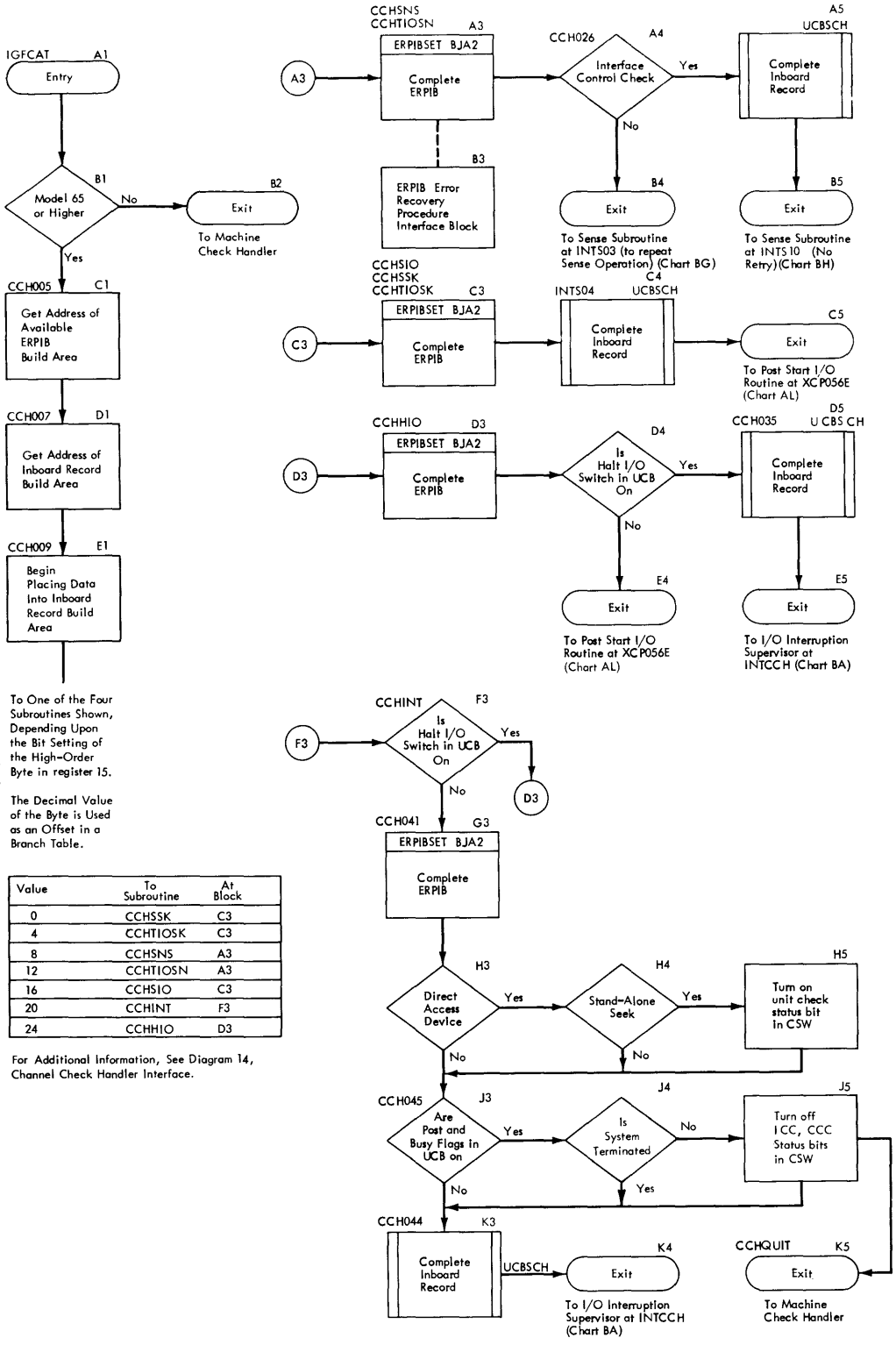


Chart BI (Part 1 of 3). Channel Check Handler

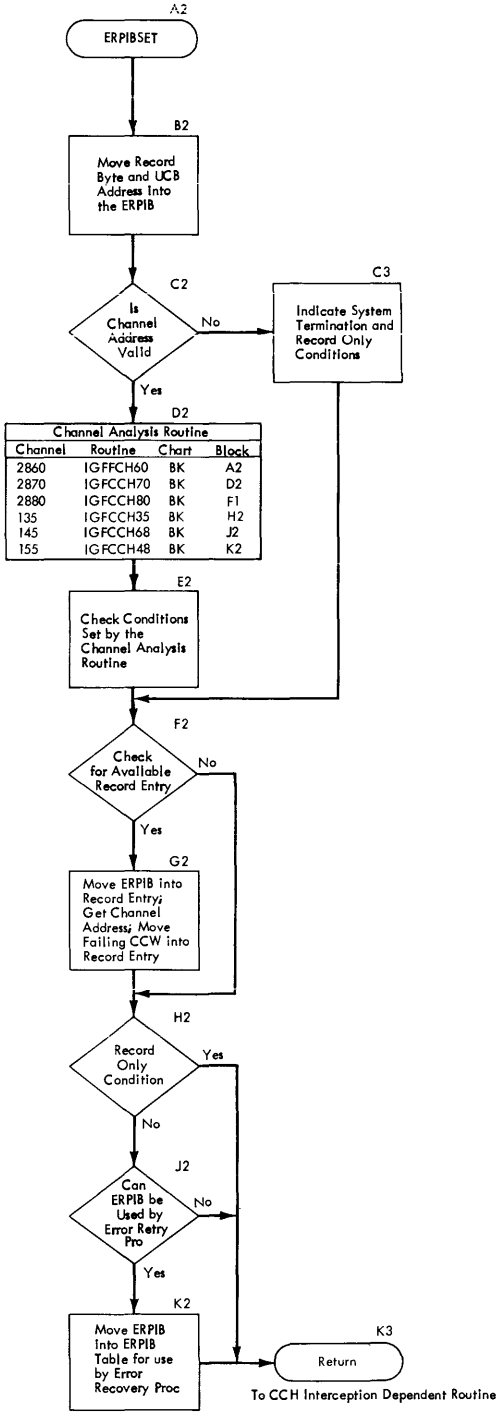


Chart BJ (Part 2 of 3). Channel Check Handler

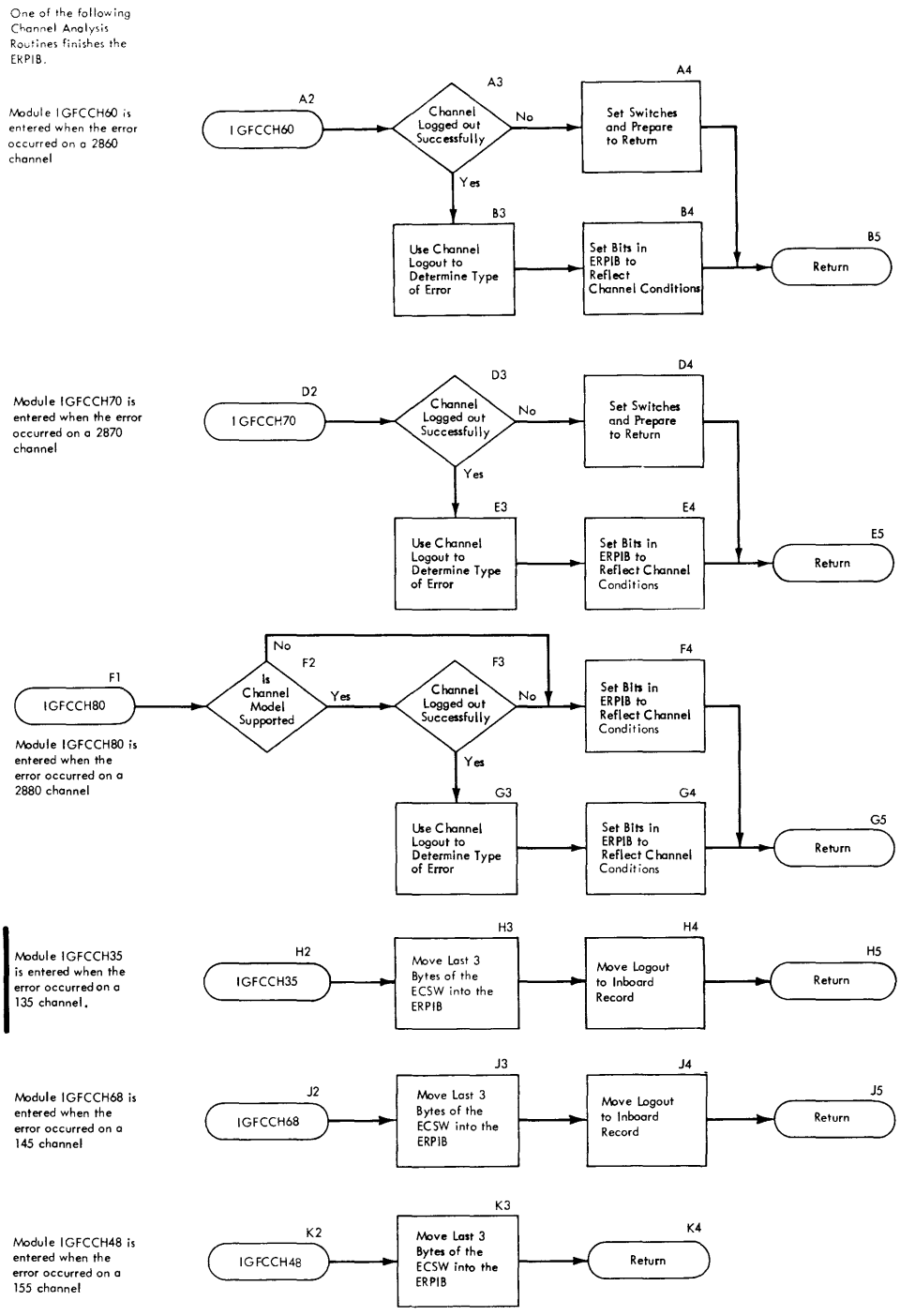


Chart BK (Part 3 of 3). Channel Check Handler

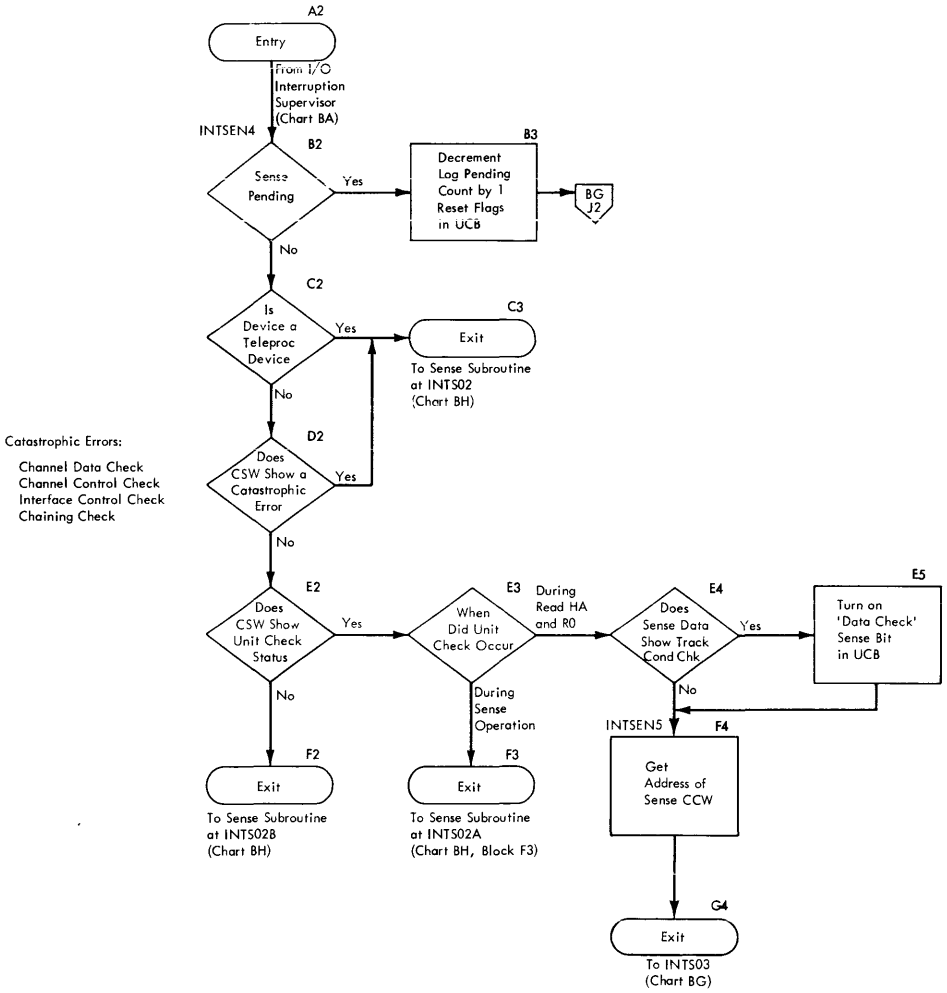


Chart BL. Teleprocessing and Shared DASD Post–Sense Processing

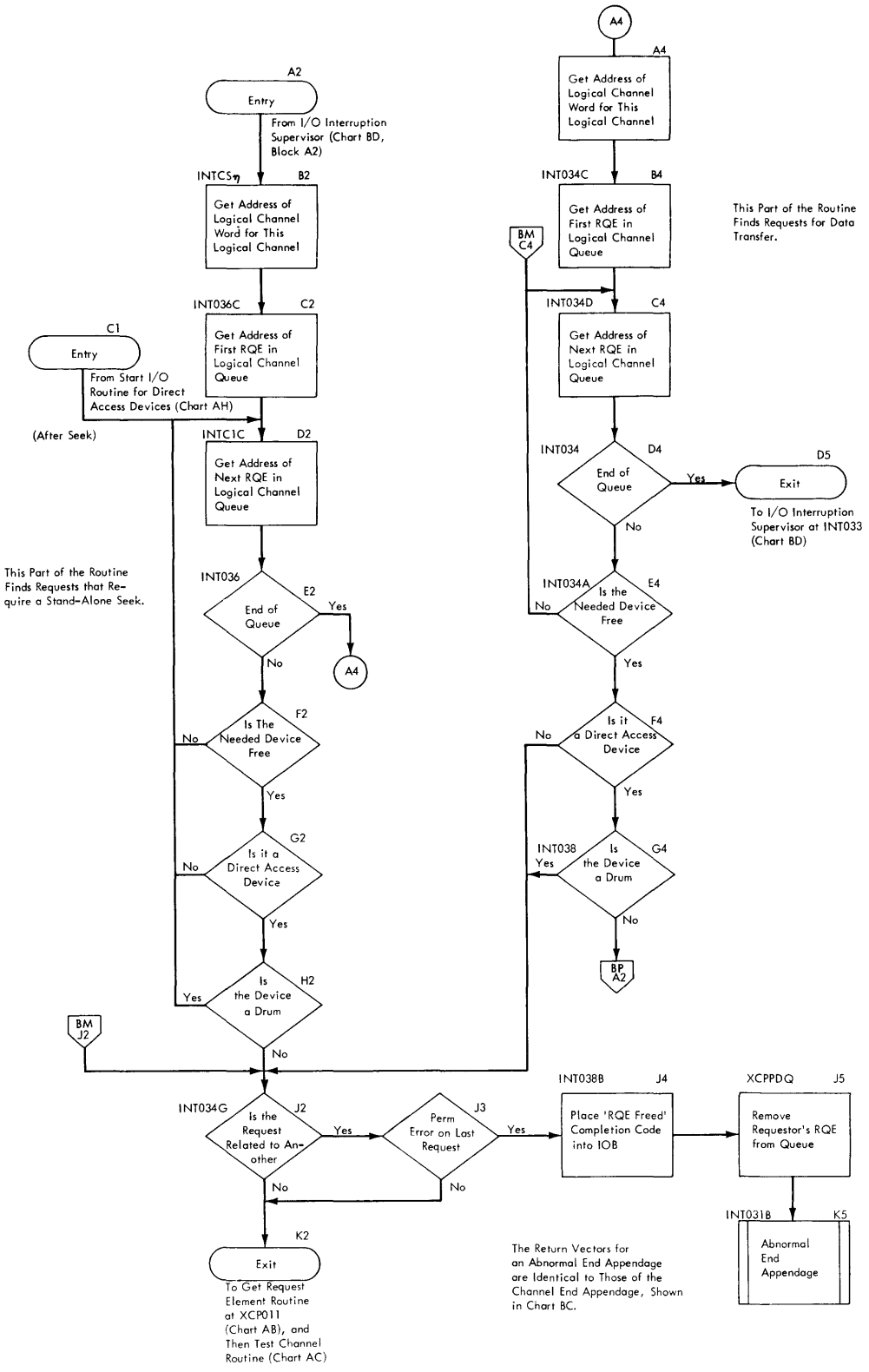


Chart BM. Channel Search Routine, No Alternate Paths

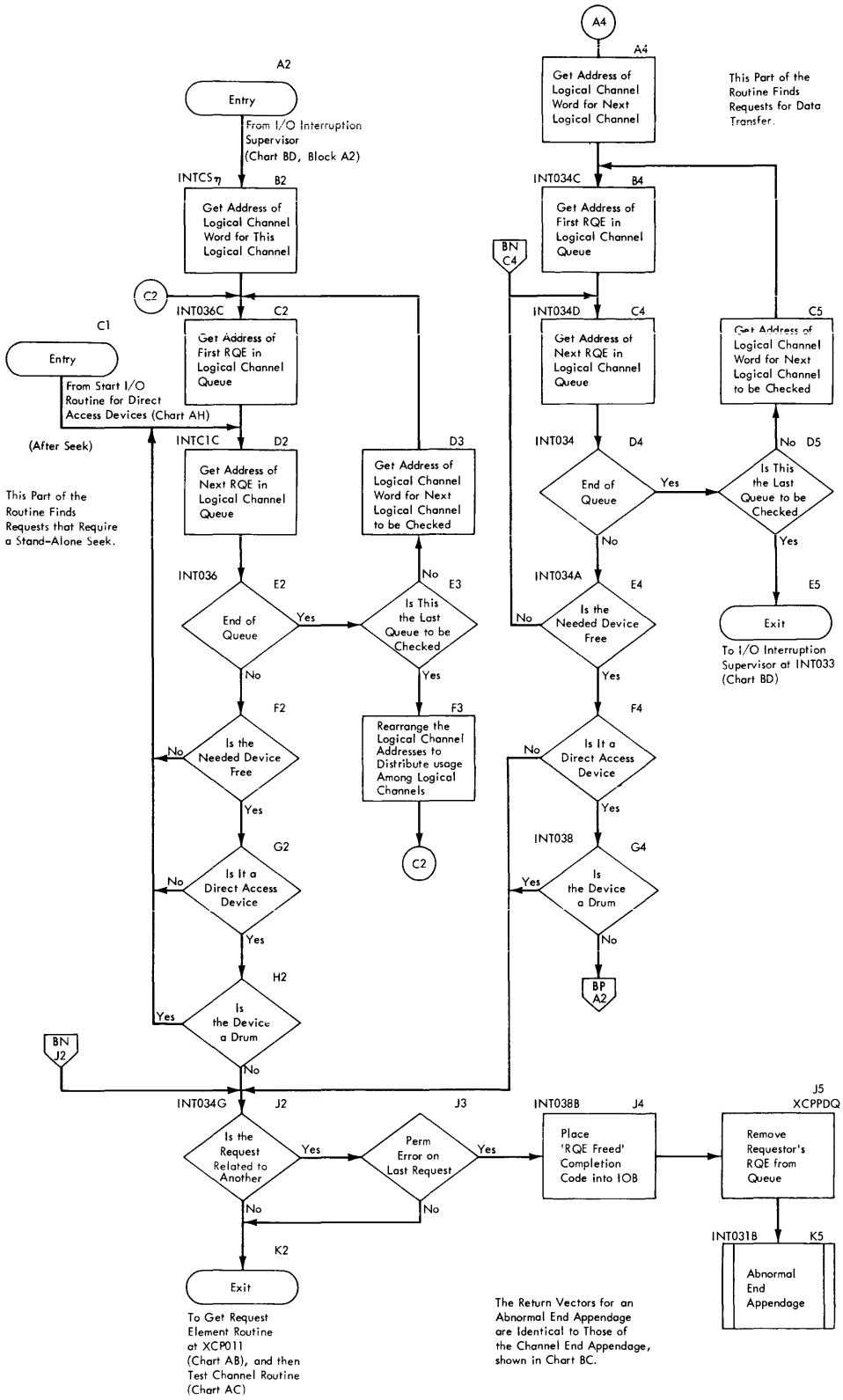


Chart BN. Channel Search Routine, Alternate Paths

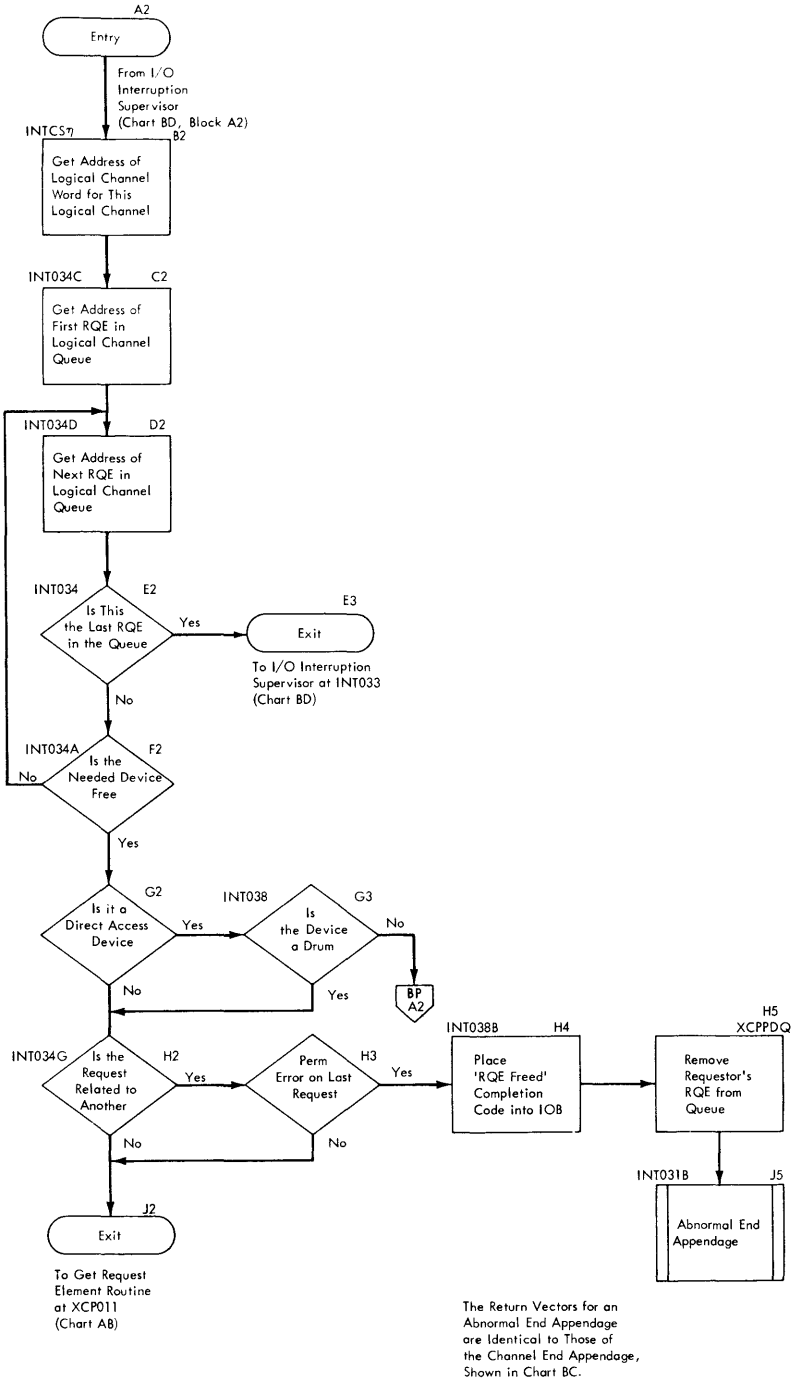


Chart BO (Part 1 of 2). Channel Search Routine, Byte–Multiplexor Channel

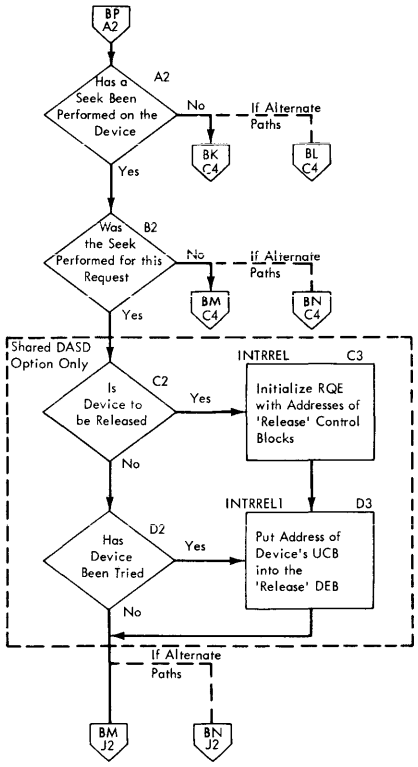


Chart BP (Part 2 of 2). Channel Search Routine

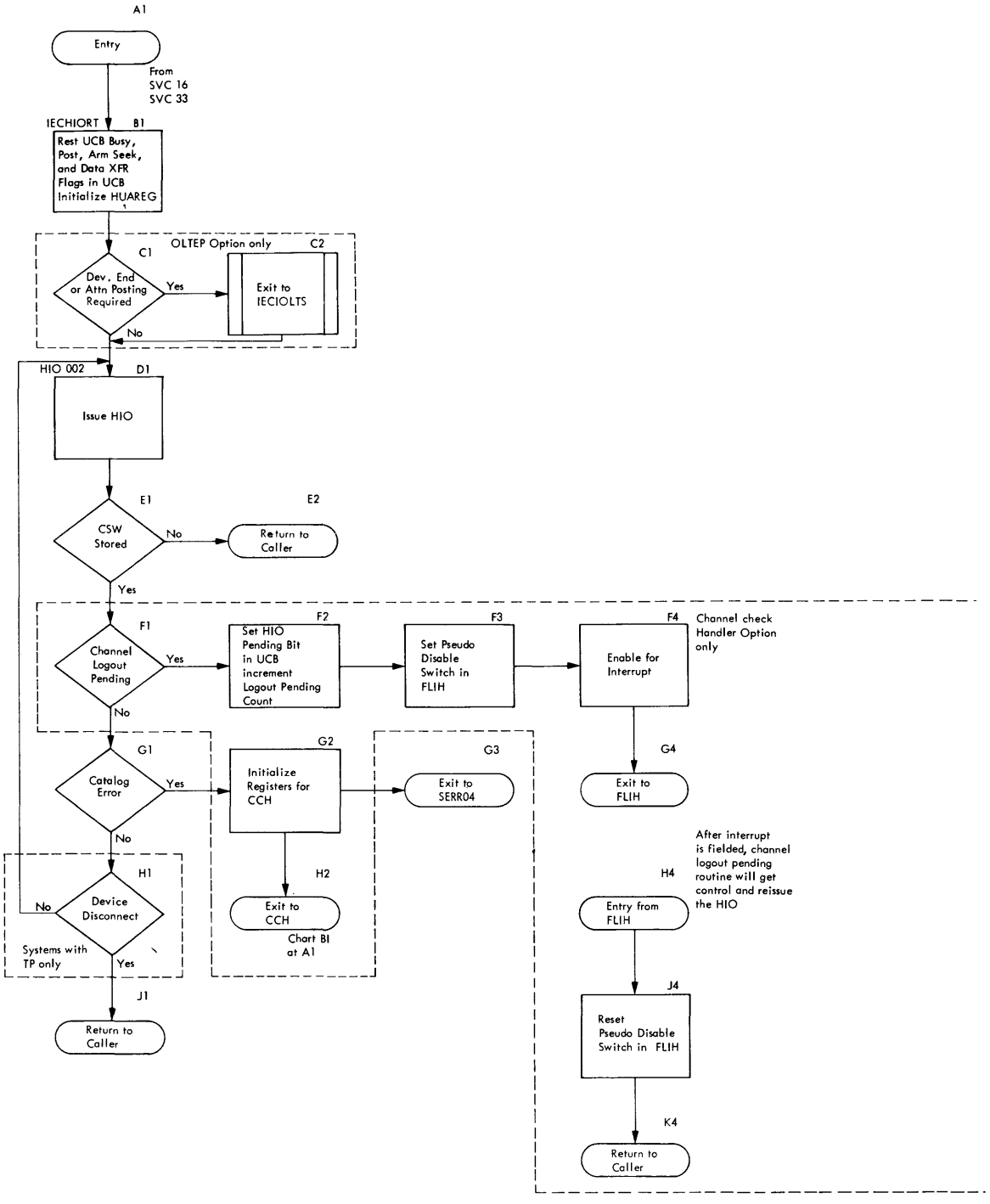


Chart BQ. Common Halt I/O Routine

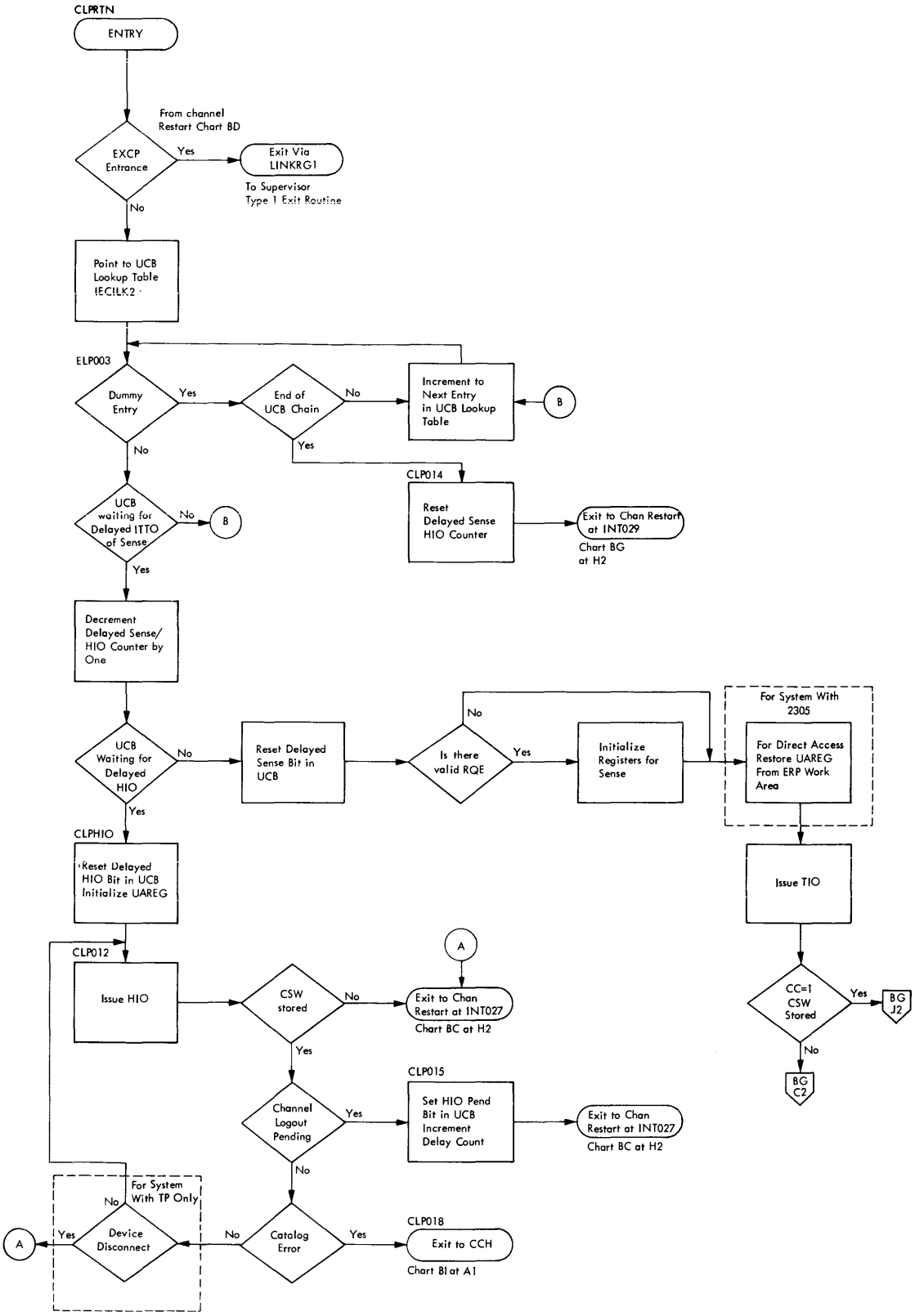


Chart BR. Channel Logout Pending Routine

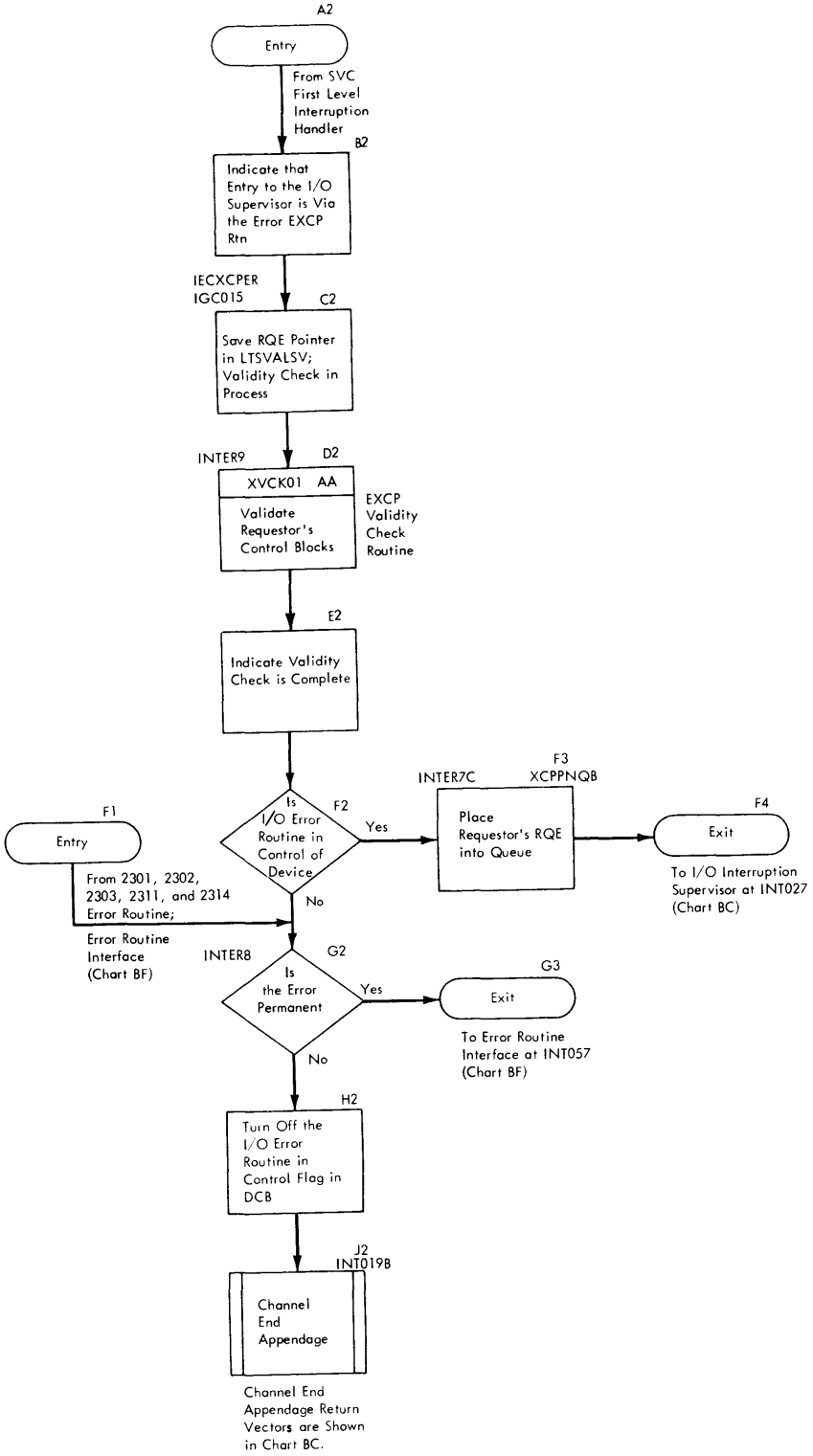


Chart CA. Error EXCP Routine

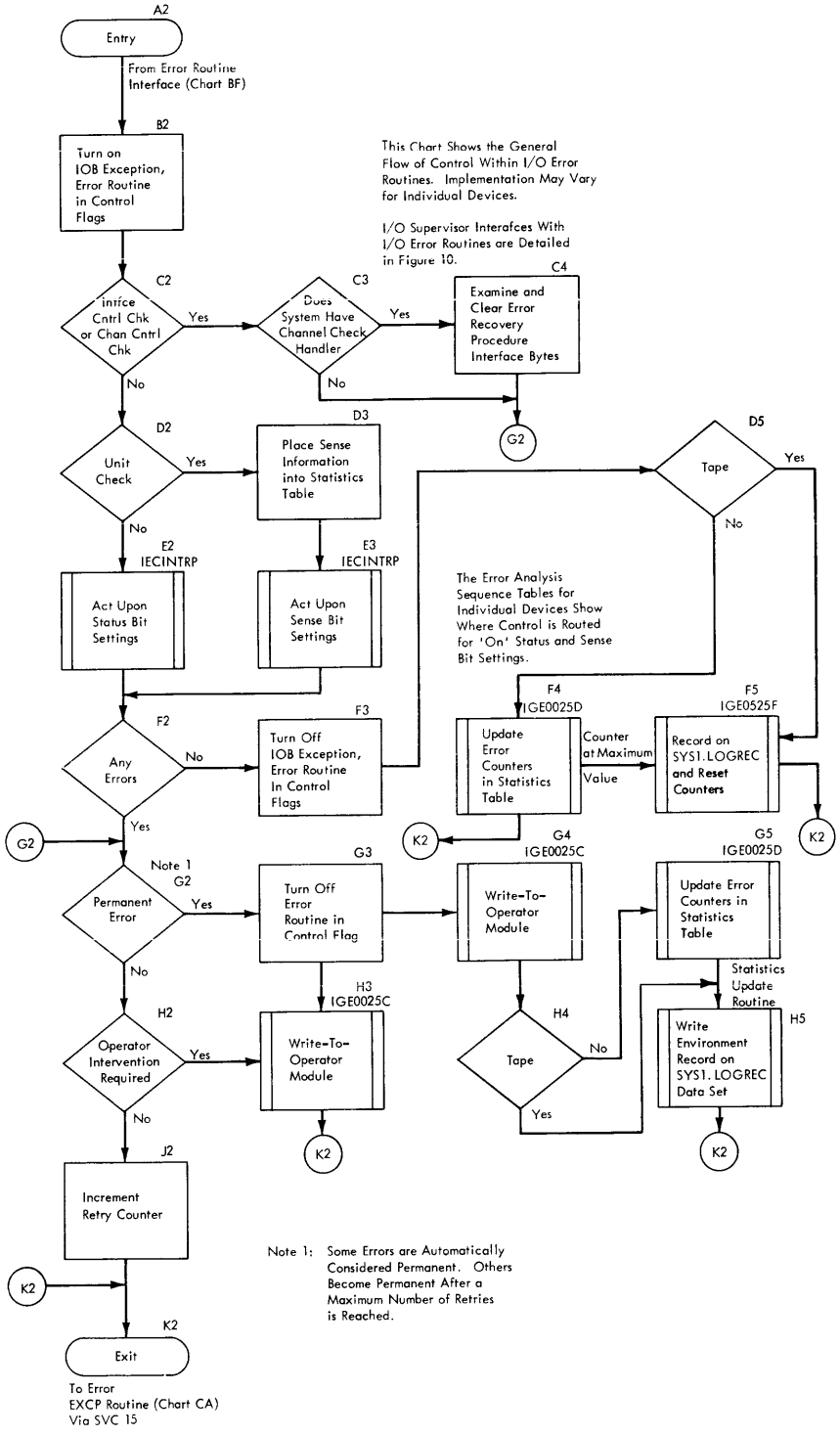
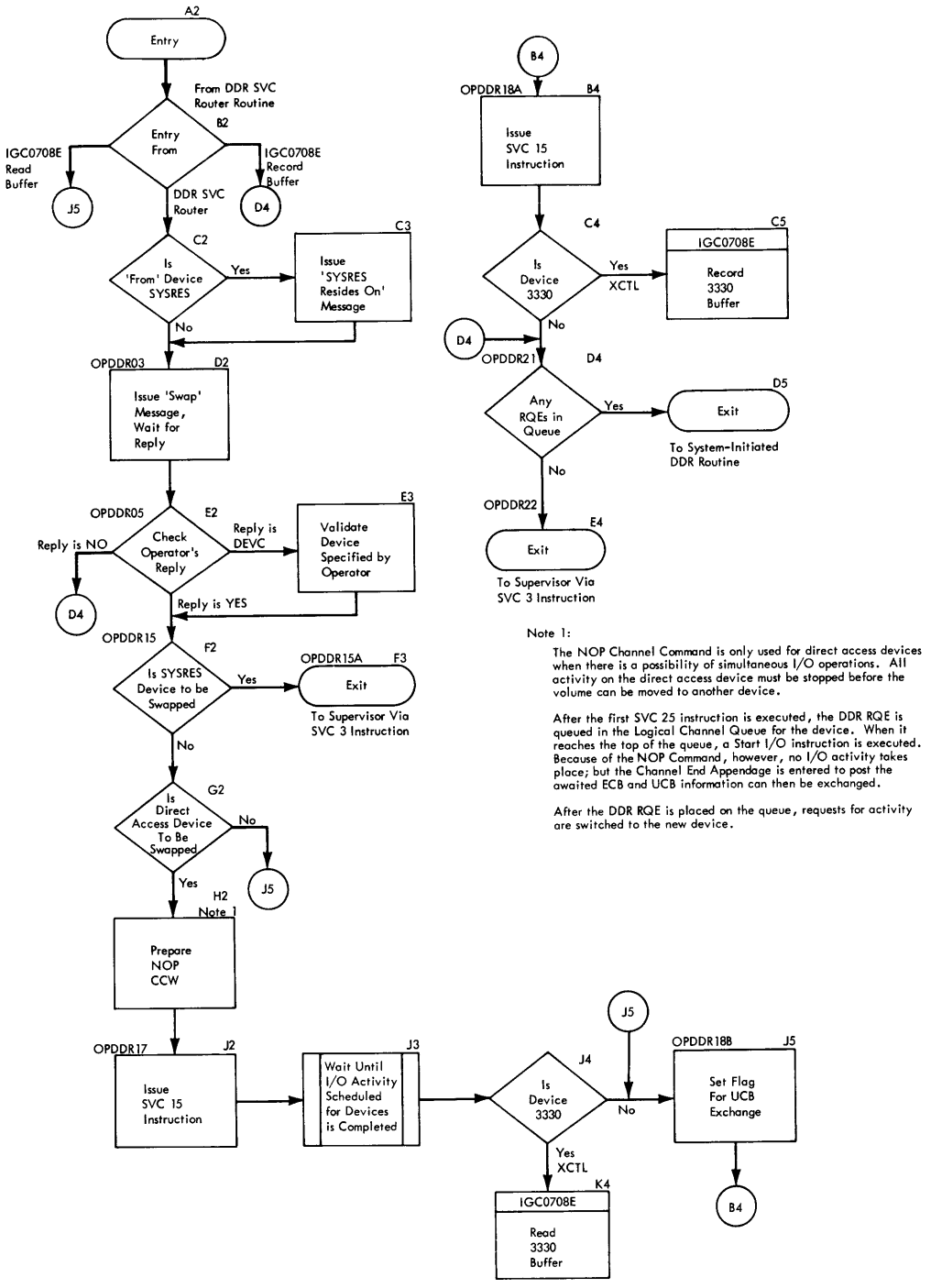


Chart CB. I/O Error Recovery Routines



Note 1:

The NOP Channel Command is only used for direct access devices when there is a possibility of simultaneous I/O operations. All activity on the direct access device must be stopped before the volume can be moved to another device.

After the first SVC 25 instruction is executed, the DDR RQE is queued in the Logical Channel Queue for the device. When it reaches the top of the queue, a Start I/O instruction is executed. Because of the NOP Command, however, no I/O activity takes place; but the Channel End Appendage is entered to post the awaited ECB and UCB information can then be exchanged.

After the DDR RQE is placed on the queue, requests for activity are switched to the new device.

Chart DA. Operator–Initiated DDR Routine

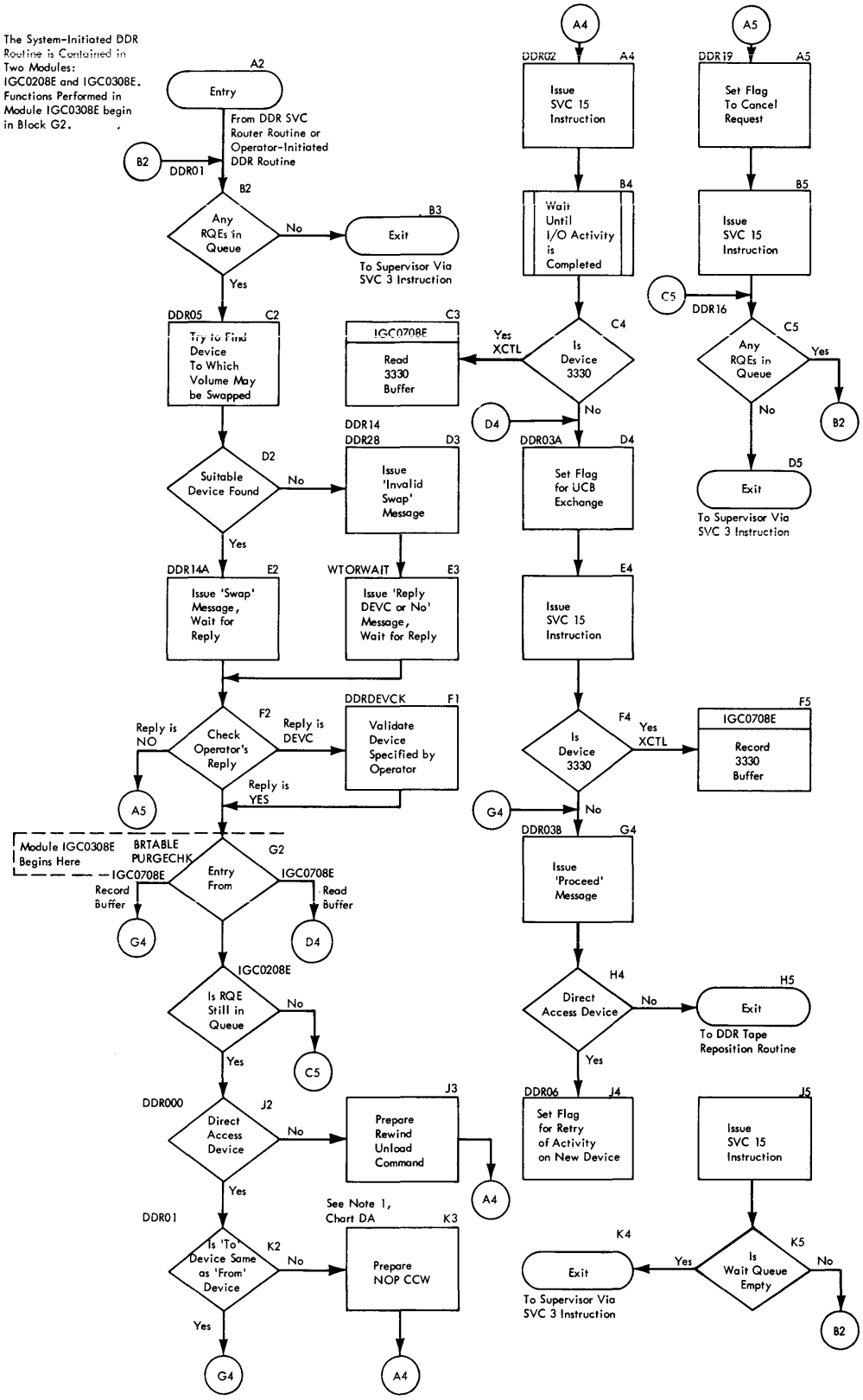


Chart DB. System–Initiated DDR Routine

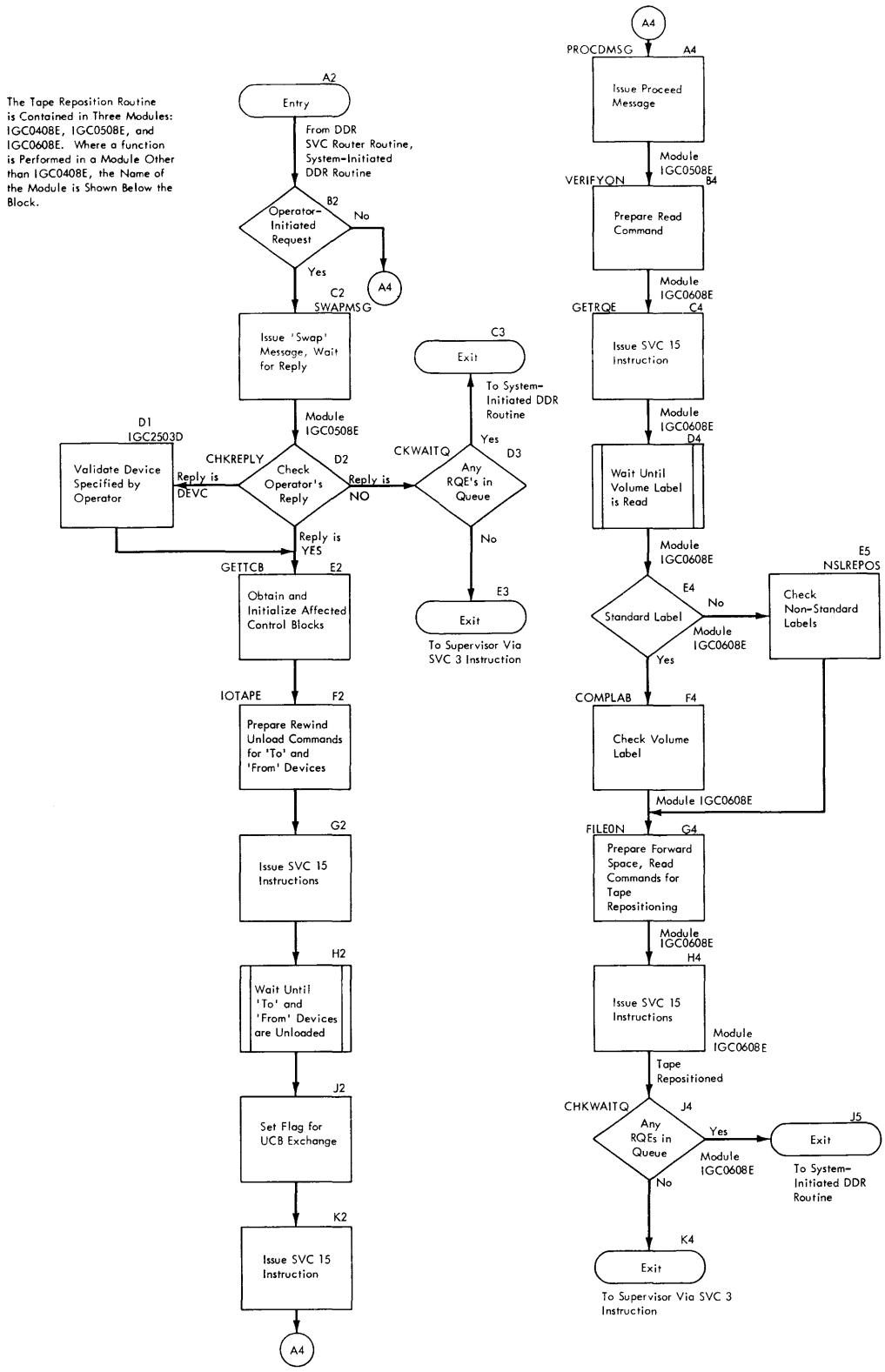


Chart DC. DDR Tape Reposition Routine

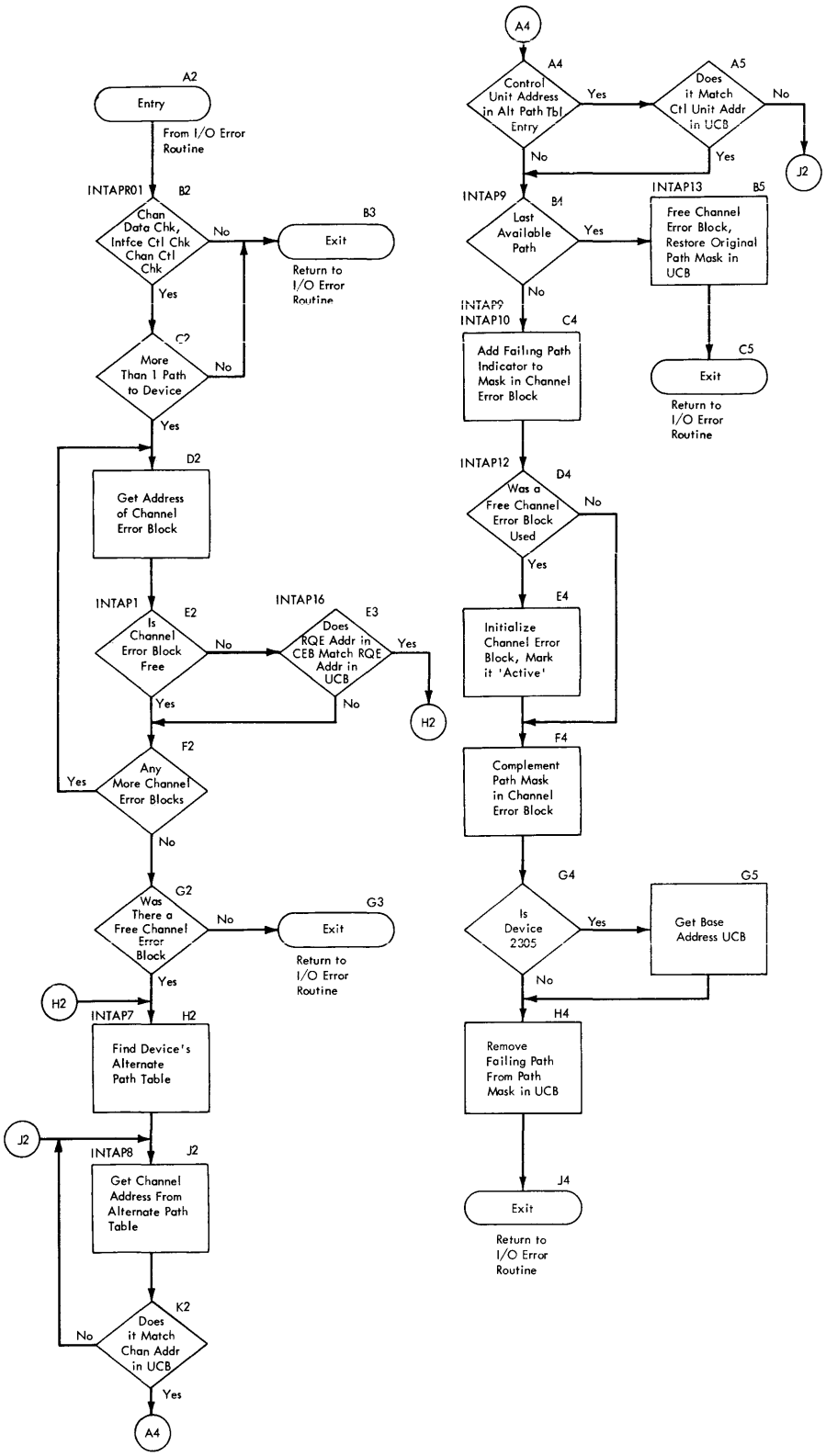


Chart EA. Alternate Path Retry Routine

SECTION 4: DIRECTORIES

Module Directory

Data Area Directory

Symbol Table

Module Directory

Table 33 contains information about the physical structure of the I/O supervisor. The column headings and their meanings are:

Symbolic Name: The symbolic name of a table, routine, object module, or control section.

Description: The type of item to which the symbolic name applies.

Object Module Name: The name of the object module containing the item. The microfiche cards containing program listings are ordered by object module name.

Control Section Name: The name of the control section containing the item.

PLM References: Places in this publication where more information about the item can be found.

Library: The data set normally containing the item.

Code	Data Set
NUC	SYS1.NUCLEUS
SVC	SYS1.SVCLIB

If SVC Routine: Information about I/O supervisor SVC routines. There are four types of SVC routines.

Type 1 SVC routines are part of the nucleus and are disabled (masked) for all interruptions except machine check interruptions.

Type 2 SVC routines are part of the nucleus but may be enabled (interruptable) for part of their operation.

Type 3 SVC routines are nonresident, may be enabled, and are not larger than 1024 bytes.

Type 4 SVC routines are nonresident, may be enabled, and are larger than 1024 bytes. They are brought into storage in segments of up to 1024 bytes.

Name: The name of the item being described.

When the control section name for an item is not the same as the object module name, the item will have two entries in the table—one filed by control section name and the other filed by object module name. Therefore, it is unnecessary to check beyond the first column when looking for a symbolic name.

The three major groups of routines that make up the I/O supervisor—the EXCP supervisor, the I/O interruption supervisor, and the error EXCP supervisor—are contained in the control program nucleus. As a result, there are no CSECT names or load module names in these three major groups of routines. Linkage parameter lists, usually associated with multi–load routines, are also unnecessary. Therefore entry points are not of the formal one–or–two–entries–only type (due to stringent parameter list requirements), but rather are ordinary symbolic labels, undistinguishable from other symbolic labels.

Table 33 (Part 1 of 5). I/O Supervisor Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	PLM References		Library	If SVC Routine			Name
				Section	Chart		Type	Macro Instruction	SVC No.	
CAWLOC	Table	*	*	5						Channel Address Word
CSWLOC	Table	*	*	5						Channel Status Word
DEVTAB	Table	*	*	5		NUC				Device Table
IECCST	Table	*	*	5		NUC				Channel Table
IECILCH	Table	*	*	5		NUC				Logical Channel Table
IECILK1	Table	*	*	5		NUC				UCB Lookup Table
IECINT	Routine	*	*	3	BA-BE	NUC				I/O Interruption Supervisor
IECINTRP	Object Module	IECINTRP	IECINTRP	2		NUC				Error Interpreter Routine
IECIOQET	Table	*	*	5		NUC				Request Queue Element Table
IECIPRMP	Object Module	IECIPRMP	IGC016	7		SVC	2	PURGE	16	Purge Routine (Model 65 Multiprocessing)
IECIPRTS	Object Module	IECIPRTS	IGC016	7		SVC	2	PURGE	16	Purge Routine (TSO)
IECIPR1A	Object Module	IECIPR1A	IGC016A	7		SVC	4	PURGE	16	Purge Routine, Load 2 of 3 (MFT)
IECIPR1B	Object Module	IECIPR1B	IGC016B	7		SVC	4	PURGE	16	Purge Routine, Load 3 of 3 (MFT)
IECIPR12	Object Module	IECIPR12	IGC016	7		SVC	4	PURGE	16	Purge Routine, Load 1 of 3 (MFT)
IECIPR16	Object Module	IECIPR16	IGC016	7		SVC	2	PURGE	16	Purge Routine (MVT)
IECSTATA	Control Section	IGE0025D	IECSTATA	2		SVC				Statistics Update Routine
IECSTB	Table	*	*	5		NUC				Statistics Table
IECWTORA	Control Section	IGE0025C	IECWTORA	2		SVC				Write-to-Operator Routine, Load 1 of 5 [1]
IECWTORB	Control Section	IGE0125C	IECWTORB	2		SVC				Write-to-Operator Routine, Load 2 of 5 [1]
IECWTORC	Control Section	IGE0225C	IECWTORC	2		SVC				Write-to-Operator Routine, Load 3 of 5 [1]
IECWTORD	Control Section	IGE0325C	IECWTORD	2		SVC				Write-to-Operator Routine, Load 4 of 5 [1]
IECWTORE	Control Section	IEC0425C	IECWTORE	2		SVC				Write-to-Operator Routine, Load 5 of 5 [1]
IEC1052A	Control Section	IGE0000D	IEC1052A	2		SVC				1052 Error Routine
IEC1402A	Control Section	IGE0001C	IEC1402A	2		SVC				2540 Error Routine, Load 1 of 2
IEC1402B	Control Section	IGE0101C	IEC1402B	2		SVC				2540 Error Routine, Load 2 of 2
IEC1403A	Control Section	IGE0000G	IEC1403A	2		SVC				1403 and 1443 Error Routine
IEC1442A	Control Section	IGE0000E	IEC1442A	2		SVC				2501, 2520, and 1442 Error Routine
IEC23XXF	Object Module	*	*	2		NUC				2301, 2302, 2303, 2305, 2311, 2314, 2321 and 3330 Error Routine
IEC2400I	Control Section	IGE0900I	IEC2400I	2		SVC				2400/3400 Tape Series Error Routine, Load 6 of 6

* Refer to installation system generation listing.

1 Do not confuse with the Write-to-Operator SVC routine (SVC 35), described in the publications:

OS MFT Job Management Logic, GY27-7128
OS MVT Supervisor Logic, GY28-6659

Table 33 (Part 2 of 5). I/O Supervisor Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	PLM References		Library	If SVC Routine			Name
				Section	Chart		Type	Macro Instruction	SVC No.	
IEC2671A	Control Section	IGE0002I	IEC2671A	2		SVC				2671 Error Routine
IEC3211A	Control Section	IGE0000F	IEC3211A	2		SVC				3211 Error Routine
IEC3211B	Control Section	IGE0100F	IEC3211B	2		SVC				3211 Error Routine
IFBSTAT	Object Module	IFBSTAT	IGC0007F	2,7		SVC	3	-none-	76	SYS1.LOGREC Recording Routine
IGC000	Routine	*	*	3	AA-AI	NUC	1	EXCP	0	EXCP Supervisor
IGC0001G	Object Module	IGC0001G	SVC017	7		SVC	3	RESTORE	17	Restore Routine
IGC0003C	Object Module	IGC0003C	IGC00033	7		SVC	3	IOHALT	33	IOHALT Routine
IGC00033	Control Section	IGC0003C	IGC00033	7		SVC	3	IOHALT	33	IOHALT Routine
IGC0007F	Object Module	IFBSTAT	IGC0007F	7		SVC	4	-none-	76	SYS1.LOGREC Recorder Load 1 of 4
IGC0008E	Object Module	IGC0008E	IGC0008E	7		SVC	4	-none-	85	DDR SVC Router,Initiator,Terminator Routine
IGC0009A	Object Module	IGC0009A	IGC0009A	7		SVC	3	-none-	91	VOLSTAT Routine
IGC0010A	Object Module	IGC0010A	IGC0010A	7		SVC				Loads 2305/3330
IGC0024	Control Section	IGC0002D	IGC0024	7		SVC	3	DEVTYPE	24	DEVTYPE Routine
IGC0107F	Object Module	IFBSTAT1	IGC0107F	7		SVC	4	-none-	76	SYS1.LOGREC IPL-EOD Load 3 of 4
IGC0108E	Object Module	IGC0108E	IGC0108E	7	DA	SVC	4	-none-	85	Operator-Initiated DDR Routine
IGC015	Routine	*	*	3	CA	NUC	1	-none-	15	Error EXCP Supervisor
IGC016	Control Section	IECIPRMP	IGC016	7		SVC	2	PURGE	16	Purge Routine (Model 65 Multiprocessing)
IGC016	Control Section	IECIPRTS	IGC016	7		SVC	2	PURGE	16	Purge Routine (TSO)
IGC016	Control Section	IECIPR12	IGC016	7		SVC	4	PURGE	16	Purge Routine, Load 1 of 3 (PCP & MFT)
IGC016	Control Section	IECIPR16	IGC016	7		SVC	2	PURGE	16	Purge Routine (MVT)
IGC016A	Control Section	IECIPR1A	IGC016A	7		SVC	4	PURGE	16	Purge Routine, Load 2 of 3 (PCP & MFT)
IGC016B	Control Section	IECIPR1B	IGC016B	7		SVC	4	PURGE	16	Purge Routine, Load 3 of 3 (PCP & MFT)
IGC0207F	Object Module	IFBSTAT2	IGC0207F	7		SVC	4	-none-	76	SYS1.LOGREC Message Routine Load 4 of 4
IGC0208E	Object Module	IGC0208E	IGC0208E	7	DB	SVC	4	-none-	85	System-Initiated DDR Routine, Load 1 of 2
IGC0307F	Object Module	IFBSTAT0	IGC0307F	7		SVC	4	-none-	76	SYS1.LOGREC Statistics Function Load 2 of 4
IGC0308E	Object Module	IGC0308E	IGC0308E	7	DB	SVC	4	-none-	85	System-Initiated DDR Routine, Load 2 of 2
IGC0408E	Object Module	IGC0408E	IGC0408E	7	DC	SVC	4	-none-	85	DDR Tape Reposition Routine, Load 1 of 2
IGC0508E	Object Module	IGC0508E	IGC0508E	7	DC	SVC	4	-none-	85	DDR MSG Mod #1
IGC0608E	Object Module	IGC0608E	IGC0608E	7	DC	SVC	4	-none-	85	DDR Tape Reposition Routine, Load 2 of 2
IGC0708E	Object Module	IGC0708E	IGC0708E	7		SVC	4	-none-		DDR Recording
IGC0808E	Object Module	IGC0808E	IGC0808E	7		SVC	4	-none-		DDRMSG Mod #2
IGC092	Routine	*	*	7		NUC	1	-none-	92	TCB EXCP Routine (TSO)

* Refer to installation system generation listing.

Table 33 (Part 3 of 5). I/O Supervisor Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	PLM References		Library	If SVC Routine			Name
				Section	Chart		Type	Macro Instruction	SVC No.	
IGC2503D	Object Module	IGC2503D	IGF2503D	7		SVC				DDR Swap Command Processor Routine
IGE0000D	Object Module	IGE0000D	IEC1052A	2		SVC				1052 Error Routine
IGE0000E	Object Module	IGE0000E	IEC1442A	2		SVC				2501, 2520, and 1442 Error Routine
IGE0000F	Object Module	IGE0000F	IEC3211A	2		SVC				3211 Error Routine
IGE0000G	Object Module	IGE0000G	IEC1403A	2		SVC				1403 and 1443 Error Routine
IGE0000I	Object Module	IGE0000I	IGE0001	2		SVC				2400/3400 Tape Series Error Routine, Load 1 of 6
IGE0001C	Object Module	IGE0001C	IEC1402A	2		SVC				2540 Error Routine, Load 1 of 2
IGE0002I	Object Module	IGE0002I	IEC2671A	2		SVC				2671 Error Routine
IGE0010A	Object Module	IGE0010A	IGE0010A	2		SVC				2250 Error Routine
IGE0010B	Object Module	IGE0010B	IGE0010B	2		SVC				2260 and 1053 Error Routine, Load 1 of 2
IGE0010D	Object Module	IGE0010D	IGE0010D	2		SVC				5450 Error Routine
IGE0011A	Object Module	IGE0011A	IGE0011A	2		SVC				2495 Error Routine
IGE0011B	Object Module	IGE0011B	IGE0011B	2		SVC				1285 Error Routine
IGE0011C	Object Module	IGE0011C	IGE0011C	2		SVC				1287 Error Routine
IGE0011D	Object Module	IGE0011D	IGE0011D	2		SVC				1288 Error Routine
IGE0011E	Object Module	IGE0011E	IGE0011E	2		SVC				1419/1275 Error Routine
IGE0025C	Object Module	IGE0025C	IECWTORA	2		SVC				Write-to-Operator Routine, Load 1 of 5 [1]
IGE0025D	Object Module	IGE0025D	IECSTATA	2		SVC				Statistics Update Routine
IGE0025E	Object Module	IGE0025E	IGE0025E	2		SVC				I/O Purge Routine
IGE0025F	Object Module	IGE0025F	IGE0025F	2		SVC				Outboard Recorder Routine, Load 1 of 2
IGE0100F	Object Module	IGE0100F	IEC3211B	2		SVC				3211 Error Routine, Load 2 of 2
IGE0100I	Object Module	IGE0100I	IGE0100I	2		SVC				2400/3400 Tape Series Error Routine, Load 2 of 6
IGE0101C	Object Module	IGE0101C	IEC1402B	2		SVC				2540 Error Routine, Load 2 of 2
IGE0110B	Object Module	IGE0110B	IGE0110B	2		SVC				2260 and 1053 Error Routine, Load 2 of 2
IGE0125C	Object Module	IGE0125C	IECWTORB	2		SVC				Write-to-Operator Routine, Load 2 of 5 [1]
IGE0125E	Object Module	IGE0125E	IGE0125E	7		SVC				Volume Verification Routine, Load 1 of 2
IGE0125F	Object Module	IGE0125F	IGE0125F	2		SVC				Outboard Recorder Routine, Load 2 of 2

* Refer to installation system generation listing.

1 Do not confuse with the Write-to-Operator SVC Routine (SVC 35), described in the publications:

OS MFT Job Management Logic, GY27-7128.
OS MVT Supervisor Logic, GY28-6659.

Table 33 (Part 4 of 5). I/O Supervisor Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	PLM References		Library	If SVC Routine			Name
				Section	Chart		Type	Macro Instruction	SVC No.	
IGE02001	Object Module	IGE02001	IGE02001	2		SVC				2400/3400 Tape Series Error Routine, Load 3 of 6
IGE0225C	Object Module	IGE0225C	IECWTORC	2		SVC				Write-to-Operator Routine, Load 3 of 5 [1]
IGE0225E	Object Module	IGE0225E	IGE0225E	7		SVC				Volume Verification Routine, Load 2 of 2
IGE03001	Object Module	IGE03001	IGE03001	2		SVC				2400/3400 Tape Series Error Routine, Load 4 of 6
IGE0325C	Control Section	IGE0325C	IECWTORD	2		SVC				Write-to-Operator Routine, Load 4 of 5 [1]
IGE04001	Object Module	IGE04001	IGE04001	2		SVC				2400/3400 Tape Series Error Routine, Load 5 of 6
IGE0625F	Object Module	IGE0625F	IGE0525F	2		SVC				Miscellaneous Data Recording Routine
IGE0425C	Control Section	IGE0425C	IECWTORE	2		SVC				Write-to-Operator Routine, Load 5 of 5 [1]
IGE0425F	Object Module	IGE0425F	IGE0425F	2		SVC				System Environment Recording Message Routine
IGE0660A	Object Module	IGE0660A	IGE0660A	7		SVC				DDR Central Routine
IGE09001	Object Module	IGE09001	IEC2400D	2		SVC				2400/3400 Tape Series Error Routine, Load 6 of 6
IGFCAT	Routine	*	IGFCAT	3	BI	NUC				Channel Check Handler Routine
IGFCCH35	Object Module	IGFCCH35	IGFCCH35	7	BK	LINK				Channel Dependent Analysis for 135
IGFCCH48	Object Module	IGFCCH48	IGFCCH35	7	BK	LINK				Channel Dependent Analysis for 155
IGFCCH60	Object Module	IGFCCH60	IGFCCH60	3	BI	LINK				Channel Dependent Analysis for 2860
IGFCCH68	Object Module	IGFCCH68	IGFCCH68	7	BK	LINK				Channel Dependent Analysis for 145
IGFCCH70	Object Module	IGFCCH70	IGFCCH70	3	BI	LINK				Channel Dependent Analysis for 2870
IGFCCH80	Object Module	IGFCCH80	IGFCCH80	7	BK	LINK				Channel Dependent Analysis for 2880
IGFDDRMF	Object Module	IGFDDRMF	IGFDDRMF	7		SVC				DDR Wait Routine (MFT)
IGFDDRMV	Object Module	IGFDDRMV	IGFDDRMV	7		SVC				DDR Wait Routine (MVT)
IGFDDRSR	Control Section	IGFDDR00	IGFDDRSR	7		SVC				DDR SYSRES Routine (Without MCS)
IGFDDRSR	Control Section	IGFDDR10	IGFDDRSR	7		SVC				DDR SYSRES Routine (With MCS)
IGFDDR00	Object Module	IGFDDR00	IGFDDRSR	7		SVC				DDR SYSRES Routine (Without MCS)
IGFDDR01	Object Module	IGFDDRMV	IGFDDR01	7		SVC				DDR Resident Module
IGFDDR02	Object Module	IGFDDR02	IGFDDR02	7		SVC				DDR Channel End Appendages
IGFDDR03	Object Module	IGFDDR03	IGFDDR03	7		SVC				DDR Abnormal End Appendage
IGFDDR10	Object Module	IGFDDR10	IGFDDRSR	7		SVC				DDR SYSRES Routine (With MCS)
IGF2503D	Control Section	IGC2503D	IGF2503D	7		SVC				DDR Swap Command Processor Routine
IGX00015	Object Module	IGX00015	IGX00015	7		SVC				Extended SVC Routine
INTAPR01	Routine	*	*	7	EA	NUC				Alternate Path Retry Routine
INTATT	Routine	*	*	3	AI	NUC				Attention Routine Interface
INTCSη	Routine	*	*	3	BN-BP	NUC				Channel Search Routine

* Refer to installation system generation listing.

Table 33 (Part 5 of 5). I/O Supervisor Module Directory

Symbolic Name	Description	Object Module Name	Control Section Name	PLM References		Library	If SVC Routine			Name
				Section	Chart		Type	Macro Instruction	SVC No.	
INTDAT	Routine	*	*	3	BB	NUC				Trap Routine for Direct Access Devices
INTERR	Routine	*	*	3	BF	NUC				Error Routine Interface
INTSEN	Routine	*	*	3	BG-BH	NUC				Sense Subroutine
INTTAT	Routine	*	*	3	BB	NUC				Trap Routine for Magnetic Tape Devices
INTURT	Routine	*	*	3	BB	NUC				Trap Routine for Unit Record and Communications Devices
INT027	Routine	*	*	3	BC	NUC				Channel Restart Routine
IONPSW	Table	*	*	5						I/O New PSW
IOPSWO	Table	*	*	5						I/O Old PSW
LCHTAB	Table	*	*	5		NUC				Logical Channel Table
PRGCOMA	Routine	*	*	7		NUC				Quiesce Complete Subroutine
SERR04	Routine	*	*	3	AL,BA, BH	NUC				SER/CCH Routine Interface
SVCOPSW	Table	*	*	5						SVC Old PSW
SVC017	Control Section	IGC0001G	SVC017	7		SVC	3	RESTORE	17	Restore Routine
TSTAR	Table	*	*	5		NUC				Request Queue Element Table
UCBTAB	Table	*	*	5		NUC				UCB Lookup Table
VALCHK	Routine	*	*	3	AA	NUC				Validity Check Subroutine
XCPCHη	Routine	*	*	3	AC	NUC				Test Channel Routine
XCPPDQ	Routine	*	*	3	**	NUC				Dequeue Subroutine
XCPPIO	Routine	*	*	3	AL	NUC				Post Start I/O Routine
XCPPNQ	Routine	*	*	3	AB	NUC				Enqueue Subroutine
XCPPST	Routine	*	*	3	BC	NUC				Post Routine Interface
XCPSIO	Routine	*	*	3	AK	NUC				Start I/O Subroutine
XCPTST	Routine	*	*	3	AB	NUC				Get Request Element Routine
XIODSK1	Routine	*	*	3	AF-AG	NUC				Start I/O Routine for Direct Access Devices
XIOTPE	Routine	*	*	3	AE	NUC				Start I/O Routine for Magnetic Tape Devices
XIOUR	Routine	*	*	3	AD	NUC				Start I/O Routine for Unit Record and Communications Devices
XVCK01	Routine	*	*	3	AA	NUC				EXCP Validity Check Routine

* Refer to installation system generation listing.

** Refer to XCPPDQ in the Symbol Table for flowcharts showing the Dequeue Subroutine.

Data Area Directory

Table 34 contains a summary of information about the major data areas used by the I/O supervisor. The column headings and their meanings are:

Data Area Name: The name of the data area and its abbreviation, if there is one.

Beginning Symbol: Meaningful only for data areas contained in the nucleus. This symbol identifies the beginning of the data area, and can be used to locate the data area in the program listings.

Creation: Contains some indication as to the origin of the data area.

> Permanent Storage Assignment means that the area is part of the hardware and always occupies the main–storage location shown in the "Storage Area" column.
>
> Requestor means that creation and maintenance of the data area is the responsibility of the requestor of the I/O activity. All requestors do not have to explicitly create the needed data areas. (See Figure 1 and its accompanying text.)
>
> System Generation means that the data area is created during system generation. (This may mean simply that space is set aside for the area during system generation.)
>
> Supervisor means that the area is created and maintained by the supervisor portion of the control program.

Storage Area: Indicates where the data area can be found in main storage. Where "Requestor's" appears in this column, the data area is obtained by the requestor when it is needed; consequently, its location is not fixed.

Size: The size of the data area.

Means of Access: The most commonly used way of referring to the data area or one of its entries.

Table 34 (Part 1 of 2). Data Area Directory

Data Area Name	Beginning Symbol	Creation	Storage Area	Size	Means of Access
Alternate Path Table	XCPCHnB	System Generation	Nucleus	Three to Five Fullwords, Depending Upon No. of Paths to a Device	Beginning symbol.
Channel Address Word (CAW)	CAWLOC	Permanent Storage Assignment	72 (48)	Word	Beginning symbol.
Channel Availability Table (M65MP Option Only)	———	System Generation	Prefixed Storage Area	14 Bytes	The entry for each channel is addressable via an offset from the label CHAN0. The offset is based upon the channel address.
Channel Command Word (CCW)	———	By Requestor when Needed. IOS CCWs are Created during System Generation	Requestor's; Nucleus	Double Word	Address at requestor's first CCW is contained at offsets IOBST (start) or IOBSRS (restart) fields of IOB. Access to IOS CCWs varies with device type and circumstances. See Diagrams 4-7 in Section 2.
Channel Error Block Table	CEBTAB	System Generation	Nucleus	24 Bytes	Beginning symbol.
Channel Status Word (CSW)	CSWLOC	Permanent Storage Assignment	64 (40)	Double Word	Beginning symbol.
Channel Table	IECCST	System Generation	Nucleus	One-Word Entry for Each Physical Channel	To locate entry for specific channel, channel number is multiplied by four and added to beginning address of table.
Data Control Block (DCB)	———	By Requestor	Requestor's	Varies with Access Method	Symbolic names equated to offsets of fields.
Data Extent Block (DEB)	———	By Requestor	Requestor's	Varies with Device and Access Method	Symbolic names equated to offsets of fields.
Device Statistics Table	IECSTB	System Generation	Nucleus	One 10-Byte Entry for Each Device, plus One 10 Byte Control Field	Normally, the address of an entry for a device is obtained by multiplying the statistics table index in the device's UCB by 10 and adding the result to the beginning address of the device statistics table: STATAB x 10 + Beginning Address When there are more than 256 devices, however, the following method is used: (STATAB + 256η) x 10 + Beginning Address In the above, η is the number one or two to indicate the second and third 256-entry group in the device statistics table. The UCB addresses in the control field of the table are used to determine the number η. For the 2314 Direct Access Storage Facility, the low-order four bits of the fifth sense byte are added to the statistics table index before the index is used.
Device Table	DEVTAB	System Generation	Nucleus	One 6-Byte Entry for Each Queuing Option Selected for Each Device Type	Desired entry located by adding device table index from UCB to beginning address of table. A specific field within the entry is then located by adding the field's offset to the above sum.
Error Recovery Procedure Interface Blocks (ERPIB)	———	By Channel Check Handler	Nucleus	Double Word	I/O error routines find the ERPIB by 1) obtaining the address of the SYS1.LOGREC DCB, 2) obtaining the address of the SYS1.LOGREC parameter table from the field at offset 0 in the DCB, and 3) obtaining the address of the ERPIB from a field at offset 0 in the SYS1.LOGREC parameter table.

Table 34 (Part 2 of 2). Data Area Directory

Data Area Name	Beginning Symbol	Creation	Storage Area	Size	Means of Access
Event Control Block (ECB)	———	By Requestor	Requestor's	Word	Via address contained at offset 5 of the IOB.
Input/Output Block (IOB)	———	By Requestor	Requestor's	32 Bytes, plus a Variable Amount that Depends Upon the Access Method	Initially, address is provided in register 1 by requestor. It is moved to and maintained in register 2 (IOBREG).
Logical Channel Table (LCH)	LCHTAB IECILCH	System Generation	Nucleus	One Double-Word Logical Channel Word for Each Logical Channel Queue	To locate a needed logical channel word, the logical channel index in the UCB is multiplied by 8 and added to the beginning address of the logical channel table.
Program Status Word (PSW)		Permanent Storage Assignment			
SVC Old PSW	SVCOPSW		32 (20)		Beginning symbol.
I/O Old PSW	IOPSWO		56 (38)		Beginning symbol.
I/O New PSW	IONPSW		120 (78)		Beginning symbol.
Recovery Management Support Communication Area	IORMS	System Generation	Nucleus	112 Bytes	An IORMSCOM macro instruction is used to build a DSECT. The address for the base register is obtained from the field at offset 0 of the SYS1.LOGREC DCB.
Request Queue Element (RQE)	TSTAR IECIOQET	System Generation	Nucleus	12 Bytes (MFT) 16 Bytes (MVT)	Varies depending upon status of request: Address of RQE available for assignment is contained in location NEXAVL. Address of assigned (but not queued) RQE is contained in register 1 (TSTREG). Address of the first RQE in a logical channel queue is contained in the LCHFTS field of the logical channel word for that queue.
Task Control Block (TCB)	———	By Supervisor	Nucleus	171 Bytes	Symbolic names equated to offsets of fields.
Unit Control Block (UCB)	———	System Generation	Nucleus	Variable from 24 to 288 Bytes. One UCB for Each Device Address Defined for the System.	Initially, via address contained in UCB address field of DEB. The address is moved to the request queue element. Following interruptions, the address of the UCB for the device that caused the interruption is obtained via the UCB lookup table.
UCB Lookup Table	UCBTAB IECILK1	System Generation	Nucleus	Variable, depending upon Number and Addresses of Devices, Control Units, and Channels, and Number of Zero Entries Eliminated by Table-Building Routine.	Beginning symbol.
Volume Statistics Table	———	System Generation	Nucleus	24 Bytes for Each Entry	Via address contained in field at offset 49 of the UCB containing the volume. Each entry is effectively an extension to a UCB.

Symbol Table

Symbols (or labels) are the same as those found in program listings and in the flowcharts (Program Organization section) of this manual. To find a flowchart for a labeled segment of code, look for the label in the table's Symbol column. If you find the label, a flowchart ID will be listed next to it in the chart column.

Symbol	Chart	Routine
BRTABLE	DB	System–Initiated DDR Routine
CCHHIO	BI	Channel Check Handler
CCHINT	BI	Channel Check Handler
CCHQUIT	BI	Channel Check Handler
CCHSIO	BI	Channel Check Handler
CCHSNS	BI	Channel Check Handler
CCHSSK	BI	Channel Check Handler
CCHTIOSK	BI	Channel Check Handler
CCHTIOSN	BI	Channel Check Handler
CCH005	BI	Channel Check Handler
CCH007	BI	Channel Check Handler
CCH009	BI	Channel Check Handler
CCH035	BI	Channel Check Handler
CCH041	BI	Channel Check Handler
CCH044	BI	Channel Check Handler
CCH045	BI	Channel Check Handler
CHKREPLY	DC	DDR Tape Reposition Routine
CKWAITQ	DC	DDR Tape Reposition Routine
COMPLAB	DC	DDR Tape Reposition Routine
DDRDEVCK	DB	System–Initiated DDR Routine
DDR000	DB	System–Initiated DDR Routine
DDR01	DB	System–Initiated DDR Routine
DDR02	DB	System–Initiated DDR Routine
DDR03A	DB	System–Initiated DDR Routine
DDR03B	DB	System–Initiated DDR Routine
DDR05	DB	System–Initiated DDR Routine
DDR06	DB	System–Initiated DDR Routine
DDR14	DB	System–Initiated DDR Routine
DDR14A	DB	System–Initiated DDR Routine
DDR16	DB	System–Initiated DDR Routine
DDR19	DB	System–Initiated DDR Routine
DDR28	DB	System–Initiated DDR Routine
ERPIBSET	BJ	Channel Check Handler
ER2311	BF	Error Routine Interface
FILEON	DC	DDR Tape Resposition Routine
GETRQE	DC	DDR Tape Reposition Routine
GETTCB	DC	DDR Tape Reposition Routine
IEA0AB00	AA	EXCP Validity Check Routine
IEA0DS02	BC	I/O Interruption Supervisor
IEA0EF00	BF	Error Routine Interface
IEA0PT01	BC	I/O Interruption Supervisor
IECINT	00	I/O Supervisor Overall Flow
IECINT	BA	I/O Interruption Supervisor
IECINTRP	CB	I/O Error Recovery Routines

Symbol	Chart	Routine
IECXCPER	00	I/O Supervisor Overall Flow
IECXCPER	CA	Error EXCP Routine
IEEBA1	AL	Post Start I/O Routine
IGC000	AA	EXCP Validity Check Routine
IGC015	CA	Error EXCP Routine
IGC2503D	DC	DDR Tape Reposition Routine
IGE0025C	CB	I/O Error Recovery Routines
IGE0025D	CB	I/O Error Recovery Routines
IGE0025F	CB	I/O Error Recovery Routines
IGE0525F	CB	I/O Error Recovery Routines
IGFCAT	BI	Channel Check Handler
IGFCCH35	BK	135 Channel Analysis Routine
IGFCCH48	BK	155 Channel Analysis Routine
IGFCCH60	BK	2860 Channel Analysis Routine
IGFCCH68	BK	145 Channel Analysis Routine
IGFCCH70	BK	2870 Channel Analysis Routine
IGFCCH80	BK	2880 Channel Analysis Routine
IGX00015	—	Extended SVC Routine
INTAPR01	EA	Alternate Path Retry Routine
INTAP1	EA	Alternate Path Retry Routine
INTAP7	EA	Alternate Path Retry Routine
INTAP8	EA	Alternate Path Retry Routine
INTAP9	EA	Alternate Path Retry Routine
INTAP10	EA	Alternate Path Retry Routine
INTAP12	EA	Alternate Path Retry Routine
INTAP12A	EA	Alternate Path Retry Routine
INTAP13	EA	Alternate Path Retry Routine
INTAP16	EA	Alternate Path Retry Routine
INTATT	BE	I/O Interruption Supervisor
INTATT2	AL	Post Start I/O Routine
INTATT2	BE	I/O Interruption Supervisor
INTCCH	BA	I/O Interruption Supervisor
INTCSn	00	I/O Supervisor Overall Flow
INTCSn	BD	I/O Interruption Supervisor
INTCSn	BM	Channel Search Routine, No Alternate Paths
INTCSn	BN	Channel Search Routine, Alternate Paths
INTCSn	BO	Channel Search Routine, Channels With No Direct Access Devices Requiring Seeks
INTC1C	BM	Channel Search Routine, No Alternate Paths
INTC1C	BN	Channel Search Routine, Alternate Paths
INTERR	BF	Error Routine Interface
INTERR3	BF	Error Routine Interface
INTERR4	BF	Error Routine Interface
INTER7	BF	Error Routine Interface
INTER7C	00	I/O Supervisor Overall Flow
INTER7C	CA	Error EXCP Routine
INTER8	00	I/O Supervisor Overall Flow
INTER8	CA	Error EXCP Routine
INTER9	CA	Error EXCP Routine
INTRREL	BP	Channel Search Routine
INTRREL1	BP	Channel Search Routine
INTRR00	BG	Sense Subroutine

Symbol	Chart	Routine
INTSEN	00	I/O Supervisor Overall Flow
INTSEN	BE	I/O Interruption Supervisor
INTSEN	BG	Sense Subroutine
INTS01	BG	Sense Subroutine
INTS02	BH	Sense Subroutine
INTS02A	BH	Sense Subroutine
INTS02B	BH	Sense Subroutine
INTS02D	BG	Sense Subroutine
INTS02G	BH	Sense Subroutine
INTS02H	BH	Sense Subroutine
INTS03	BG	Sense Subroutine
INTS03A	BG	Sense Subroutine
INTS04	BG	Sense Subroutine
INTS04	BH	Sense Subroutine
INTS05	BL	Teleprocessing and Shared DASD Post Sense Processing
INTTIO	BH	Sense Subroutine
INTTRAP	BB	I/O Interruption Supervisor
INTVMSA	BC	I/O Interruption Supervisor
INT002A	BA	I/O Interruption Supervisor
INT003	00	I/O Supervisor Overall Flow
INT003	BA	I/O Interruption Supervisor
INT005	00	I/O Supervisor Overall Flow
INT005	BB	I/O Interruption Supervisor
INT006	BA	I/O Interruption Supervisor
INT008	BB	I/O Interruption Supervisor
INT009	BE	I/O Interruption Supervisor
INT01A	00	I/O Supervisor Overall Flow
INT01A	BA	I/O Interruption Supervisor
INT07A	BC	I/O Interruption Supervisor
INT010	00	I/O Supervisor Overall Flow
INT010	BB	I/O Interruption Supervisor
INT010A	00	I/O Supervisor Overall Flow
INT010A	BB	I/O Interruption Supervisor
INT011	BE	I/O Interruption Supervisor
INT011B	00	I/O Supervisor Overall Flow
INT011B	BE	I/O Interruption Supervisor
INT012	BB	I/O Interruption Supervisor
INT12C	BB	I/O Interruption Supervisor
INT013	00	I/O Supervisor Overall Flow
INT013	BE	I/O Interruption Supervisor
INT014	BA	I/O Interruption Supervisor
INT014	BB	I/O Interruption Supervisor
INT019	BB	I/O Interruption Supervisor
INT019B	00	I/O Supervisor Overall Flow
INT019B	CA	Error EXCP Routine
INT022	BF	Error Routine Interface
INT023	00	I/O Supervisor Overall Flow
INT023	BC	I/O Interruption Supervisor
INT024	00	I/O Supervisor Overall Flow
INT024	BC	I/O Interruption Supervisor

Symbol	Chart	Routine
INT024B	BC	I/O Interruption Supervisor
INT025	BC	I/O Interruption Supervisor
INT025A	00	I/O Supervisor Overall Flow
INT025A	BC	I/O Interruption Supervisor
INT025B	BC	I/O Interruption Supervisor
INT027	BC	I/O Interruption Supervisor
INT031	00	I/O Supervisor Overall Flow
INT031	AF	Start I/O Routine for Direct–Access Devices
INT031	BE	I/O Interruption Supervisor
INT031B	00	I/O Supervisor Overall Flow
INT031B	BF	Error Routine Interface
INT031B	BH	Sense Subroutine
INT031B	BM	Channel Search Routine, No Alternate Paths
INT031B	BN	Channel Search Routine, Alternate Paths
INT031B	BO	Channel Search Routine, Channels With No Direct Access Devices Requiring Seeks
INT033	00	I/O Supervisor Overall Flow
INT033	BD	I/O Interruption Supervisor
INT033C	BD	I/O Interruption Supervisor
INT034	BM	Channel Search Routine, No Alternate Paths
INT034	BN	Channel Search Routine, Alternate Paths
INT034	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT034A	BM	Channel Search Routine, No Alternate Paths
INT034A	BN	Channel Search Routine, Alternate Paths
INT034A	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT034C	BM	Channel Search Routine, No Alternate Paths
INT034C	BN	Channel Search Routine, Alternate Paths
INT034C	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT034D	BM	Channel Search Routine, No Alternate Paths
INT034D	BN	Channel Search Routine, Alternate Paths
INT034D	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT034G	AB	Get Request Element Routine
INT034G	BM	Channel Search Routine, No Alternate Paths
INT034G	BN	Channel Search Routine, Alternate Paths
INT034G	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT036	BM	Channel Search Routine, No Alternate Paths
INT036	BN	Channel Search Routine, Alternate Paths
INT036C	BM	Channel Search Routine, No Alternate Paths
INT036C	BN	Channel Search Routine, Alternate Paths

Symbol	Chart	Routine
INT038	BM	Channel Search Routine, No Alternate Paths
INT038	BN	Channel Search Routine, Alternate Paths
INT038	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT038B	BM	Channel Search Routine, No Alternate Paths
INT038B	BN	Channel Search Routine, Alternate Paths
INT038B	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
INT050A	BF	Error Routine Interface
INT055	BF	Error Routine Interface
INT057	BF	Error Routine Interface
INT058	BF	Error Routine Interface
INT059	BF	Error Routine Interface
INT12B	00	I/O Supervisor Overall Flow
INT12B	BC	I/O Interruption Supervisor
INT12C	AF	Start I/O Routine for Direct–Access Devices
INT17A	BC	I/O Interruption Supervisor
IOTAPE	DC	DDR Tape Reposition Routine
NSLREPOS	DC	DDR Tape Reposition Routine
OPDDR03	DA	Operator–Initiated DDR Routine
OPDDR05	DA	Operator–Initiated DDR Routine
OPDDR15	DA	Operator–Initiated DDR Routine
OPDDR15A	DA	Operator–Initiated DDR Routine
OPDDR17	DA	Operator–Initiated DDR Routine
OPDDR18A	DA	Operator–Initiated DDR Routine
OPDDR18B	DA	Operator–Initiated DDR Routine
OPDDR21	DA	Operator–Initiated DDR Routine
OPDDR22	DA	Operator–Initiated DDR Routine
PRGCOMA	BC	I/O Interruption Supervisor
PRGCOMB	BC	I/O Interruption Supervisor
PROCDMSG	DC	DDR Tape Reposition Routine
PURGECHK	DB	System–Initiated DDR Routine
SERR01	AL	Post Start I/O Routine
SERR04	AL	Post Start I/O Routine
SERR04	BA	I/O Interruption Supervisor
SERR04	BH	Sense Subroutine
SWAPMSG	DC	DDR Tape Reposition Routine
TRACE	AK	Start I/O Subroutine
UCBSCH	BI	Channel Check Handler
VALCHK	AA	I/O Interruption Supervisor
VALCHK2	AA	EXCP Validity Check Routine
VERIFYON	DC	DDR Tape Reposition Routine
WTORWAIT	DB	System–Initiated DDR Routine
XCPCH	AC	Test Channel Routines
XCPPDQ	AA	EXCP Validity Check Routine 0
XCPPDQ	AB	Get Request Element Routine
XCPPDQ	AF	Start I/O Routine for Direct–Access Devices
XCPPDQ	AK	Start I/O Subroutine

Symbol	Chart	Routine
XCPPDQ	AL	Post Start I/O Routine
XCPPDQ	BH	Sense Subroutine
XCPPDQ	BM	Channel Search Routine, No Alternate Paths
XCPPDQ	BN	Channel Search Routine, Alternate Paths
XCPPDQ	BO	Channel Search Routine, Channels With No Direct–Access Devices Requiring Seeks
XCPPIO	AL	Post Start I/O Routine
XCPPI02	00	I/O Supervisor Overall Flow
XCPPI02	AL	Post Start I/O Routine
XCPPI04	AL	Post Start I/O Routine
XCPPNQ	00	I/O Supervisor Overall Flow
XCPPNQ	AB	Get Request Element Routine
XCPPNQB	BC	I/O Interruption Supervisor
XCPPNQB	BF	Error Routine Interface
XCPPNQB	CA	Error EXCP Routine
XCPPST	BC	I/O Interruption Supervisor
XCPRR007	AG	Start I/O Routine for Direct–Access Devices
XCPR008B	AG	Start I/O Routine for Direct–Access Devices
XCPSIO	AD	Start I/O Routine for Unit Record and Communications Devices
XCPSIO	AE	Start I/O Routine for Magnetic–Tape Devices
XCPSIO	AK	Start I/O Subroutine
XCPTCH	00	I/O Supervisor Overall Flow
XCPTCH	AC	Test Channel Routines
XCPTCH3	AC	Test Channel Routines
XCPTST	00	I/O Supervisor Overall Flow
XCPTST	AB	Get Request Element Routine
XCPTST2	AB	Get Request Element Routine
XCP010A	00	I/O Supervisor Overall Flow
XCP010A	AB	Get Request Element Routine
XCP011	AB	Get Request Element Routine
XCP020	AB	Get Request Element Routine
XCP021	BD	I/O Interruption Supervisor
XCP03E	AG	Start I/O Routine for Direct–Access Devices
XCP052	AL	Post Start I/O Routine
XCP054	AK	Start I/O Subroutine
XCP054A	AK	Start I/O Subroutine
XCP056C	AL	Post Start I/O Routine
XCP056E	00	I/O Supervisor Overall Flow
XCP056E	AL	Post Start I/O Routine
XCP060	AA	EXCP Validity Check Routine
XCP061C	AA	EXCP Validity Check Routine
XCP064	AA	EXCP Validity Check Routine
XCP064	BC	I/O Interruption Supervisor
XCP070	AB	Get Request Element Routine
XCP072	AB	Get Request Element Routine
XCP110	AK	Start I/O Subroutine
XCP110B	AK	Start I/O Subroutine
XCP110C	00	I/O Supervisor Overall Flow
XCP110C	AK	Start I/O Subroutine

Symbol	Chart	Routine
XCP111	AG	Start I/O Routine for Direct–Access Devices
XCP111	AK	Start I/O Subroutine
XCP111B	00	I/O Supervisor Overall Flow
XCP111B	AK	Start I/O Subroutine
XCP112	AK	Start I/O Subroutine
XCP120	AD	Start I/O Routine for Unit–Record and Communications Devices
XCP121	AD	Start I/O Routine for Unit–Record and Communications Devices
XCP130	AD	Start I/O Routine for Unit–Record and Communications Devices
XCP130	AE	Start I/O Routine for Magnetic–Tape Devices
XCP131	AE	Start I/O Routine for Magnetic–Tape Devices
XCP133	AE	Start I/O Routine for Magnetic–Tape Devices
XCP160	AH	Start I/O Routine for Direct–Access Devices
XCP161	AG	Start I/O Routine for Direct–Access Devices
XCP162	AG	Start I/O Routine for Direct–Access Devices
XCP163	AH	Start I/O Routine for Direct–Access Devices
XCP167	AG	Start I/O Routine for Direct–Access Devices
XEXCP	00	I/O Supervisor Overall Flow
XEXCP	AA	EXCP Validity Check Routine
XIODSK	AF	Start I/O Routine for Direct–Access Devices
XIODSK1	AF	Start I/O Routine for Direct–Access Devices
XIOTPE	AE	Start I/O Routine for Magnetic–Tape Devices
XIOTP06	AE	Start I/O Routine for Magnetic–Tape Devices
XIOUR	AD	Start I/O Routine for Unit–Record and Communications Devices
XVCK01	AA	EXCP Validity Check Routine
XVCK01	CA	Error EXCP Routine

SECTION 5: DATA AREAS

Data Area Relationships

Data Area Layouts

Data Area Relationships

The major paths by which I/O supervisor routines can reach specific data areas are shown in Figure 13. The longer paths are seldom used, because pointers to major data areas are normally maintained in registers. For example IOBREG, which is register 2, will normally contain the address of the input/output block (IOB) for a request in process. One exception is the Purge routine, which must use the longer paths in locating and removing elements from queues.

Data Area Layouts

This section contains descriptions of the principal data areas used by routines of the I/O supervisor.

In some cases major portions of the block, not relevant to the functions of the I/O supervisor, are omitted. In those cases, a reference is made to a publication where a more complete description can be found.

Some of the data areas (for example, the CAW, CSW, and the PSW) are fully described in the publications *IBM System/360 Principles of Operation,* GA22–6821, and *IBM System/370 Principles of Operation,* GA22–7000. The descriptions of those data areas in this section are therefore condensed. They are meant to minimize, but not to eliminate, references to those publications.

The symbolic names shown in individual data area fields represent the offset, in bytes, from the beginning of a table to the field. Access is gained to a specific field by using an instruction in which the beginning address of the table (usually contained in a register) is the base address, and the symbolic field name represents the displacement.

There are places where the symbolic field names will differ from names used in other publications. Names used here were taken from I/O supervisor listings, and where differences exist, a non–I/O supervisor program may refer to the field by the other name. (To resolve name differences, compare offsets; if the offsets match, the names represent the same field.)

Usage of the data area fields can be traced in the I/O supervisor listings by first locating the symbolic field names in the cross–reference table at the back of the listings and then noting where the names are used. Where no symbolic name appears in a data area field, the field is most likely not referred to by the I/O supervisor.

The page format used for data area field description is identical to that used in the publication *OS System Control Blocks,* GC28–6628. The field headings and their meanings are:

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning

Offset—The numeric address of the field relative to the beginning of the data area.

The first number is the offset in decimal, followed (in parentheses) by the hexadecimal equivalent.

Example:
16 (10)

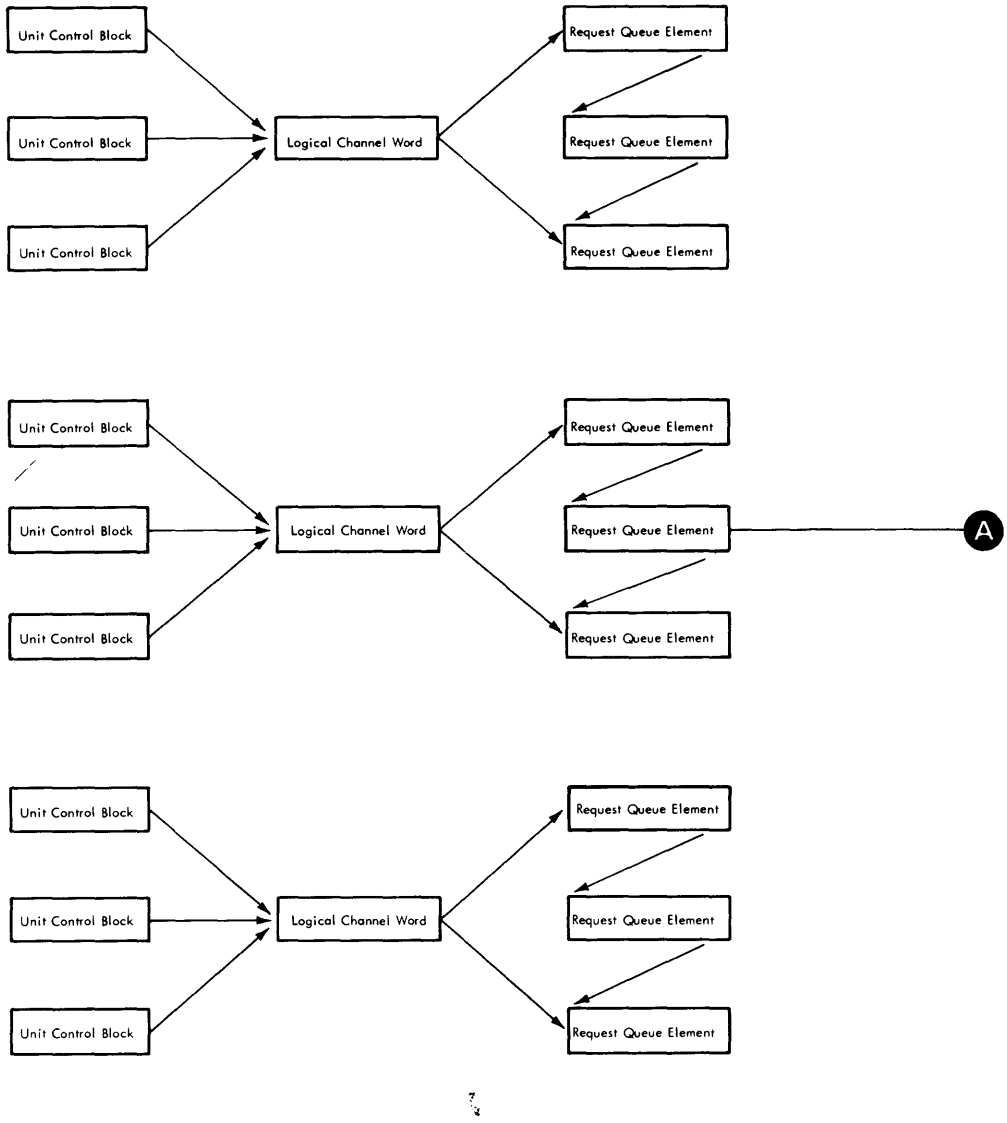
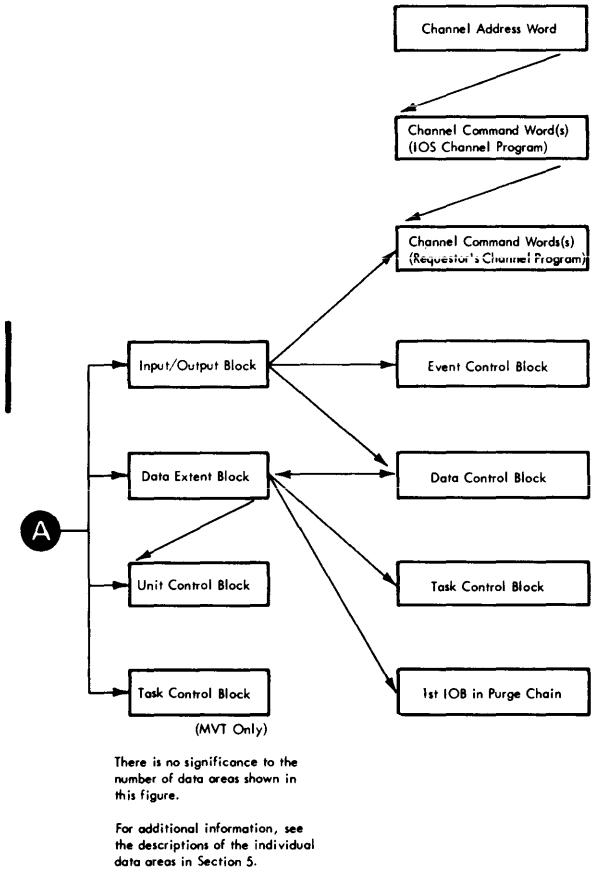


Figure 13. Data Area Relationships



There is no significance to the number of data areas shown in this figure.

For additional information, see the descriptions of the individual data areas in Section 5.

Data Area Name	Offset	Field Name	Content
Data Extent Block	1(1)	DEBTCBAD	† Task Control Block
	17(11)	DEBUSRPG	† First IOB in Purge Chain
	25(19)	DEBDCBAD	† Data Control Block
	33(21)	DEBUCBAD	† Unit Control Block
Input/Output Block	5(5)	IOBECB	† Event Control Block
	17(11)	IOBST	† Requestor's Channel Program
	21(15)	IOBDCB	† Data Control Block
Logical Channel Word	0(0)	LCHFTS	† First RQE in Logical Channel Queue
	2(2)	LCHLTS	† Last RQE in Logical Channel Queue
Request Queue Element	0(0)	TSTLNK	† Next RQE in Logical Channel Queue
	2(2)	TSTUCB	† Unit Control Block
	5(5)	TSTIOB	† Input/Output Block
	9(9)	TSTDEB	† Data Extent Block
	15(0F)	TSTTCB	† Task Control Block (MVT only)
Unit Control Block	10(A)	UCBLCI	Value which, when multiplied by 8, becomes an index to the logical channel word for the logical channel containing the device.

Figure 13. Data Area Relationships

Bytes and Alignment—The size (number of bytes) of the field and its alignment relative to the fullword boundary.

Examples:

4 . . .	A 4–byte field beginning on a word boundary.
. . 2 .	A 2–byte field beginning on a halfword boundary.
. . . 1	A 1–byte field in the low–order byte of a word.
. . . 3	A 3–byte field beginning at the low–order byte of a word (and running into the next word).

Field Name—A name that identifies the field.

This column is also used to show the bit settings of flag fields; that is, the state of bits in a byte. When the column is used to show the state of bits (0, 1), in a flag byte, it is shown as follows:

....	The 8 bit positions (0 – 7) in a byte. For ease of scanning, the high–order (left–hand) 4 bits are separated from the low–order 4 bits.
x...	A reference to bit 0.
1...	Bit 0 is on.
0...	Bit 0 is off.
.... ..xx	A reference to bits 6 and 7.

Bit settings that are significant are shown and described. Bit settings that are not presently significant are described as reserved bits. Do not use these bits because the Operating System may make use of them in the future.

Field Description, Contents, Meaning—The use of the field.

Where a field's contents relate directly to a value coded by the user (generally in job control statements) the value coded is shown under the heading:

Code—The value coded by the user that resulted in the described contents.

Alternate Path Table

The alternate path table (Figure 14) contains a record of the paths by which a device can be reached. There is one alternate path table for each logical channel that contains more than one channel. In the listings, an alternate path table immediately precedes the Test Channel routine for its associated channel.

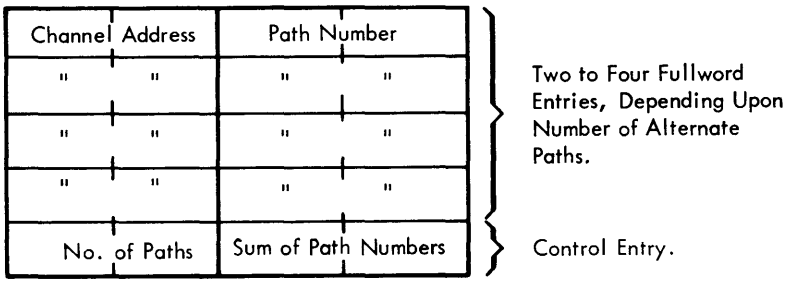


Figure 14. Alternate Path Table

Channel Address Word

The channel address word (Figure 15) is referred to by a channel during execution of a Start I/O instruction. It is the means by which the channel can determine the main storage location from which it should fetch the first channel command word (CCW). The channel address word is permanently assigned to main storage location 72.

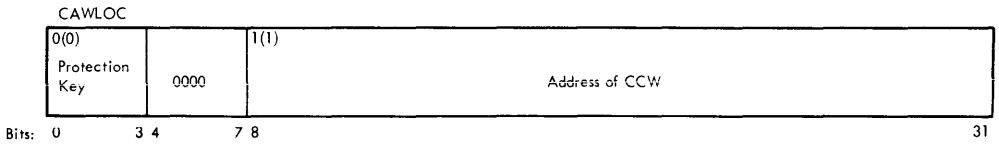


Figure 15. Channel Address Word

CHANNEL ADDRESS WORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CAWLOC	Protection Key. In systems having the data set protection feature, contains the requestor's protection key. Otherwise, contains zeros.
1(1)	. 3		The main–storage address of the first CCW to be executed.

Channel Availability Table

The channel availability table (Figure 16) exists only in those systems where the M65MP option has been selected. There is one channel availability table for each of the two CPUs, located in the prefixed storage area for that CPU. The table contains flags that are used in determining if a channel of the other CPU is available.

For convenience, other data areas located adjacent to the channel availability table in the prefixed storage area are also shown and described.

CHANNEL AVAILABILITY TABLE AND ADJACENT DATA AREAS

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	4		Address of the M65MP extension to the communication vector table.
4(4)	2	CHAN0	Channel 0 flags. Second byte not used.
		1...	Channel busy. Set to 1 by EXCP supervisor following SIO. Set to 0 by interruption supervisor after channel end.
		.1..	Channel not operational. Set to 1 by the nucleus initialization program (NIP) if the channel responds "not operational" (cc=3) to test channel instruction. This flag is also set to 1 following a Vary Channel command placing the channel offline.

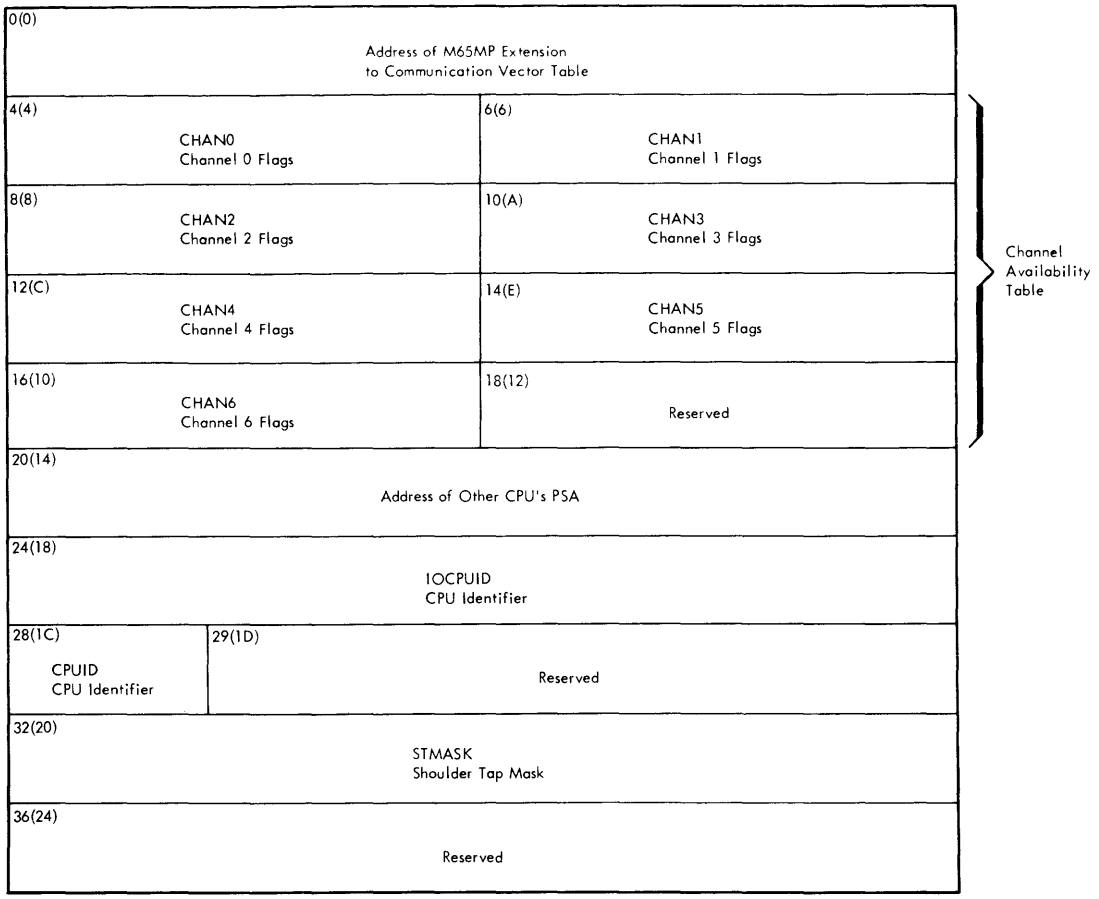


Figure 16. Channel Availability Table and Adjacent Data Areas

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		..1.	Channel not in system. Set to 1 by NIP if the channel is not included in system generation.
		...1	Channel not available. Assembled as a 1, and set to 0 by NIP following a Test Channel response indicating availability. This flag is also set to 1 after a Vary CPU command placing the channel's CPU offline.
		.... x...	Not used.
		xxx	The physical channel address, from 0 through 6.
6(6)	. 2	CHAN1	Channel 1 flags. Same as channel 0 flags.
8(8)	2	CHAN2	Channel 2 flags. Same as channel 0 flags.
10(A)	. 2	CHAN3	Channel 3 flags. Same as channel 0 flags.
12(C)	2	CHAN4	Channel 4 flags. Same as channel 0 flags.
14(E)	. 2	CHAN5	Channel 5 flags. Same as channel 0 flags.
16(10)	2	CHAN6	Channel 6 flags. Same as channel 0 flags.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
18(12)	. 2		Reserved.
20(14)	4		Address of the other CPU's prefixed storage area (PSA).
24(18)	4	IOCPUID	CPU identifier. Set by NIP to X'00000000' for CPU A and X'00000008' for CPU B. Used by EXCP supervisor to set bit 4 of the M65MP flags in the UCB following SIO. The interruption supervisor uses this field to test the UCB flags following an interruption. If the setting does not match, the interruption is identified as the second of two device ends presented when a device changes status from "not ready" to "ready". Some control units present one device end for this change to each attached channel.
28(1C)	1	CPUID	CPU identifier. An identifier set by NIP to X'C1' (EBCDIC'A') for CPU A and to X'C2' (EBCDIC'B') for CPU B.
29(1D)	. 3		Reserved.
32(20)	4	STMASK	Shoulder tap mask. Bit settings in the shoulder tap mask are tested by the receiving CPU following a shoulder tap to see what actions are requested. In each case the performing CPU resets the flag to 0 when the action is completed.
		Bit 0	A Write Direct instruction has already been issued, but not accepted by the other CPU. Additional bits may be set on without issuing another Write Direct instruction.
		Bit 6	Halt I/O requested.
		Bit 16	A Quiesce command is pending.
		Bit 17	A Vary CPU command is pending.
		Bits 24–31	Start I/O requested. (X'01')

Channel Command Word

The channel command word (CCW, Figure 17) indicates to a channel what I/O operation it should start. For operations involving data transfer, the CCW also indicates the main storage location into which data is to be placed or read from, and how many bytes of data are to be transferred.

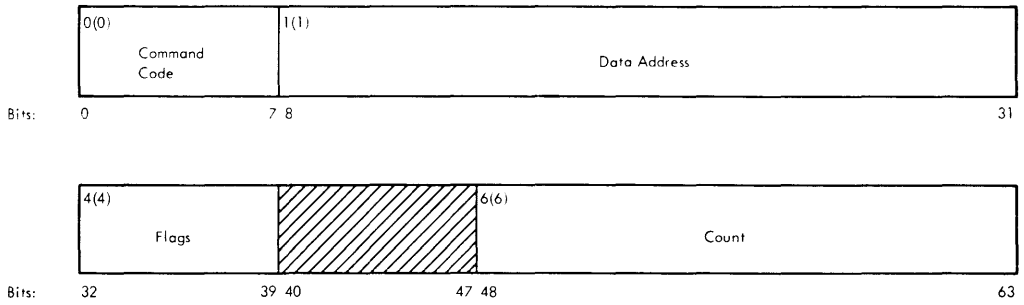


Figure 17. Channel Command Word

CHANNEL COMMAND WORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1		Command code. Specifies the operation to be performed.
1(1)	. 3		Data address. Specifies the main storage location of a data area. Depending upon the command code, data is either read from or placed into the data area during an I/O operation involving data transfer.
4(4)	1	10..	Chain–Data (CD) flag. The data area designated by the next CCW is to be used with the current operation.
		01..	Chain–Command (CC) flag. The operation specified by the command code of the next CCW is to be initiated on normal completion of the current operation.
		..1.	Suppress–Length–Indication (SLI) flag. The incorrect length status bit in the channel status word is not to be set by the channel if it detects an incorrect–length condition.
		...1	Skip flag. Data transfer to main storage is to be suppressed. This flag is valid only for read, read backward, and sense operations.
		.... 1...	Program controlled interruption (PCI) flag. The channel is to cause an interruption when this CCW is executed.
		.... .000	Must be zeros for every CCW except for those CCWs specifying a transfer in channel operation.
6(6)	. . 2		Count. Specifies the number of bytes in the data area associated with this CCW.

Channel Error Block Table

The channel error block table (Figure 18) is used by the optional alternate path retry routines. It contains entries (Figure 19) used to keep track of the failing paths to a device. (Alternate path retry routines remove failing paths from contention so that retries are only attempted on remaining non–failing paths.)

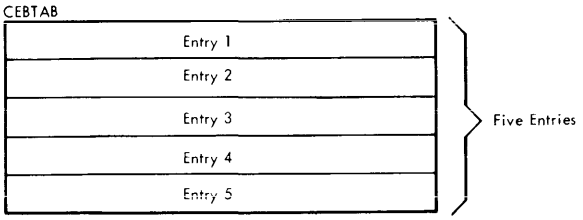


Figure 18. Channel Error Block Table

Figure 19. Channel Error Block Table Entry

CHANNEL ERROR BLOCK TABLE ENTRY

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CEBINA	Active/inactive indicator:
			Content (Hex.) — Meaning
			01 — Used only in the first CEB. Indicates there is at least one active CEB in the CEB table.
			FE — This CEB is active.
1(1)	. 1	CEBCHMSK	Failing path mask. Zeros indicate failing paths.
2(2)	. . 2	CEBRQE	Address of RQE for the failing request.

Channel Status Word

The channel status word (CSW, Figure 20) indicates to a program the status of an I/O device, control unit, channel, and subchannel. The CSW is assigned permanently to main storage location 64. Information is stored in the CSW by a channel after an I/O interruption, and also during execution of the Start I/O, Test I/O, and Halt I/O instructions.

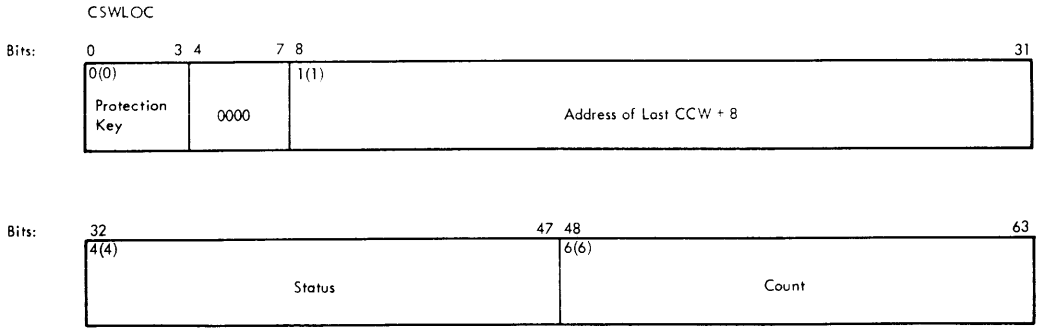


Figure 20. Channel Status Word (CSW)

CHANNEL STATUS WORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	xxxx	Protection Key. In systems having the data set protection feature, contains the requestor's protection key. Otherwise, contains zeros.
		 0000	Always zeros.
1(1)	. 3		A main–storage address which is eight higher than the address of the last executed CCW.
4(4)	2	Status Byte 1	
		1...	Attention.
		.1..	Status modifier.
		..1.	Control unit end.
		...1	Busy.
		.... 1...	Channel end
		.... .1..	Device end.
		.... ..1.	Unit check.
		1	Unit exception.
		Status Byte 2	
		1...	Program–controlled interruption.
		.1..	Incorrect length.
		..1.	Program check.
		...1	Protection check.
		.... 1...	Channel data check.
		.... .1..	Channel control check.
		.... ..1.	Interface control check.
		1	Chaining check.
6(6)	. . 2		Count. The number of bytes of data that remained to be transferred after the last CCW was executed.

Channel Table

The channel table is composed of entries containing addresses of Channel Search routines, arranged in channel number order (Figure 21). It is used when a channel becomes free and a channel–dependent Channel Search routine is needed to select requests that should be started next. The format of a channel table entry is shown in Figure 22.

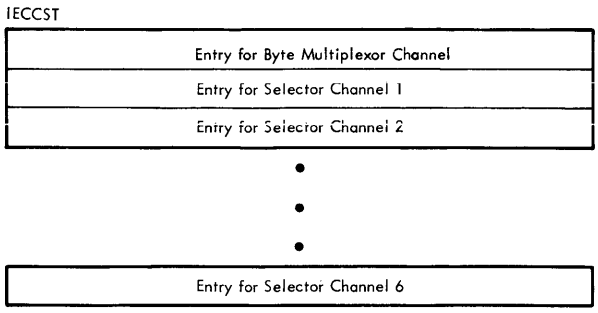


Figure 21. Channel Table

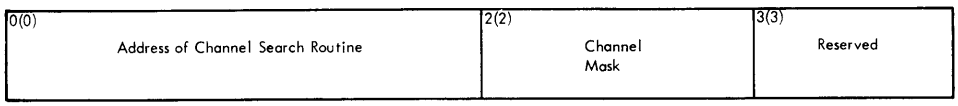


Figure 22. Channel Table Entry

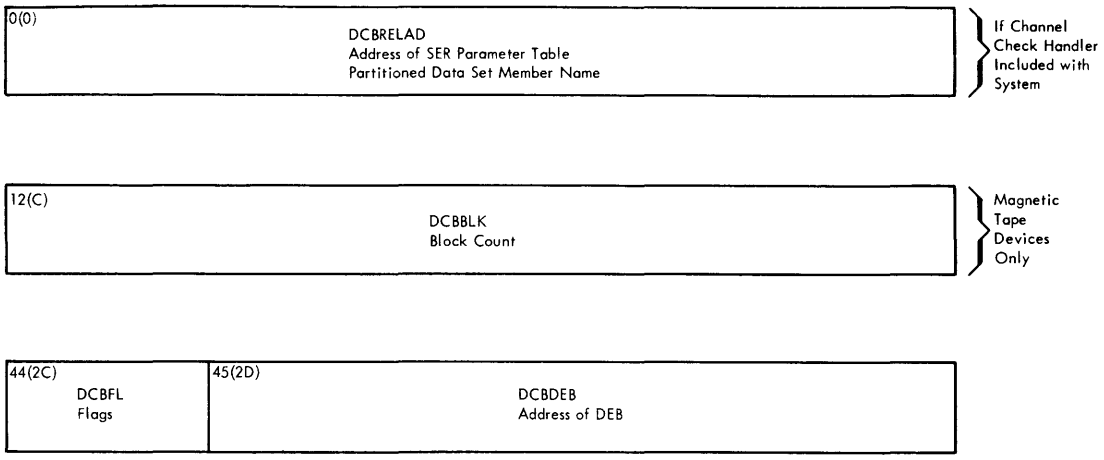
CHANNEL TABLE ENTRY

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	2		Address of the Channel Search routines for the channel represented by this entry
2(2)	1		Channel mask
		1000 0000	Channel 0
		0100 0000	Channel 1
		0010 0000	Channel 2
		0001 0000	Channel 3
		0000 1000	Channel 4
		0000 0100	Channel 5
		0000 0010	Channel 6
		0000 0001	Channel 7

Data Control Block

Data control blocks (DCBs) describe the current use of a data set. For every data set to be processed by a program, there is a corresponding DCB.

Although they are maintained primarily by data management routines, DCBs do contain a limited amount of information maintained or referred to by the I/O supervisor (Figure 23).



The symbolic names of fields in this control block may not agree with names used in other publications. For additional information, see the explanation at the beginning of the Data Area Layouts section.

Figure 23. Data Control Block Fields Used by the I/O Supervisor

DATA CONTROL BLOCK

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	4	DCBRELAD	If the system has the Channel Check Handler, contains the address of a 12–byte parameter list. In MFT systems, the list is in control section IEAAIH00; in MVT systems it is in control section IEAQFX00. If the system does not have the Channel Check Handler, contains the address of a partitioned data set member currently being used.
12(C)	4	DCBBLK	A count of the number of blocks read from or written onto magnetic tape. After a successful I/O operation, this value is increased by an increment provided by the requestor in his IOB. The addition takes place in the tape trapcode routine.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
44(2C)	1	DCBFL	Used in communicating error conditions to a requestor and in determining corrective procedures.
		00.....	Not in error procedure.
		01.....	Error correction in process.
		11.....	Permanent error condition.
		..10....	Channel 9 printer carriage tape punch sensed.
		..01....	Channel 12 printer carriage tape punch sensed.
		.... 00..	Always use I/O supervisor error routine.
		.... 11..	Never use I/O supervisor error routine.
		.... 01..	Never use I/O supervisor error routine.
		.... 10..	Never use I/O supervisor error routine.
		xx	Reserved.
45(2D)	. 3	DCBDEB	Address of data extent block for the data set.

Data Extent Block

The data extent block (DEB) contains an extension of information in the data control block (DCB). Every DEB is associated with a DCB, and the two point to each other. The DEB contains information concerning the physical characteristics of a data set.

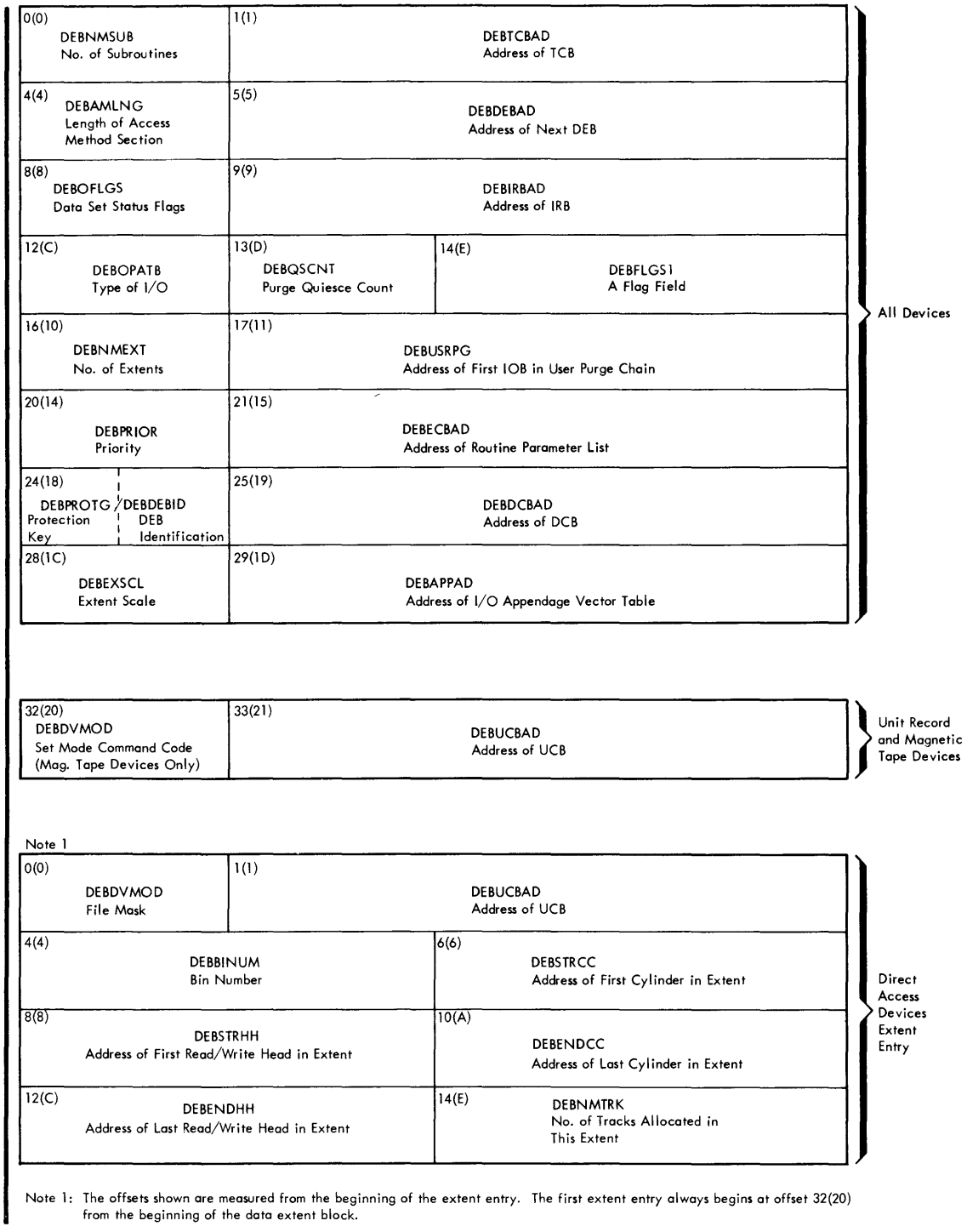
Each DEB (Figure 24) consists of one 32–byte base plus:

- One 4–byte extension if the data set is to be processed on unit–record or magnetic–tape devices
- One 16–byte extension for each extent if the data set is to be processed on a direct–access device

There are special forms of DEBs that are not described here. A complete description is contained in the publication *OS System Control Blocks,* GC28–6628.

DATA EXTENT BLOCK

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	DEBNMSUB	Number of subroutines loaded by the open executor routines.
1(1)	. 3	DEBTCBAD	Address of requestor's TCB.
4(4)	1	DEBAMLNG	Number of bytes in the access method dependent section. For BDAM this field contains the length expressed in number of words.
5(5)	. 3	DEBDEBAD	Address of next DEB for the same task.
8(8)	1	DEBOFLGS	Data set status flags.
		01..	Disposition is OLD.
		10..	Disposition is MOD.
		11..	Disposition is NEW.
		..1.	EOV or EOF.
		...1	Release unused external storage.



Note 1: The offsets shown are measured from the beginning of the extent entry. The first extent entry always begins at offset 32(20) from the beginning of the data extent block.

Figure 24. Data Extent Block (DEB) Fields Used by the I/O Supervisor

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		.... 1...	DCB modification.
		.... .1..	Split cylinder.
		.... ..1.	Nonstandard labels.
		1	Use reduced error recovery procedure (magnetic–tape devices only).
9(9)	. 3	DEBIRBAD	Address of IRB used for appendage asynchronous exits.
12(C)	1	DEBOPATB	The method of input/output processing and the disposition that is to be performed when an end–of–volume condition occurs.
		0...	(always zero)
		.1..	(MVT only) Set by ABEND to indicate SYSABEND or SYSUDUMP data set.
		..01	REREAD
		..11	LEAVE
		 0000	INPUT
		 1111	OUTPUT
		 0011	INOUT
		 0111	OUTIN
		 0001	RDBACK
		 0100	UPDAT
13(D)	. 1	DEBQSCNT	Purge quiesce count. When Purge (SVC16) is issued with the quiesce function, this field contains the count of the active devices associated with the data extent block.
14(E)	. . 2	DEBFLGS1	A flag field.
16(10)	1	DEBNMEXT	Number of extents. The number of direct–access device extent entries in this DEB.
17(11)	. 3	DEBUSRPG	The address of the first IOB in the user purge chain.
20(14)	1	DEBPRIOR	The priority of the requestor's task.
21(15)	. 3	DEBECBAD	The address of a parameter list used to locate PURGE ECB of an SVC purge quiesce request.
24(18)	1	DEBPROTG, DEBDEBID	
		xxxx	Requestor's protection key.
		 1111	Identifies this block as a DEB.
25(19)	. 3	DEBDCBAD	Address of DCB associated with this DEB.
28(1C)	1	DEBEXSCL	Extent scale: 4 for direct–access devices, 2 for nondirect–access and communications devices. Used in determining the size of the device–dependent section of this DEB.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
29(1D)	. 3	DEBAPPAD	Address of I/O appendage vector table.
32(20)	1	DEBDVMOD	Operation code of Set Mode command (magnetic–tape devices only.)
		00..	200 BPI
		01..	556 BPI
		10..	800 BPI
		..10 1...	Even parity
		..11 1...	Odd parity
33(21)		DEBUCBAD	Address of UCB for device associated with this data set.

DIRECT–ACCESS STORAGE DEVICES

EXTENT DESCRIPTION SEGMENTS: For each extent there is one 16–byte segment as follows:

0(0)	1	DEBDVMOD*	File mask for Set File Mask command. The file mask describes the Write and Seek commands that can be performed in a CCW chain.
1 (1)	. 3	DEBUCBAD*	Address of the UCB for the device associated with this data set.
4(4)	2	DEBBINUM	The cell number for an IBM 2321 Data Cell Drive. Zero for all other devices.
6(6)	. . 2	DEBSTRCC	The starting cylinder number on all devices except the IBM 2321 Data Cell Drive. For the 2321, contains the starting subcell and strip number.
8(8)	2	DEBSTRHH	The starting read/write head number on all devices except the IBM 2321 Data Cell Drive. For the 2321, contains the starting cylinder number and read/write head number.
10(A)	. . 2	DEBENDCC	The ending cylinder number on all devices except the IBM 2321 Data Cell Drive. For the 2321, contains the ending subcell and strip number.
12(C)	2	DEBENDHH	The ending read/write head number on all devices except the IBM 2321 Data Cell Drive. For the 2321, contains the ending cylinder number and read/write head number.
14(E)	. . 2	DEBNMTRK	The number of tracks allocated in this extent.

*Access to these fields is gained via the beginning of the DEB. Access to the remaining fields is via the beginning of the direct section of the DEB.

Device Statistics Table

The device statistics table contains counters that are used to keep track of the number of times error conditions have occurred on I/O devices.

There is one 10–byte entry in the device statistics table for each I/O device in a system; in addition, there is a 10–byte control field at the beginning of the table which is used in locating entries to be updated (Figure 25).

In the case of the 3400 tape devices, a 20–byte statistics table entry is allocated for each device in a system.

There are four general formats of device statistics table entries (Figure 26). Bytes 0 through 7 of every entry contain as many four–bit counters as are needed to keep the relevant statistics for the device. Bytes 8 and 9 of each entry are work areas into which error routines place bit patterns indicating which counters are to be incremented.

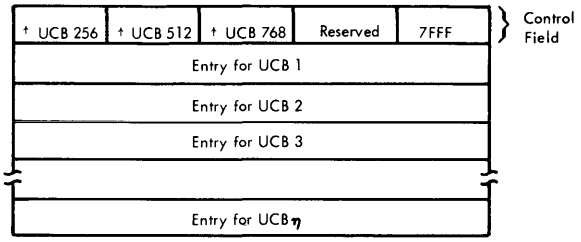


Figure 25. Device Statistics Table

Unit Record Devices

0(0) Temporary Read Failures	Temporary Write Failures	1(1)	Bus–Out Check	2(2) Equipment Check	Overrun	3(3) Device Dependent (Sense Byte 6)	Device Dependent (Sense Byte 7)
4(4)		5(5)		6(6)		7(7)	
8(8) Work Area		9(9) Work Area					

2400/3400 Series Magnetic Tape Devices

0(0) Temporary Read Failures	Temporary Write Failures	1(1) Intervention Required	Bus–Out Check	2(2) Equipment Check	Overrun	3(3) Ward Count Zero	Data Converter Check
4(4) Read/Write Vert. Red. Check	Longitudinal Redundancy Check	5(5) Skew	Cyclic Redundancy Check	6(6) Skew Reg. Vert. Red. Check	Noise	7(7) Read Opposite Recovery	Channel Data Check
8(8) Work Area		9(9) Work Area					

Figure 26 (Part 1 of 2). Device Statistics Table Entries

Devices Attached to 2820 Control Units

0(0) Temporary Read Failures / Temporary Write Failures	1(1) Bus-Out Check	2(2) Equipment Check	3(3) Track Condition Check
4(4) Track Overrun	5(5)	6(6) No Record Found	7(7)
8(8) Work Area	9(9) Work Area		

Devices Attached to 2841 Control Units

0(0) Temporary Read Failures / Temporary Write Failures	1(1) Bus-Out Check	2(2) Equipment Check / Overrun	3(3) Track Condition Check / Seek Check
4(4) Unsafe	5(5) Serializer/ Deserializer / Control Unit Tag Line	6(6) Arithmetic Logical Unit	7(7) Missing Address Marker
8(8) Work Area	9(9) Work Area		

3410 Series Magnetic Tape Devices

0(0)	1(1) Noise 1,0	2(2) VRC 3,0	3(3) MTE/LRCR 3,1
4(4) EDC/CRC 3,3	5(5) Envelope Check 3,4	6(6) Overrun 0,5 / Skew 3,2	7(7) Spare 3,7 / Spare 4,3
8(8) PE ID CH 5,3 / Mask Bit Expansion / P	9(9) Track in Error Mask Bits 2,0-7 (0 1 2 3 4 5 6 7)	10(A) Write TM Check 5,2 / Parity Compare 5,4	11(B) Tach Check 5,5 / False End Mark 5,6
12(C) Spare 8,0 / Feed-Through Check 8,1	13(D) Spare 8,2 / End Velocity Check 8,3	14(E) No Readback Data 8,4 / Start Velocity Check 8,5	15(F) Spare 8,6 / Marginal Velocity 8,7
16(10) Not Used 9,0 / Not Used 9,1	17(11) Not Used 9,2 / Not Used 9,3	18(12) Backward 3,6	19(13) Bus Out Check 0,2 / Tape Unit Positioning Check 4,0

3420 Series Magnetic Tape Devices

0(0)	1(1) Noise 1,0	2(2) Read Write VRC 3,0	3(3) MTE/LRCR 3,1
4(4) EDC/CRC 3,3	5(5) Envelope Check /VRC 3,4	6(6) Overrun 0,5 / Skew 3,2	7(7) C-Compare 3,7 / Write Trigger VRC 4,3
8(8) PE ID CH 5,3 / Mask Bit Expansion / P	9(9) Track in Error Mask Bits 2,0-7 (0 1 2 3 4 5 6 7)	10(A) Write TM Check 5,2 / Start Read Check 5,4	11(B) Partial Record 5,5 / Excessive Post Amble or TM 5,6
12(C) IBG Drop While Writing 8,0 / Feed-Through Check 8,1	13(D) Spare 8,2 / Early Begin Read Back Check 8,3	14(E) Early Begin Read Back Check 8,4 / Slow Begin Read Back Check 8,5	15(F) Slow End Read Back Check 8,6 / Velocity Retry 8,7
16(10) Not Used 9,0 / Vel. Change During Write 9,1	17(11) Not Used 9,2 / Not Used 9,3	18(12) Backward 3,6	19(13) Bus Out Check 0,2 / ALV Hardware Error 4,0

Figure 26 (Part 2 of 2). Device Statistics Table Entries

Note: The sense byte and bit corresponding to each error counter and mask is indicated. (for example, 1,0 = Sense Byte 1, Bit 0)

Device Table

The device table (Figure 27) provides the I/O supervisor with a means for obtaining the addresses of certain device—and queuing—option dependent routines. The format of a device table entry is shown in Figure 28.

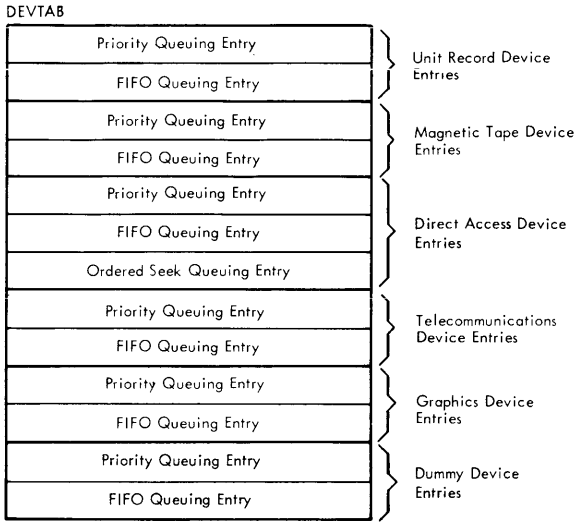


Figure 27. Device Table

DEVICE TABLE ENTRY

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	2	DVTENQ	The address of the Enqueue routine for the queuing option represented by this entry
2(2)	. 2	DVTSIO	The address of the Start I/O routine for the device type represented by this entry
4(4)	2	DVTTRP	The address of the Trapcode routine for the device type represented by this entry
6(6)	2	DVTSEN	The address of the sense subroutine to be used for the device

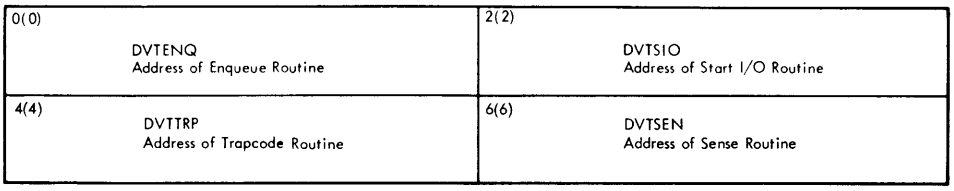


Figure 28. Device Table Entry

Error Recovery Procedure Interface Block

When there is a malfunction in a channel and the system has the Channel Check Handler routine, the failure is not automatically considered to be permanent. The Channel Check Handler routine is entered before any I/O error routine is invoked, and it produces an error recovery procedure interface block (Figure 29) that contains information pertaining to the cause of the channel failure. When the I/O error routine is invoked, it can use the error recovery procedure interface block to determine whether or not a retry should be attempted.

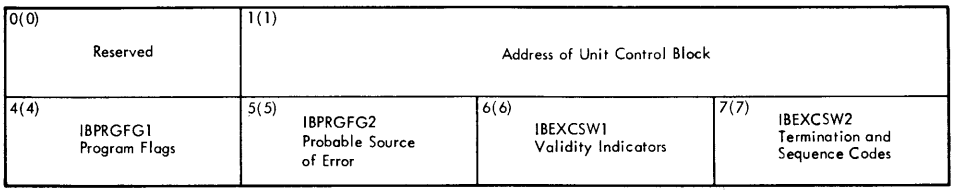


Figure 29. Error Recovery Procedure Interface Block

ERROR RECOVERY PROCEDURE INTERFACE BLOCK

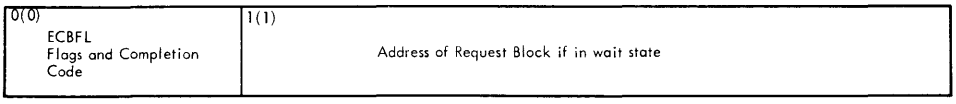
Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	xxxx xxxx	Reserved.
1(1)	. 3		Address of unit control block (UCB). The address of the UCB for the device in use when the channel failure occurred.
4(4)	1	IBPRGFG1	Program flags.
		1...	Channel status word (CSW) was stored after a Start I/O instruction was executed.
		.1..	CSW was stored after an I/O interruption.
		..1.	CSW was stored after a Test I/O instruction was executed.
		...1	CSW was stored after a Halt I/O instruction was executed.
		.... x...	Reserved.
		.... .1..	Sense data was stored.
		.... ..1.	Count in CSW is valid.
		1	No retry is to be tried under any conditions.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
5(5)	. 1	IBFRGFG2	Probable source of error.
		1...	CPU error.
		.1..	Channel error.
		..1.	Storage control unit error.
		...1	Storage error.
		.... 1...	Control unit error.
		xxx	Reserved.
6(6)	. . 1	IBEXCSW1	Validity indicators. Invalid fields may contain some useful information. However, they should not normally be used by I/O error routines.
		1...	Interface address is valid.
		.xx.	Reserved.
		...1	Sequence code is valid.
		.... 1...	Unit status is valid.
		.... .1..	Command address is valid. The CSW contains a valid command address.
		.... ..1.	Channel address is valid.
		1	Device address is valid. The device address in the I/O old PSW is valid. This bit should not be used by I/O error routines.
7(7)	. . . 1	IBEXCSW2	Termination and sequence (retry) codes.
		xx..	Termination code. Specifies the termination signals used on the I/O interface after the channel detected the error.
		00..	Interface disconnect.
		01..	Forced ending sequence (Stop). The channel responded to Service In with Command Out.
		10..	Selective reset.
		11..	System reset. A reset will not occur without a channel control check or an interface control check.
		..xx	Reserved.
		.... x...	I/O error alert.
		.... 1...	The indicated unit has signaled the I/O error on the I/O interface. The channel performs a selective reset and causes an interface control check to be set in the CSW.
		xxx	Sequence code. Indicates when the channel detected the error. Meaningful only for channel control checks or interface control checks. Not to be used by error routines involved with unit checks.
		.... .000	The error occurred during execution of a Test I/O instruction. A pending error interruption in the channel may have been cleared.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		.... .001	The channel has sent a Command Out signal but has not examined the unit status. May indicate unpredictable movement on devices with control units that start movement at the Command Out signal.
		.... .010	The device accepted the command but no data was transferred. Magnetic tape devices do not begin tape motion for a write operation until the first byte of data has been transferred.
		.... .011	At least one byte of data was transferred over the interface. The command address in the CSW is eight bytes higher than the address of the command causing the data transfer. In general this means device movement may have taken place if an Interface Disconnect signal was issued.
		.... .100	The command was not accepted by the control unit or a Command Out signal has not been sent to the control unit for the command at the address eight bytes higher than the address in the CSW. No device movement has taken place.
		.... .101	The command was accepted but data transfer may not have taken place. If the termination code is 'interface disconnect,' activity can be retried on most devices. It cannot be retried if the command was a Write command for a magnetic–tape device.
		.... .110	Reserved.
		.... .111	No other codes apply.

Event Control Block

The event control block (ECB, Figure 30) is used for communication between various components of the control program, as well as between processing programs and the control program.



The symbolic name of the first field in this control block may not agree with names used in other publications. For additional information, see the explanation at the beginning of the Data Area Layouts section.

Figure 30. Event Control Block (ECB)

EVENT CONTROL BLOCK

Offset	Bytes and Alignment	Field Name		Field Description, Contents, Meaning
0(0)	1	ECBFL		
		1...		Waiting for an event to occur.
		.1..		The event has occurred.
		.xxx xxxx	Hex.	Completion Code:
		.111 1111	7F	I/O activity completed without error.
		.100 0001	41	I/O activity not completed because a permanent error occurred.
		.100 0100	44	The request was intercepted because a permanent error occurred the last time the device was used.
		.100 1000	48	The request element has been freed because the data set has been found to be in permanent error.
		.100 1011	4B	One of the following critical errors occurred during tape error recovery processing: 1) The CSW command address in the IOB is zeros, erroneously 2) An unexpected Load Point was encountered
		.100 1111	4F	A direct-access device error recovery routine was unable to read the home address record or record 0.
1(1)	. 3			Before event completion, contains the address of the requestor's request block. After event completion, contains zeros.

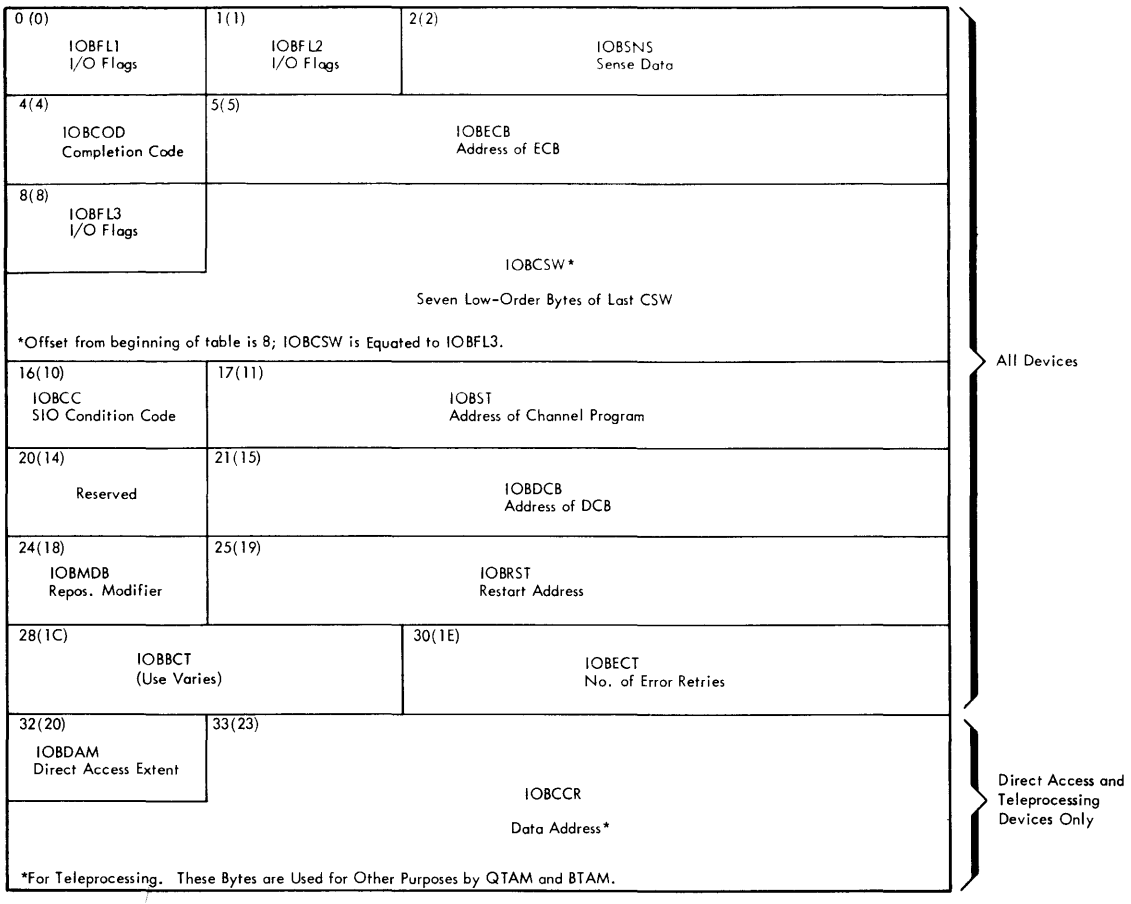
Input/Output Block

The input/output block (IOB, Figure 31) is the primary means of communication between a requestor of an I/O operation and the I/O supervisor. All of the information passed between the requestor and the I/O supervisor is either contained in the IOB, or is pointed to by the IOB.

Although the I/O supervisor uses IOBs, it neither creates them nor disposes of them; IOBs belong to the requestor of an I/O operation.

INPUT/OUTPUT BLOCK

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	IOBFL1	Flag byte 1.
		00..	No chaining.
		01..	Command chaining.
		10..	Data chaining.
		11..	Both command and data chaining.
		..1.	Error routine in control.
		...1	Device is to be repositioned (2400 series tape devices only).
			Modifier flag (1052).



The symbolic names of fields in this control block may not agree with names used in other publications.
For additional information, see the explanation at the beginning of the Data Area Layouts section.

Figure 31. Input/Output Block (IOB) Fields Used by the I/O Supervisor

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		.... 1...	Cyclic redundancy check needed—tape only.
		.... .1..	Exceptional condition. When an error routine returns and this bit is on, the error is considered permanent.
		.... ..1.	Not a related I/O request.
		0	Start.
		1	Restart.
1(1)	. 1	IOBFL2	Flag byte 2.
		x...	Not used.
		.1..	Sense will not be performed until device is free. At device end, device is free and sense command will be issued.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		..1.	IOB has been purged. Set by SVC or I/O purge routine.
		...1	Set by direct–access device error routines when no seek is required.
		.... 1...	Set by direct access error routines when alternate track is used.
		.... .1..	Set by direct access error routines when updating seek address because a cylinder end or file mask condition occurred.
		.... ..1.	Set by Device End Post trapcode module when channel end occurred without device end (graphics only).
		1	Set by QSAM routines when error recovery is to be used for 2540 card punch.
2 (2)	. . 2	IOBSNS	Sense data (device dependent).
4(4)	1	IOBCOD	Completion code for the I/O event (see ECB).
5(5)	. 3	IOBECB	Address of the ECB to be posted upon completion of the I/O event.
8(8)	1	IOBFL3	Device–dependent flags. See the descriptions of I/O error recovery routines for individual devices.
16(10)	1	IOBCC	Instruction length code (01 in bits 0 and 1) and condition code (bits 2 and 3) returned after execution of the start I/O instruction. Bits 4-7 are not used.
17(11)	. 3	IOBST	Address of the first CCW in the channel program to be executed.
20(14)	1		Reserved.
21(15)	. 3	IOBDCB	Address of the DCB needed for this request.
24(18)	1	IOBMDB	During error recovery, contains the command code for a needed immediate operation.
25(19)	. 3	IOBRST	Address of the first CCW in the channel program to be used for a restart.
			The four–byte field made up of IOBMDB and IOBRST combined may also have the following meanings:
			After SVC16 (PURGE) Quiesce, contains the address of the next IOB in the purge chain. For the last IOB in the chain, it contains ones.
			During I/O supervisor Write–to–Operator routine control, contains the track address of a defective track.
28(1C)	2	IOBBCI	QSAM, BSAM, EXCP access methods—Normal scheduling: The value used to increment the block count in the DCB for magnetic tape. Chained scheduling: Zeros.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
28(1C)	1		BTAM flags:
		1...	SAD or ENABLE given by Open routine resulted in a permanent I/O error.
		.1..	This IOB is being used.
		..xx xxx.	(Reserved bits).
		1	Line is under on–line test operation.
			DIRECT–ACCESS DEVICES
30(1E)	. 2	IOBECT	The number of times an I/O operation has been retried.
32(20)	1	IOBDAM	The number of the DEB extent block for the data set to be read or written. (The first extent block is number 0, the second number 1, etc.)
33(23)	. 7	IOBCCR	The beginning address of a data area on a direct–access device:

	Disk and Drum Storage Devices	IBM 2321 Data Cell Drive
Bytes 1–2	Zeros	Cell number
Bytes 3–4	Cylinder number	Subcell(3) and Strip(4) number
Bytes 5–6	Read/write head number	Cylinder number(5), and head number(6)
Byte 7	Record number	Record number

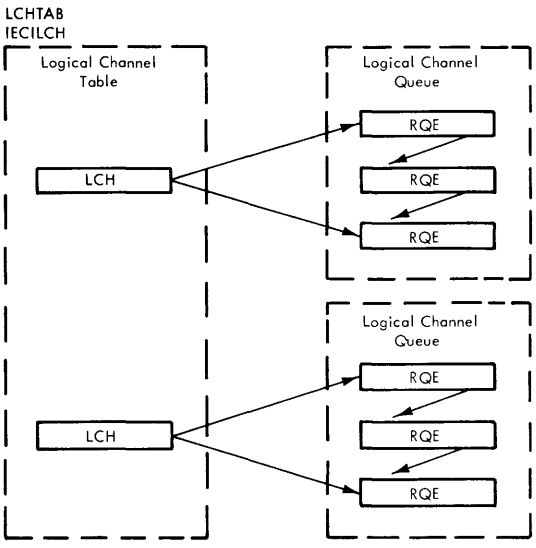


Figure 32. Logical Channel Queues

Logical Channel Word

The logical channel word (LCH) is an eight–byte data area which is used primarily to define the bounds of a logical channel queue (Figure 32). There is one logical channel word for each logical channel queue. All of the logical channel words together make up a table called the logical channel table. The format of a logical channel word is shown in Figure 33.

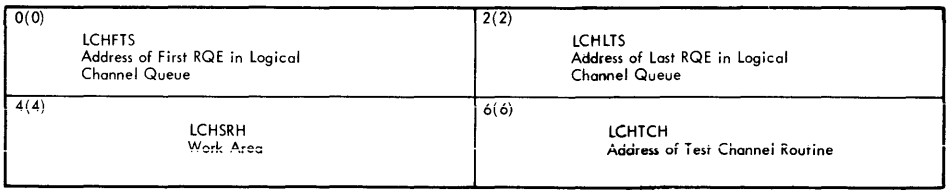


Figure 33. Logical Channel Word (LCH)

LOGICAL CHANNEL WORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	2	LCHFTS	Address of the first RQE in the logical channel represented by this logical channel word
2(2)	. 2	LCHLTS	Address of the last RQE in the logical channel represented by this logical channel word
4(4)	2	LCHSRH	Work area
6(6)	. 2	LCHTCH	Address of the Test Channel routine to be used for the channels in this logical channel

Program Status Word

The program status word (PSW, Figure 34) is a two–way communication link between a CPU and a program. All PSWs occupy permanently assigned main–storage locations. The PSWs to which the I/O supervisor refers are:

Name	Location	Symbolic Name
SVC Old PSW	32 (20)	SVCOPSW
I/O Old PSW	56 (38)	IOPSWO
I/O New PSW	120 (78)	IONPSW

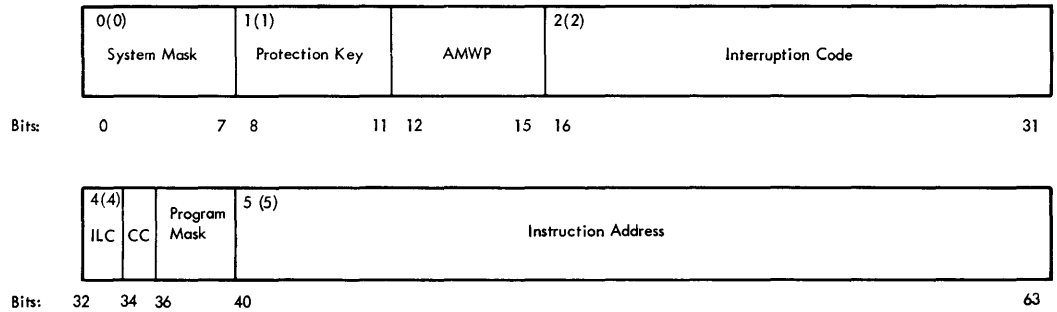


Figure 34. Program Status Word

PROGRAM STATUS WORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1		System mask. Each bit represents a potential interruption source. A system mask bit of 1 allows the corresponding source to cause an interruption. A mask bit of 0 prevents interruptions from occurring; they remain pending.
		1...	Channel 0.
		.1..	Channel 1.
		..1.	Channel 2.
		...1	Channel 3.
		.... 1...	Channel 4.
		.... .1..	Channel 5.
		.... ..1.	Channels 6 and up.
		1	External interruptions (timer, interruption key, and external signals of the direct control feature).
1(1)	4 bits	xxxx	Protection key. This key is matched with a storage key whenever data is stored in or fetched from a location that is protected.
1(1)	4 bits	 xxxx	AMWP bits. Four single–bit indicators:
		.... 1...	ASCII 8–character set.
		.... 0...	EBCDIC character set.
		.... .1..	Machine check interruptions can occur.
		.... .0..	Machine check interruptions will remain pending.
		.... ..1.	The CPU is in the wait state.
		.... ..0.	The CPU is in the running state.
		1	The CPU is in the problem state.
		0	The CPU is in the supervisor state.
2(2)	. 2		Interruption code. Identifies the cause or source of an interruption. For I/O interruptions, contains the address of the device that caused the interruption.
4(4)		xx..	Instruction length code (ILC). For program or or supervisor call interruptions, contains the length, in halfwords, of the last interpreted instruction. For I/O, external, and machine–check interruptions, the ILC is unpredicatable.
4(4)		..xx	Condition code (CC). Reflects the results of the execution of an instruction.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
4(4)		 xxxx	Program mask. Each bit represents a potential interruption source. A program mask bit of 1 allows the source to cause an interruption. A mask bit of 0 prevents the interruption from occuring.
		.... 1...	Fixed–point overflow.
		.... .1..	Decimal overflow.
		.... ..1.	Exponent underflow.
		1	Significance.
5(5)	. 3		Instruction address. The leftmost byte of the next instruction to be executed.

Recovery Management Support Communication Area

The recovery management support communication area (Figure 35) is used by the dynamic device reconfiguration routines. It contains the flags by which they monitor and control the change of volumes from one device to another, and it also contains the addresses of control blocks needed during the I/O operations they perform.

RECOVERY MANAGEMENT SUPPORT COMMUNICATION AREA

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	4	CCHPTTAB	Address of error recovery procedure interface block table.
4(4)	1		Flag indicating if there are any record entries to be written.
5(5)	. 3		Address of inboard record area.
8(8)	4		CCH base register value.
12(0)	4		Address of CCH channel dependent analysis routine pointer table.
16(10)	4		2880 channel logout pointer.
20(14)	1	DDRFLGSA	
		1...	SYSRES option specified.
		.x..	Reserved.
		..1.	Request being processed.
		...1	System–initiated requests permitted.
		.... 1...	Validate 'To' device.
		.... .1..	Nonstandard labels.
		.... ..1.	Nonstandard label verification routine is available.
		1	Operator–initiated request.

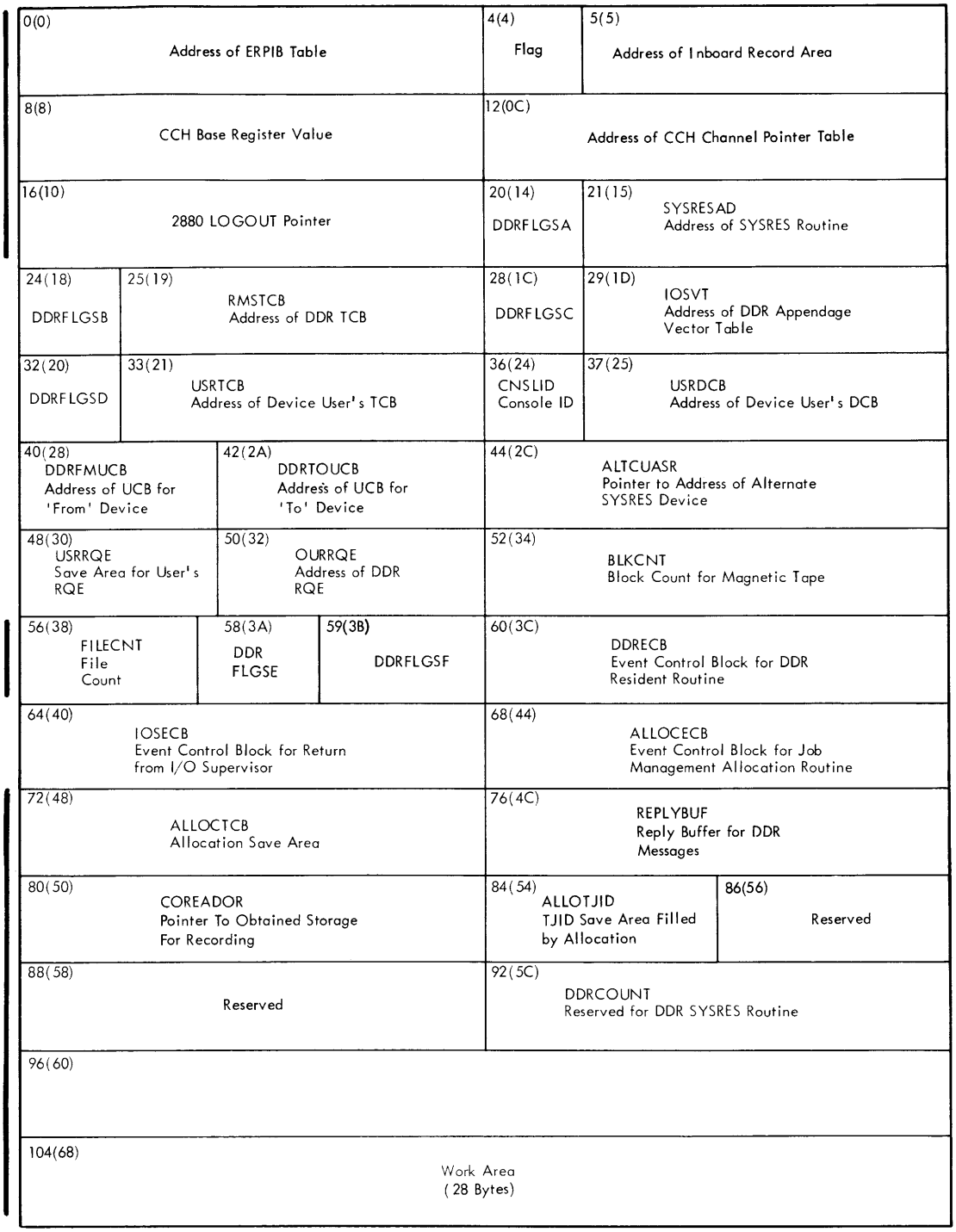


Figure 35. Recovery Management Support Communication Area

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
21(15)	. 3	SYSRESAD	Address of DDR SYSRES routine.
24(18)	1	DDRFLGSB	
		1...	Issue SWAP message.
		.1..	Issue INVALID message.
		..1.	Issue SYSRES WARNING message.
		...1	Issue DDR TERMINATED message.
		.... 1...	Issue PROCEED message.
		.... .1..	Shared direct access device.
		.... ..1.	'To' UCB not found.
		1	First I/O for control.
25(19)	. 3	RMSTCB	Address of DDR task control block.
28(1C)	1	DDRFLGSC	
		1...	Terminate DDR.
		.1..	STAE processing.
		..1.	Issue DDR CANCELED message.
		...1	Issue ERROR message.
		.... 1...	Swap UCB information.
		.... .1..	Reposition tape.
		.... ..1.	Re–EXCP without control.
		1	Issue ERP IN PROCESS message.
29(1D)	. 3	IOSVT	Address of IOS–DDR vector table.
32(20)	1	DDRFLGSD	
		1...	Branch to DDR SYSRES routine.
		.1..	Issue message IGF511A if this bit is off and the bit indicating branch to DDR SYSRES is on.
		..1.	Dump tape.
		...1	Read a record.
		.... 1...	Standard labeled tape.
		.... .1..	Unlabeled tape.
		.... ..1.	Forward space file.
		1	Re–EXCP with control.
33(21)	. 3	USRTCB	Address of device user's TCB.
36(24)	1	CNSLID	Save area for Console Identification.
37(25)	. 3	USRDCB	Address of Device User's DCB.
40(28)	2	DDRFMUCB	Address of UCB for 'From' device.
42(2A)	. . 2	DDRTOUCB	Address of UCB for 'To' device.
44(2C)	4	ALTCUASR	Pointer to address of alternate SYSRES device.
48(30)	2	USRRQE	Save area for user's RQE.
50(32)	. . 2	OURRQE	Address of DDR RQE.
52(34)	4	BLKCNT	Block count for magnetic tape.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
56(38)	2	FILECNT	File count for magnetic tape.
58(3A)	. . 1	DDRFLGSE	
		1...	Retry user.
		.1..	Issue WRONG VOLUME message.
		..1.	Tape label processing.
		...1	Read 3330 buffer.
		.... 1...	Error was encountered reading 'from' 3330 buffer.
		.... .1..	Error was encountered reading 'to' 3330 buffer.
		.... ..1.	Record 3330 buffer.
		1	'To' device buffer was read.
59(3B)	. . . 1	DDRFLGSF	
		1...	Issue COMPLETE message.
		.1..	Abnormal appendage.
		..1.	Re–initialize DDR block count.
		...1	Error in label processing.
		.... 1...	Initialize DDR processing.
		xxx	Reserved.
60(3C)	4	DDRECB	Event control block for DDR Resident routine.
64(40)	4	IOSECB	Event control block for return from I/O supervisor.
68(44)	4	ALLOCECB	Event control block for Job Management Allocation routine.
72(48)	4	ALLOCTCB	Allocation save area.
76(4C)	4	REPLYBUF	Reply buffer for DDR messages.
80(50)	4	COREADDR	Pointer to obtained storage for recording.
84(54)	2	ALLOTJID	TJID save area filled by allocation.
86(56)	. . 2	Reserved.	
88(58)	4	Reserved.	
92(5C)	4	DDRCOUNT	Reserved for DDR SYSRES routine.
104(68)	28		Work area.

Request Queue Element

The request queue element (RQE, Figure 36) contains the addresses of the major control blocks that are needed to process a request for I/O activity.

During system generation, a number of RQEs are created to equal the maximum number of I/O new operations that can be processed simultaneoulsy by the new operating system. Except for the last, each of these unassigned RQEs contains only the address of the next RQE; the last RQE contains 1s in its address, or link, field. The chain of unassigned RQEs is called a freelist.

When a request for I/O activity is received by the I/O supervisor, it removes one RQE from the freelist, and initializes that RQE with the addresses of control blocks needed to process the request. This is done for every request, regardless of whether or not the I/O activity can be started immediately.

When a request cannot be started immediately, the RQE is placed into a logical channel queue, where it remains until the needed device and a path to the device become available and, optionally, until higher–priority requests for the same device and path are satisfied.

During the I/O activity, the address of the RQE is in the UCBLTS field of the UCB.

An RQE is returned to the freelist when all I/O activity associated with the request it represents is completed.

All of the RQEs are located contiguously in main storage, and are sometimes referred to as the request queue element table. The term 'table' is used loosely, however, because access is gained to the specific RQEs via pointers, and not via offsets from the beginning of the 'table'.

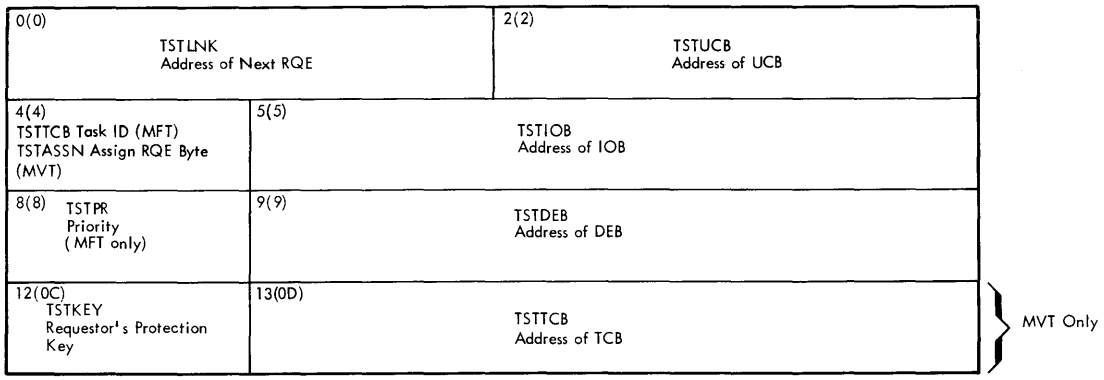


Figure 36. Request Queue Element

REQUEST QUEUE ELEMENT

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	2	TSTLNK	The address of the next RQE in the logical channel queue or the next RQE in the freelist. Contains 1s when this is the last RQE in the queue or freelist.
2(2)	. 2	TSTUCB	The address of the unit control block representing the device for which activity is desired.
4(4)	1	TSTCB	MFT: A unique TCB identifier, taken from the requestor's TCB, or ones, if the RQE is available.
		TSTASSN	MVT: Contains ones when the RQE is available, zeros when the RQE is assigned.
5(5)	. 3	TSTIOB	The address of the input/output block (IOB) to be used for this request.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
8(8)	1	TSTPR	MFT: The requestor's priority. MVT: Reserved.
9(9)	. 3	TSTDEB	The address of the data extent block (DEB) to be used for this request.
12(0C)	1	TSTKEY	MVT only: The requestor's protection key or zeros in systems without the protection feature.
13(0D)	. 3	TSTTCB	MVT only: The address of the requestor's task control block (TCB).

SYS1.LOGREC Data Set

Every time there is an equipment malfunction, data pertaining to the failure is collected and stored in the SYS1.LOGREC data set. The data can then be retrieved for analysis by use of a utility program (the IFCEREPO Utility routine, described in the publication *OS Service Aids,* GC28–6719).

The SYS1.LOGREC data set is contained on the system residence device and is initialized during system generation. It contains the following:

- One header record
- One record entry for every malfunction for which the system has a system environment recording facility

The header record (Figure 37) is used to find existing record entries and to find where new record entries are to be written.

Record entries contain information pertaining to the environment that existed at the time an error occurred. There are several types of record entries. Outboard records (Figures 38 and 39) describe I/O device failures; Inboard records (Figure 41) describe channel failures; miscellaneous data records (Figure 40) describe the error environment for buffered log devices and for IBM 2715; and CPU records describe CPU malfunctions (see the publication *OS M65 Machine–Check Handler Logic,* GY27–7155). Record entries are not written in any special grouping or order on the SYS1.LOGREC data set. A new record entry always follows the last entry written.

SYS1.LOGREC DATA SET HEADER RECORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	2	CLASRC	Header record identifier. Should contain all 1s. Otherwise, critical data has been destroyed.
2(2)	. . 4	LOWLIMIT	Address of low extent. The track address of the first extent of SYS1.LOGREC in the form CCHH.
6(6)	. . 4	UPLIMIT	Address of high extent. The track address of the last extent of SYS1.LOGREC in the form CCHH.

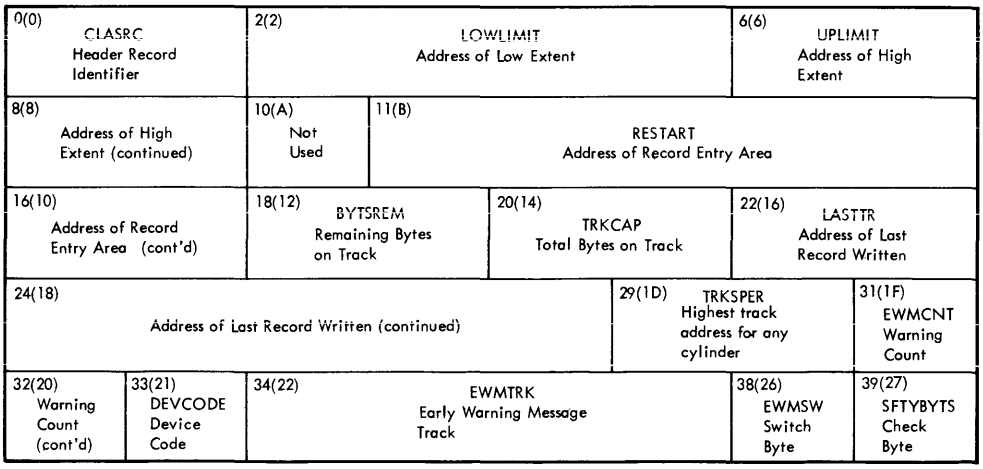


Figure 37. SYS1.LOGREC Data Set Header Record

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
10(A)	. . 1		Not used.
11(B)	. . 7	RESTART	Address of record entry area. The track address of the start of the recording area of SYS1.LOGREC in the form BBCCHHR.
18(12)	. . 2	BYTSREM	Remaining bytes on track. The number of bytes remaining on the track upon which the last record entry was written.
20(14)	2	TRKCAP	Total bytes on track. The number of bytes which can be written on a track of the device containing the SYS1.LOGREC data set.
22(16)	. . 7	LASTTR	Address of the last record written. The track address of the last record written on the SYS1.LOGREC recording area in the form BBCCHHR.
29(1D)	. 2	TRKSPER	Highest track address for any cylinder.
31(1F)	. . 2	EWMCNT	Warning count. The number of bytes remaining on the early warning message track of SYS1.LOGREC when the 90% full point is reached.
33(21)	. 1	DEVCODE	Device Code. A code denoting the type of device on which the SYS1.LOGREC data set is resident.

Code	Device	Code	Device
01	2311	06	2305–I
02	2301	07	2305–II
03	2303	08	2314
04	2302	09	3330

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
34(22)	. . 4	EWMTRK	Early warning message track. The track address, in the form CCHH, on which the 90% full point exists.
38(26)	. . 1	EWMSW 1... .... .xxx xxxx	Switch byte. The 90% full point message has been issued. Unassigned.
39(27)	. . 1	SFTYBYTS	Check byte. Contains all 1s. It is used to check the header record to ensure that it also contains all 1s.

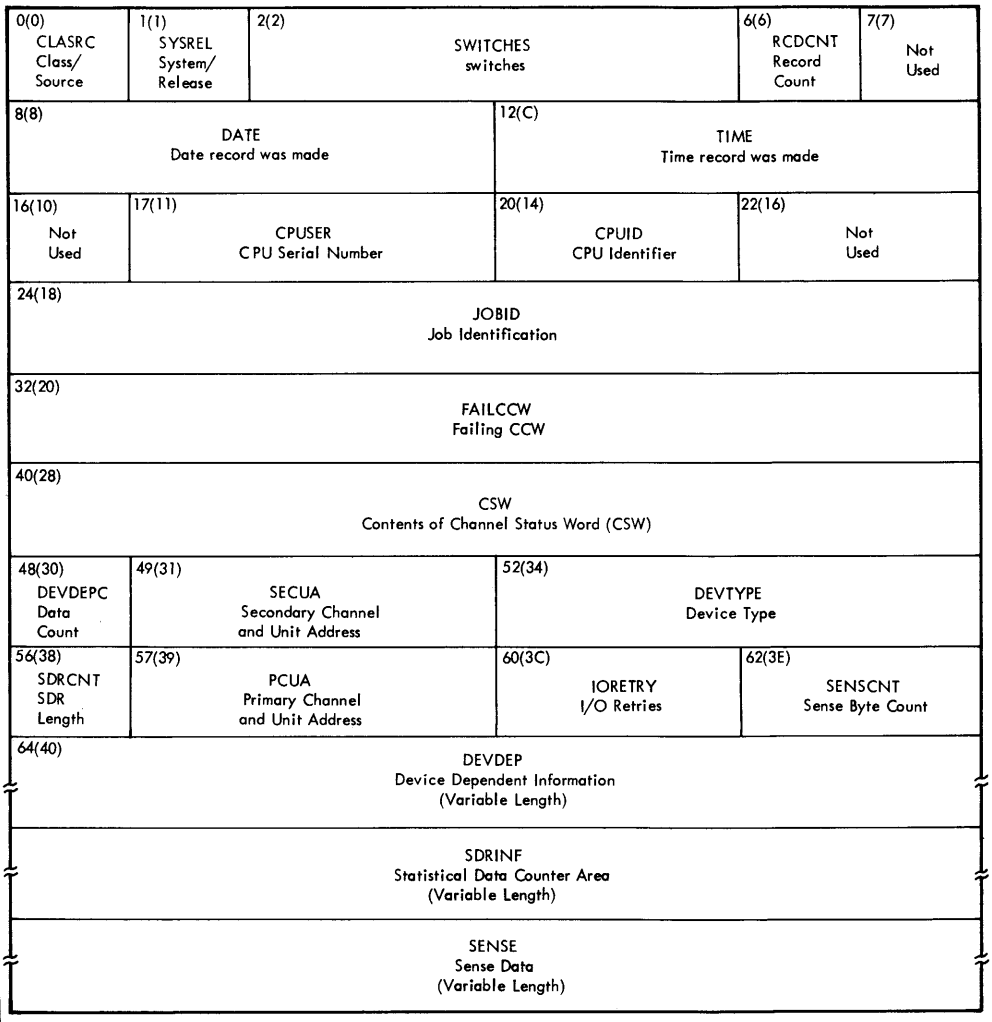


Figure 38. SYS1.LOGREC Data Set Outboard Record (Long)

SYS1.LOGREC DATA SET OUTBOARD RECORD (LONG)

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CLASRC	Class/source.
		..11 xxxx	Unit Check record.
		xxxx	OBR.
		xxxx ..1.	Converted OBR.
		xxxx .1..	TP access method (TCAM).
1(1)	. 1	SYSREL	System/release.
		...x xxxx	OS
		..1x xxxx	DOS
		bits 3–7	
		0–1F	Release level 0–31.
2(2)	. . 4	SWITCHES	Switches.
		Byte 0:	
		1...	More records follow.
		0...	Last record.
		.1..	Time–of–day clock.
		..1.	Reserved for future use.
		.... 1...	Time macro used (HHMMSS)
		...x .xxx	Unassigned.
		Byte 1	
		1...	SDR dump (EOD).
		.1..	Temporary error.
		..1.	Short record.
		...1	MP system.
		.... 1...	CPU B (MB system).
		.... .1..	Volume dismount.
		.... ..x.	Reserved.
		x	Not used.
		Bytes 2–3	Not used.
6(6)	. . 1	RCDCNT	Record count. Bits 0–3 contain the sequence number of a physical record. Bits 4–7 contain the total number of physical records in this logical record.
7(7)	. . . 1		Not used.
8(8)	4	DATE	Date record was made. System date when failure occurred.
12(C)	4	TIME	Time record was made. System time when failure occurred.
16(10)	1		Not used.
17(11)	. 3	CPUSER	CPU serial number (System/370 only).
20(14)	2	CPUID	CPU identifier.
22(16)	. . 2		Not used.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
24(18)	8	JOBID	Job identification. Name assigned to the job being executed at the time of the failure.
32(2)	8	FAILCCW	Failing CCW. The CCW which was being executed at the time of the failure.
40(28)	8	CSW	Contents of channel status word (CSW). The contents of the CSW which was stored following the detection of the I/O failure.
48(30)	1	DEVDEPC	Data count. The count of doublewords that are used in the record for device dependent data.
49(31)	. 3	SECUA	Secondary channel and unit address. The address of the I/O device associated with the final retry.
52(34)	4	DEVTYPE	Device type. The device associated with the failure.
56(38)	1	SDRCNT	SDR length. The number of bytes in this record used to contain the statistical data counter information.
57(39)	. 3	PCUA	Primary channel and unit address. The addresses of the channel and unit being used when the failure occurred. If the unit is a model 2314 or 3330, this field contains physical addresses.
60(3C)	. . 2	IORETRY	I/O retries. The number of I/O retries attempted for this failure.
62(3E)	. . . 2	SENSCNT	Sense byte count. The length of the sense byte field.
64(40)	variable	DEVDEP	Device–dependent information. Data of a device–dependent nature.
	variable	SDRINF	Statistical data counter area. The area which contains statistical counter data.
	variable	SENSE	Sense data. The sense information that was obtained as a result of the failure.

SYS1.LOGREC DATA SET OUTBOARD RECORD (SHORT)

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CLASRC	Class/source.
		..11 xxxx	Unit check record.
		xxxx	OBR.
		xxxx ..1.	Converted OBR.
		xxxx .1..	TP access method (TCAM).

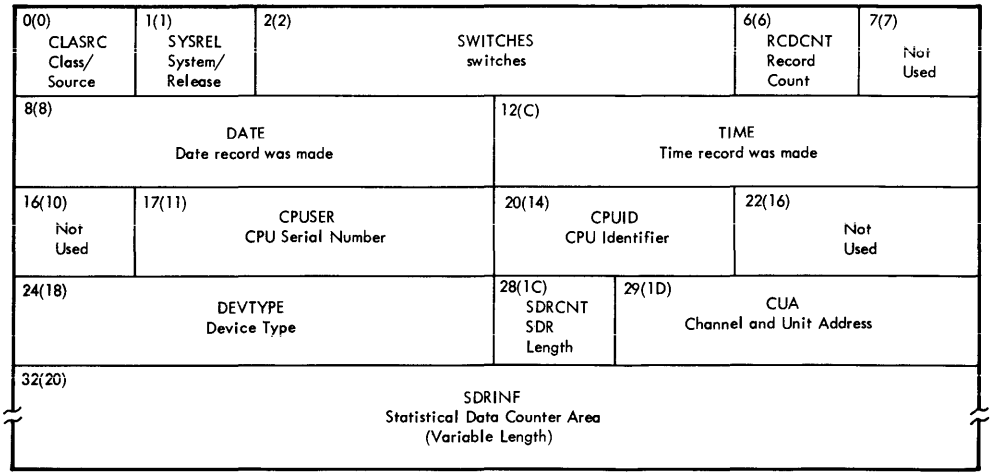


Figure 39. SYS1.LOGREC Data Set Outboard Record (Short)

SYS1.LOGREC DATA SET OUTBOARD RECORD (SHORT)

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
1(1)	. 1	SYSREL	System/release.
		...x xxxx	OS.
		..1x xxxx	DOS.
		bits 3–7	
		0–1F	Release level 0–31
2(2)	. . 4	SWITCHES	Switches.
		Byte 0:	
		1...	More records follow.
		0...	Last record.
		.1..	Time–of–day clock.
		..1.	Reserved for future use.
		.... 1...	Time macro used (HHMMSS)
		...x .xxx	Unassigned.
		Byte 1:	
		1...	SDR dump (EOD).
		.1..	Temporary error.
		..1.	Short record.
		...1	MP system.
		.... 1...	CPU B (MP system).
		.... .1..	Volume dismount.
		.... ..x.	Reserved.
		x	Not used.
		Bytes 2–3	Not used.
6(6)	. . 1	RCDCNT	Record count. Bits 0–3 contain the sequence number of a physical record. Bits 4–7 contain the total number of physical records in this logical record.
7(7)	. . . 1		Not used.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
8(8)	4	DATE	Date record was made. System date when failure occurred.
12(C)	4	TIME	Time record was made. System time when failure occurred.
16(10)	1		Not used.
17(11)	. 3	CPUSER	CPU serial number (System/370 only).
20(14)	. 2	CPUID	CPU Identifier.
22(16)	. . 2		Not used.
24(18)	4	DEVTYPE	Device type. The device associated with the failure.
28(1C)	1	SDRCNT	SDR length. The number of bytes in this record used to contain the statistical data counter information.
29(1D)	. 3	CUA	Channel and unit address. The addresses of the channel and unit being used when the failure occurred.
32(20)	variable	SDRINF	Statistical data counter area. The area which contains statistical counter data.

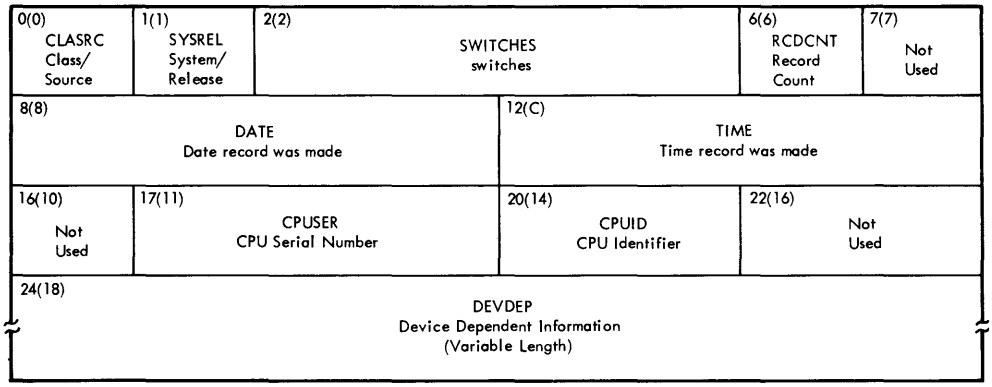


Figure 40. SYS1.LOGREC Data Set Miscellaneous Data Record

SYS1.LOGREC DATA SET MISCELLANEOUS DATA RECORD

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CLASRC	Class/source.
		1..1	Summary record from SVC 91 and DDR recorder.
		1..1 ...1	Miscellaneous data record.
		11	Converted TPER record.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
1(1)	. 1	SYSREL	System/release.
		...x xxxx	OS
		..1x xxxx	DOS
		bits 3–7	
		0–1F	Release level 0–31.
2(2)	. . 4	SWITCHES	Switches
		Byte 0:	
		1...	More records follow.
		0...	Last record.
		.1..	Time–of–day clock.
		..1.	(Reserved)
		.... 1...	Time macro used (HHMMSS)
		...x .xxx	Not used.
		Byte 1	Not used.
		Byte 2:	
		1	Model 3330.
		.... ..1.	Model 2305–2.
		.... .1..	Model 3211.
		.... 1...	Model 2715.
		...1 ..1.	Model 2305–1.
		Byte 3	Not used.
6(6)	. . 1	RCDCNT	Record count. Bits 0–3 contain the sequence number of a physical record. Bits 4–7 contain the total number of physical records in this logical record.
7(7)	. . . 1		Not used.
8(8)	4	Date	Date record was made. System date when incident occurred.
12(C)	4	TIME	Time record was made. System time when incident occurred.
16(10)	1		Not used.
17(11)	. 3	CPUSER	CPU serial number (System/370 only).
20(14)	2	CPUID	CPU Identifier (System/370 only).
22(16)	. . 2		Not used.
24(18)	variable	DEVDEP	Device–dependent information. The device–dependent data supplied by the error recovery procedure for recording.

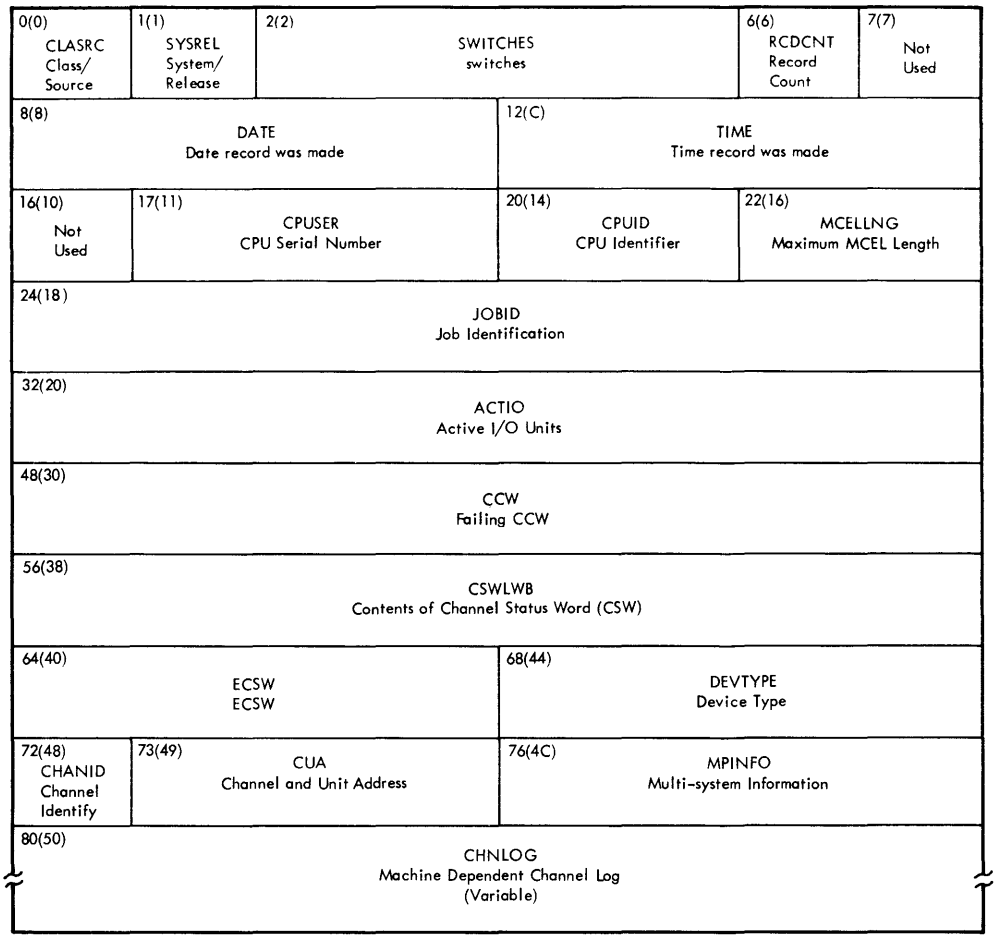


Figure 41. SYS.LOGREC Data Set Inboard (Channel–Check) Record

SYS1.LOGREC DATA SET INBOARD (CHANNEL–CHECK) RECORD

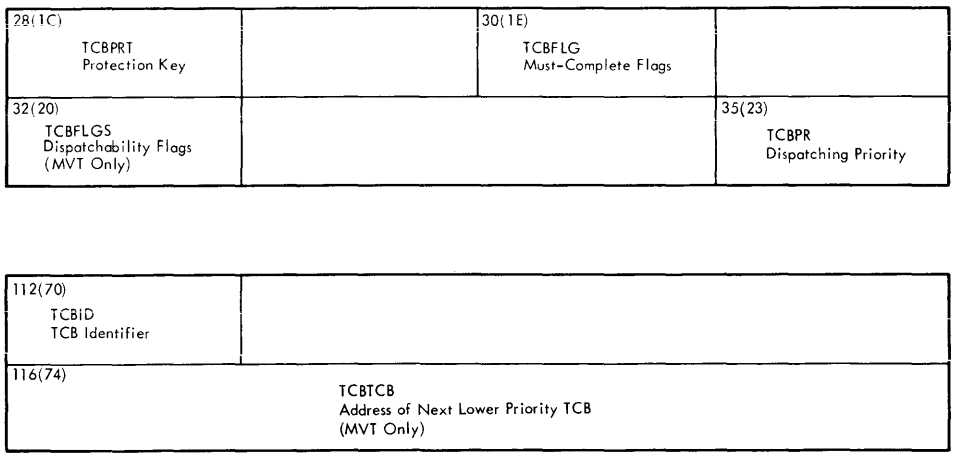
Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	CLASRC	Class/source.
		..1. xxxx	Channel–check record.
		xxxx 1...	SER1.
		xxxx 1..1	SER0.
1(1)	. 1	SYSREL	System/release.
		...x xxxx	OS.
		..1x xxxx	DOS.
		bits 3-7	
		0–1F	Release level 0–31.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
2(2)	. . 4	SWITCHES	Switches.
		Byte 0:	
		1...	More records follow.
		0...	Last record.
		.1..	Time–of–day clock.
		..1.	(Reserved).
		.... 1...	Time macro used (HHMMSS).
		...x .xxx	Not used.
		Byte 1:	
		1...	Operator message required.
		.1..	Record incomplete.
		..1.	System terminated.
		...1	Channel unsupported or failed to log.
		.... 1...	Illegal channel and unit address.
		.... .1..	Portion of data overlayed.
		.... ..1.	ERP in progress.
		x	Not used.
		Bytes 2–3	Not used.
6(6)	. . 1	RCDCNT	Record count. Bits 0–3 contain the sequence number of a physical record. Bits 4–7 contain the total number of physical records in this logical record.
7(7)	. . . 1		Not used.
8(8)	4	DATE	Date record was made. System date when incident occurred.
12(C)	4	TIME	Time record was made. System time when incident occurred.
16(10)	1		Not used.
17(11)	. 3	CPUSER	CPU serial number (System/370 only).
20(14)	2	CPUID	CPU identifier.
22(16)	. . 2	MCELLNG	Maximum MCEL length. Maximum machine check extended log length.
24(18)	8	JOBID	Job identification. Name assigned to the job being executed at the time of the failure.
32(20)	16	ACTIO	Active I/O units. A list of addresses of up to eight devices on the failing channel that were found to be busy (Device End outstanding). The list may include the address of the device associated with the failure.
48(30)	8	CCW	Failing CCW. The CCW that was being executed at the time of the failure.

56(38)	8	CSWLWB	Contents of channel status word (CSW). The contents of the CSW which was stored following the detection of the I/O failure.
64(40)	4	ECSW	ECSW. The contents of the extended channel status word.
68(44)	4	DEVTYPE	Device type. The type of device associated with the failure.
72(48)	1	CHANID	Channel identity. The type of channel associated with the failure.
73(49)	. 3	CUA	Channel and unit address. The channel and unit address of the I/O device associated with the failure.
76(4C)	4	MPINFO Byte 0: xxx. ....1 .... x... .... .x.. .... ..xx Byte 1 Bytes 2-3	Multisystem information. Not used. Multisystem feature present. Identity of failing CPU (0=1, 1=2). Not used. CPU status: 00 = normal multisystem (shared status) 01 = partitioned mode 10 = 65 mode (shared but reconfigured) Not used. Byte 2—CPU 1 Byte 3—CPU 2 In each byte there is one bit for each of the 7 possible channels showing online/offline status (offline = 1). If not in multisystem mode, bytes 2 and 3 will contain all zeros.
80(50)	variable	CHNLOG	Machine–dependent channel log. The channel logout associated with the failure which caused the channel check. Logout size is model and channel dependent.

Task Control Block

The task control block (Figure 42) serves as a repositiory for information and pointers associated with the task in progress.



The symbolic names of fields in this control block may not agree with names used in other publications. For additional information, see the explanation at the beginning of the Data Area Layouts section.

Figure 42. Task Control Block Fields Used by the I/O Supervisor

TASK CONTROL BLOCK

Offset	Bytes and Field Alignment	Name	Field Description, Contents, Meaning
28(1C)	1	TCBPRT	
		xxxx 0000	The storage protection key for the task presented by this TCB.
30(1E)	. . 1	TCBFLG	MFT:
		1...	ABEND prohibited for this task (System tasks only.)
		.xx. ..x.	(Reserved bits.)
		...1	Task has issued a system–must–complete and set all other tasks in the system non-dispatchable.
		.... 1...	Task has issued a step–must–complete and turned off all other tasks in the step.
		.... .1..	Dump processing has been initiated in ABEND.
		1	This task is a member of a time–slice group (MFT only).
		TCBFLG	MVT:
		1...	Operands of the ABEND macro instruction have been saved in the TCBCMP field.
		.1..	Second job step interval has expired (initiator TCB only).
		..1.	Job step can cause rollout (job step TCB only).
		...1	System must complete. Current task can be performed; other tasks in system cannot.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		.... 1...	Step must complete; other tasks in job step cannot be performed.
		.... .1..	SYSABEND data set already open (job step TCB only).
		.... ..1.	ETXR exit requested by attaching task.
		1	Task is a member of a time–slice group.
32(20)	1	TCBFLGS	(If any bit in this byte is 1, the task is nondispatchable.)
		1...	Set by ABDUMP routine.
		.1..	Machine check occurred. All tasks except current task placed in wait state.
		..1.	Supply of I/O request queue elements exhausted.
		...x xx..	(Reserved bits.)
		.... ..1.	Task set nondispatchable by one CPU to prevent any CPU from performing it (Model 65 multi–processing only).
		1	ABEND routine was entered by this task while DCB for SYSABEND data set was being opened for another task.
35(23)	. . . 1	TCBPR	Dispatching priority for this task.
112(70)	1	TCBID	MFT: TCB identifier field. MVT: Number of resources for which this task is enqueued.
116(74)	4	TCBTCB	Address of next TCB of lower priority on the ready queue.

UCB Lookup Table

The unit control block (UCB) lookup table provides a means for the I/O interruption supervisor to quickly find the UCB for a device which has caused an I/O interruption. By using the channel and device addresses provided in the I/O old PSW, and by referring to the UCB lookup table, the I/O interruption supervisor can obtain the address of the needed UCB without checking all UCBs.

The entire UCB lookup table (Figure 43) is created during system generation. At that time all entries are calculated on the basis of system channel and device address assignments.

Although the UCB lookup table occupies contiguous main storage locations, it consists of three separate sections: a channel index list, a control unit index list, and a device address list. Each serves as an index to the next, with the device list containing pointers to UCBs (Figure 44).

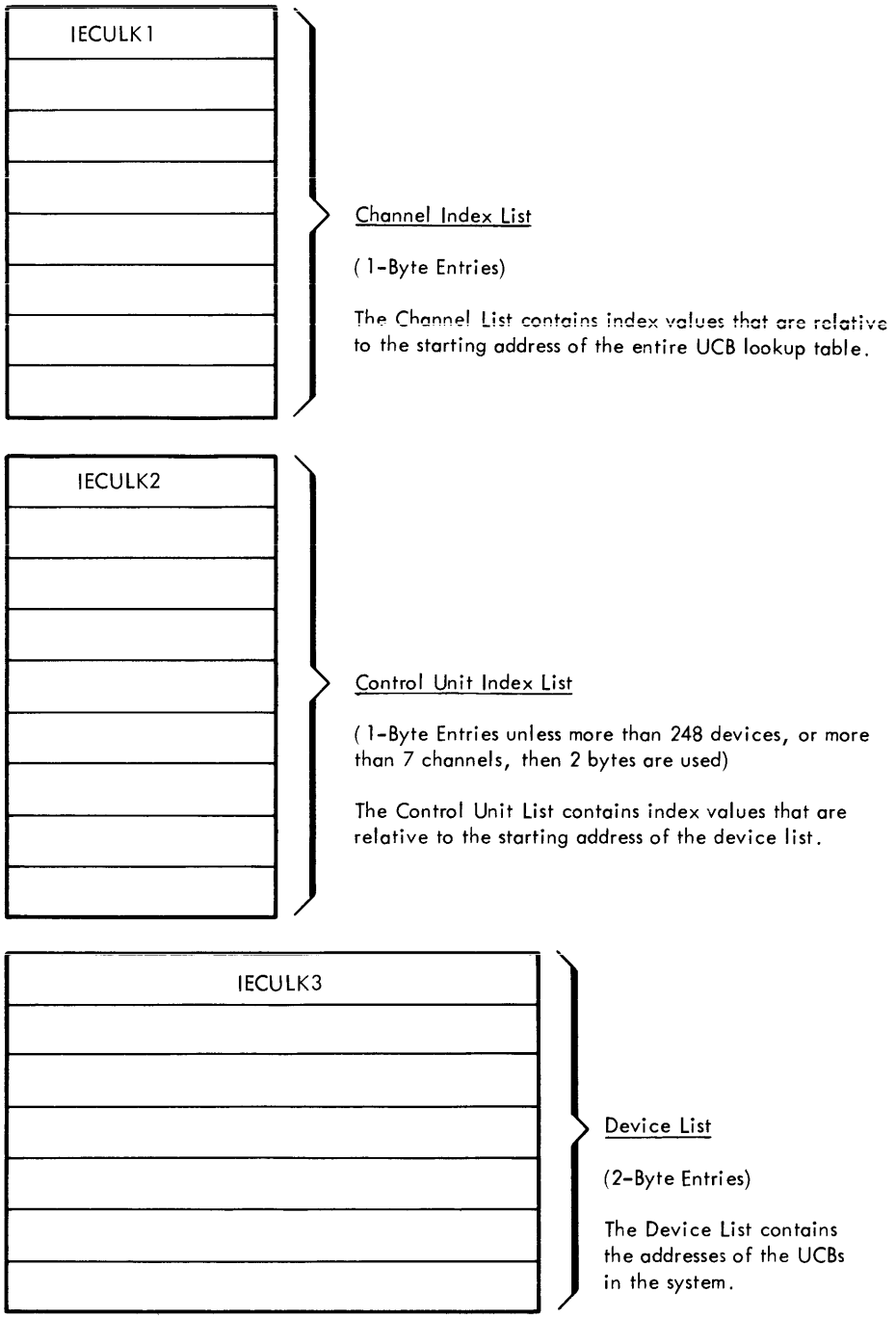
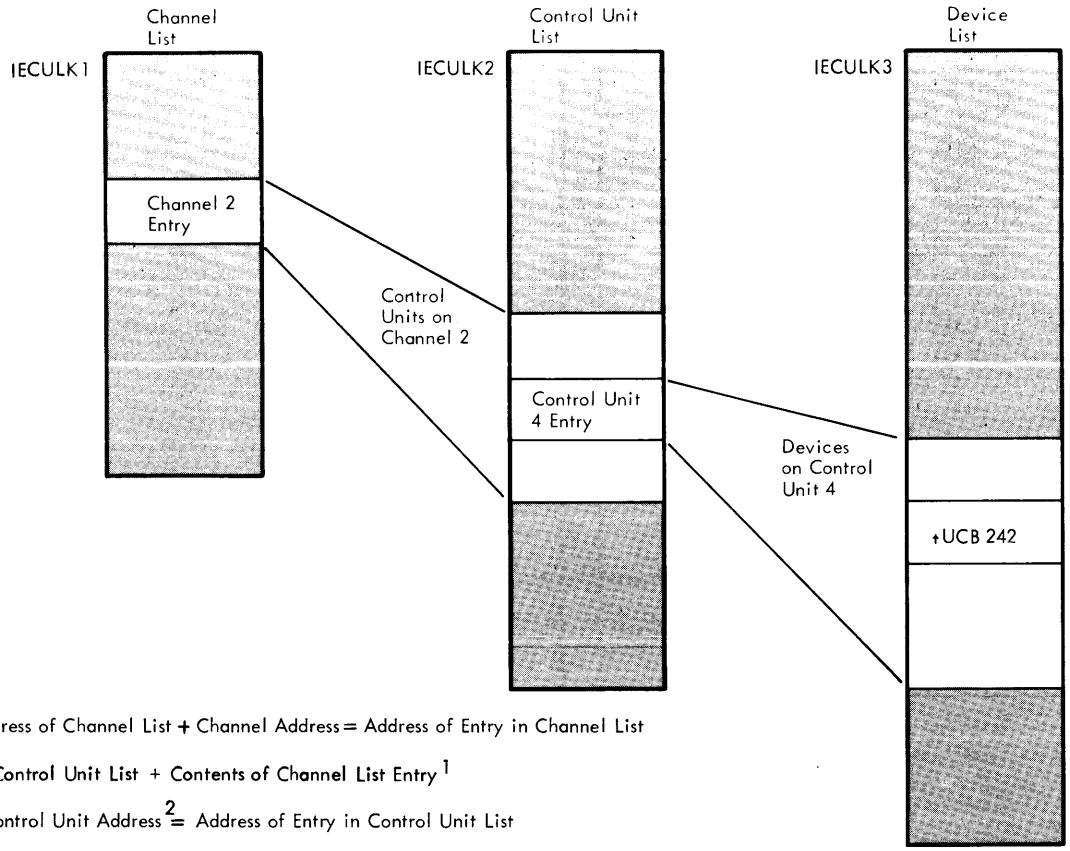


Figure 43. UCB Lookup Table



Beginning Address of Channel List + Channel Address = Address of Entry in Channel List

Beginning of Control Unit List + Contents of Channel List Entry [1]

+Control Unit Address [2] = Address of Entry in Control Unit List

Beginning Address of Device List + 2 (Contents of Control Unit List Entry)

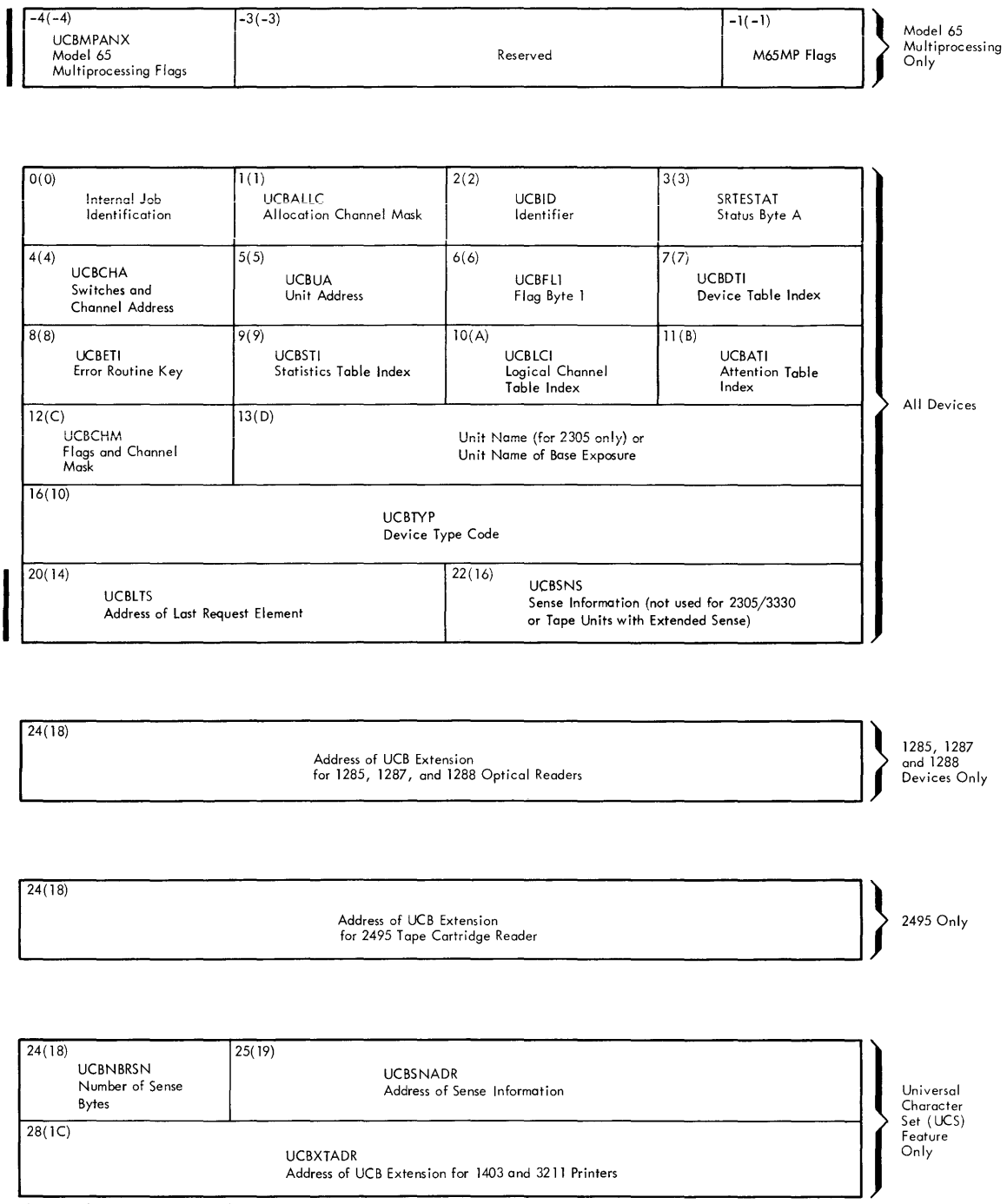
+ 2 (Device Number) = Address of Entry in Device List

1. If the channel number is 7 or greater, the contents of the channel list entry is doubled.
2. If the control unit entry list contains 2-byte entries, the control unit address is multiplied by 2 before it is used.

Figure 44. UCB Lookup Table Entry Relationships

Unit Control Block

There is a unit control block (UCB, Figure 45) for each device attached to the system. It describes the characteristics of the device to the I/O supervisor and is used by the job scheduler during allocation of the device.



The Symbolic names of fields in this control block may not agree with names used in other publications.
For additional information, see the explanation at the beginning of the Data Area Layouts section.

Figure 45 (Part 1 of 5). Unit Control Block

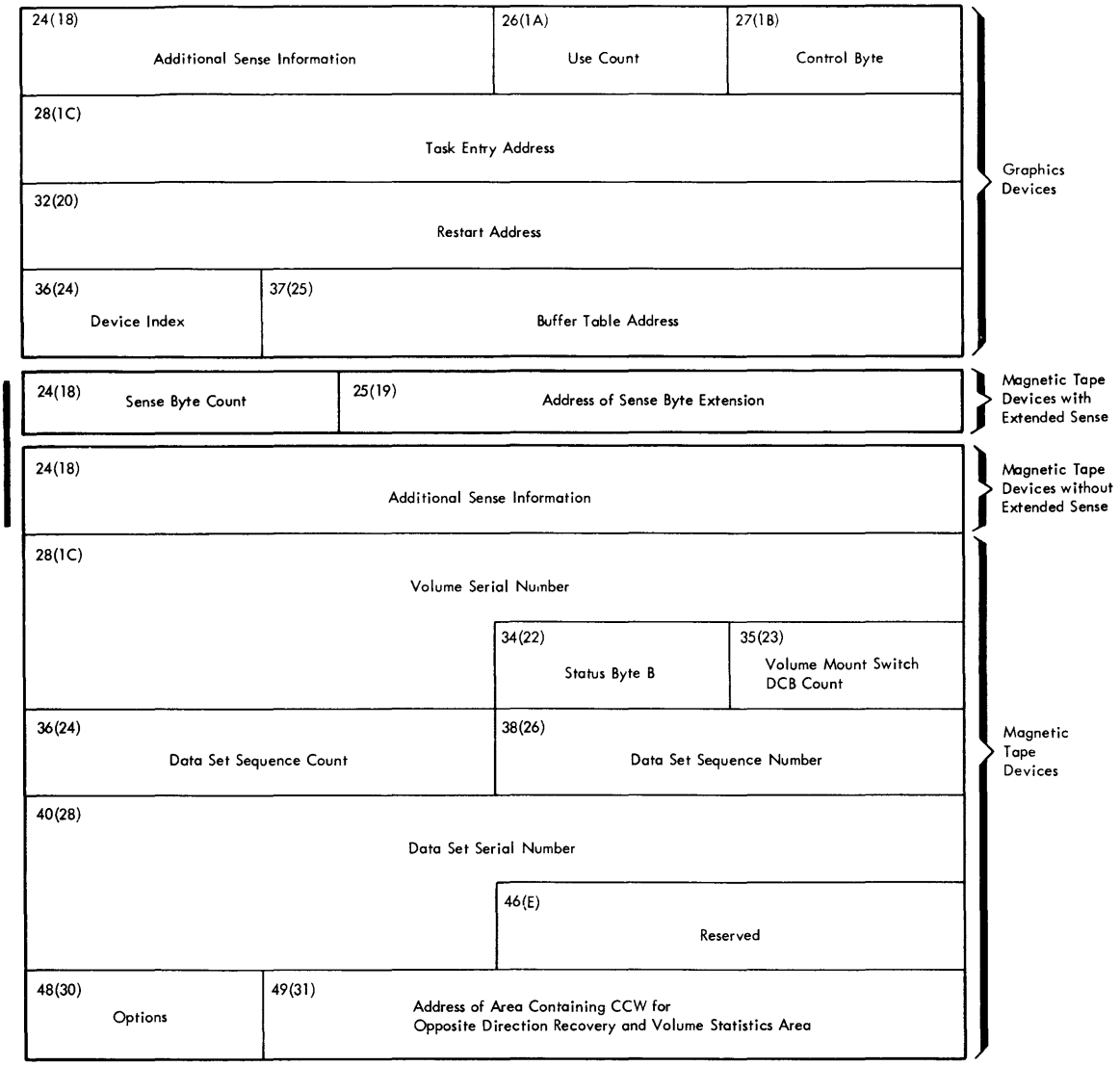
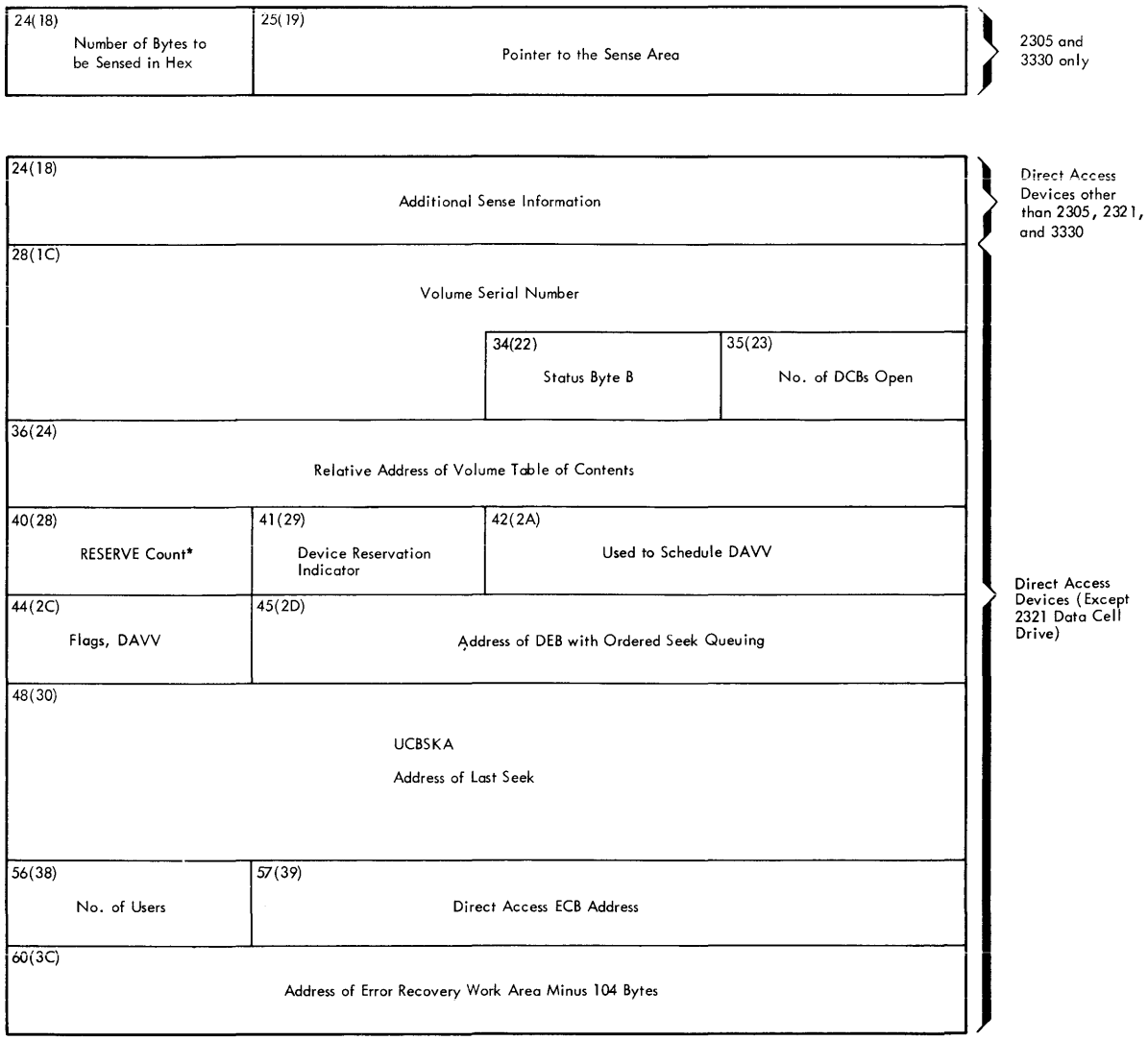


Figure 45 (Part 2 of 5). Unit Control Block



*Used by the Shared DASD Option.

Figure 45 (Part 3 of 5). Unit Control Block

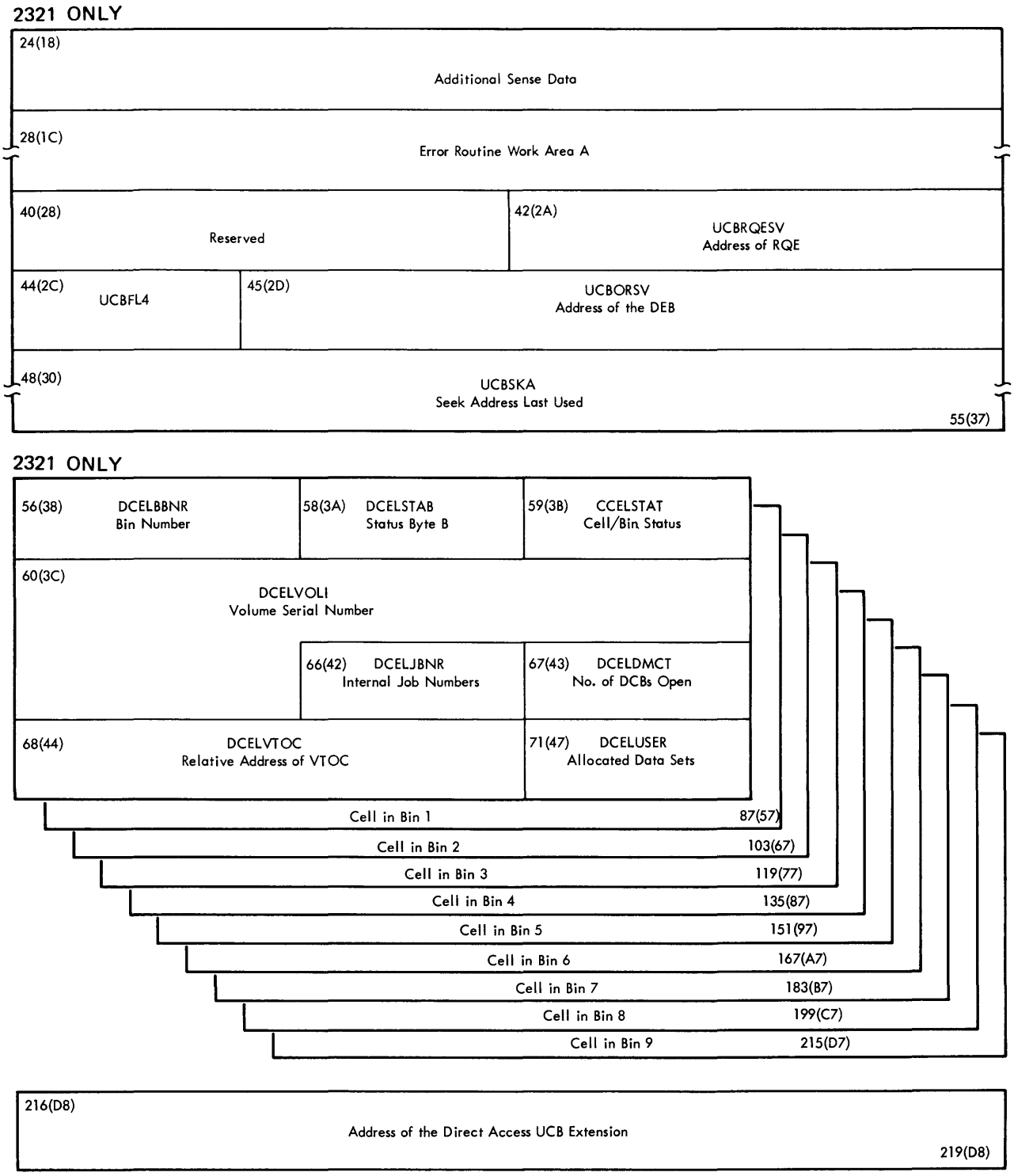
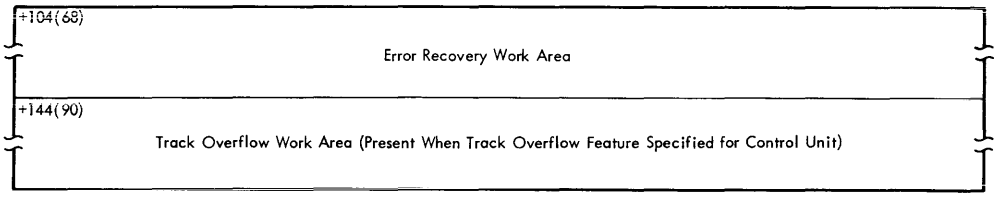
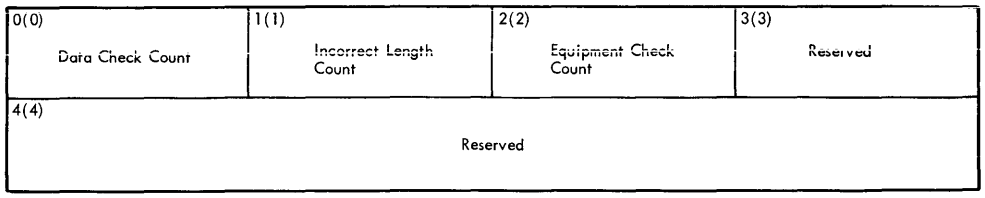


Figure 45 (Part 4 of 5). Unit Control Block

Direct Access UCB Extension:



1285, 1287, 1288 Optical Reader UCB Extension:



2495 Tape Cartridge Reader UCB Extension:

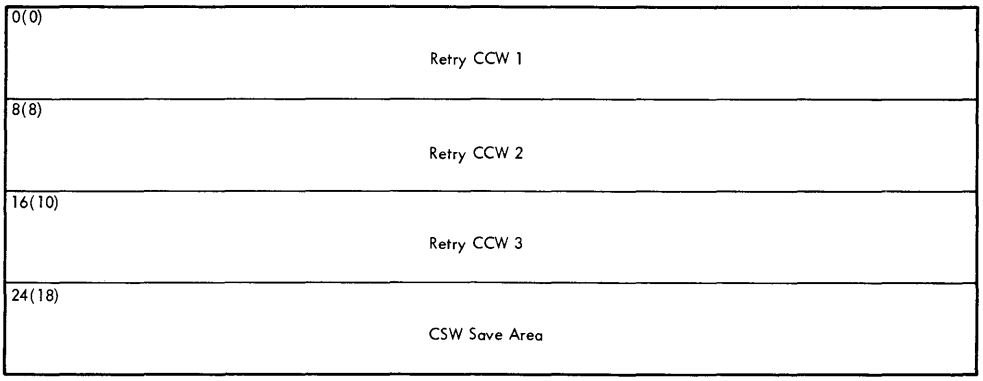


Figure 45 (Part 5 of 5). Unit Control Block

UNIT CONTROL BLOCK

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
			Prefix Segment
-4(-4)	1	UCBMPANX	Model 65 multiprocessing flags.
		.x.. .x..	(Reserved bits.)
		1...	Device can be reached via an alternate control unit.
		...1	CPU A is to use an HIO instruction for this device.
		..1.	CPU B is to use an HIO instruction for this device.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
		.... 0...	CPU A last used an SIO instruction for this device.
		.... 1...	CPU B last used an SIO instruction for this device.
		.... ..0.	CPU B has a path to this device.
		.... ..1.	CPU B has no path to this device.
		0	CPU A has a path to this device.
		1	CPU A has no path to this device.
-3(-3)	. 2	Bytes 2-3	(Reserved)
-1(-1)	. . . 1		M65MP flags.
		..11 .1..	Three one–bit switches used by extended Vary command, (always 0 on exit).
		..1.	Device was reserved by NIP (IPLed CPU)., Always zero on exit from NIP.
		...1	Device was reserved by IEAMP650 (non–IPLed CPU). Always zero on exit from NIP.
		.... .1..	Operator replied 'CONTINUE' to message IEA120A for device. Always zero on exit from NIP.
		.... ..1.	One–bit switch used by processing modules, (always 0 on exit).
		0	Device online at IPL.
		1	Device offline at IPL.
			Segment Common to All Devices
0(0)	1		Internal job identification.
		xxxx	Job protection key. Set if the mounted volume is to be retained or contain a passed data set.
		.... 00..	Zeros.
		.... ..1.	Set during device allocation if volume is to be demounted and is retained or contains a passed data set. Causes job name in demount message.
		1	Set during device allocation if the volume to be mounted is to be retained or contain a passed data set.
1(1)	. 1	UCBFL5	Extended sense bytes.
		xxxx	Reserved.
		.... 1...	UCBSNADR and UCBNBRSN fields contain valid information.
		.... .1..	Device may not be allocated. OLTEP controls the device.
		.... ..1.	Device has alternate control unit address.
		1	Device has alternate channel path.
2(2)	. . 1	UCBID	UCB identification—X'FF'.

Offset	Bytes and Alignment	Field Name		Field Description, Contents, Meaning
3(3)	. . . 1	SRTESTAT		Status byte A.
		0...	....	Device is offline.
		1...	....	Device is online.
		.1..	....	Without multiple console support: Device is to be changed from online to offline status. With multiple console support: Device status is to be changed from oneline to offline, or from online to online active console.
		..1.	....	The mount status of the volume on this device is 'reserved'. (See Note A, below.)
		...1	....	UNLOAD operator command addressed to this device; the device is not yet unloaded.
		....	1...	Device is allocated.
		....	.1..	The mount status of the volume on this device is 'permanently resident.' (See Note A, below.) This is the system residence device. This is the primary console. With multiple console support: This is an online active console.
		....	...1	One of these: Standard labels have been verified for this tape volume. This is the secondary console.
				Note A: If the mount status of a volume is neither 'reserved' nor 'permanently resident,' then the volume is removable.
4(4)	1	UCBCHA		
		1...	....	This bit is turned on when a halt I/O (HIO) is issued for the device represented by this UCB.
		.1..	....	This bit indicates either (1) that the device was busy when IOS a sensettempted to issue a command, in which case the command will be issued when the device is free, or (2) IOS is waiting for ending status from a sense command issued to a TP or shared file device.
		..1.	....	UCBDSNS bit. When on, this bit indicates that a sense command for this device has been delayed due to a channel logout pending condition.
		...1	....	UCBDHIO bit. When on, this bit indicates that a halt I/O command for this device has been delayed due to a channel logout pending condition.
		....	xxxx	These four bits contain the physical channel address of the last physical channel used for the device represented by this UCB.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
5(5)	. 1	UCBUA	Unit address.
6(6)	. . 1	UCBFL1	Flag byte 1.
		1...	UCBBSY bit. Set with UCBPST to indicate successful start I/O operation, or CSW stored with non-busy indication. If the second condition occurs, the CCH or I/O interrupt handler treats request as an interruption. Reset at device end time.
		.1..	UCBNRY bit. Indicates device is not ready, or should not be started. Bit handled by data management, scheduler, ERP–WTO routines, and DDR.
		..1.	UCBPST bit. Request UCBLTS field not yet posted. I/O supervisor assumes current RQE valid. Set with UCBBSY; cleared at channel end.
		...1	UCBITF bit. Indicates an intercept condition; error detected on device after last request was posted complete. Next request is intercepted, and its control blocks used by error recovery routine.
		.... 1...	UCBCUB bit. RQE in UCBLTS field associated device. No other request may be started on this device. Set if start I/O instruction results in a device control unit or channel busy condition. Cleared before entering start I/O module.
		.... .1..	UCBDTR bit. Set for moving arm direct access devices to indicate data transfer is in process. Always on with UCBASK bit.
		.... ..1.	UCBASK bit. Set only for moving arm direct devices to indicate that stand–alone seek has been started, completed, or not needed since it was already properly positioned. Set with UCBBSY and UCBPST bits if stand alone seek is in progress.
		1	UCBERR bit. RQE in UCBLTS field associated to this device. No other request may be started on this device. Set by DDR, DAVV, and RMS routines. Also set by the I/O supervisor upon an EXCP inspect return from resident disk error recovery procedure.
7(7)	. . . 1	UCBDTI	Indexing value, used in locating the device table entry for this device type.
8(8)	1	UCBETI	A binary number used by the exit effect or routine to complete the 8–byte name of an IBM–supplied error routine for this device.
9(9)	. 1	UCBSTI	Value which, when multiplied by 10, becomes an index to the statistics table.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
10(A)	. . 1	UCBLCI	Value which, when multiplied by 8, becomes an index to the logical channel word for the logical channel containing the device.
11(B)	. . . 1	UCBATI	Index to the attention table.
12(C)	1	UCBCHM	Flags and channel mask.
		1...	SYSIN.
		.1..	SYSOUT.
		..1.	Assumed that this device will be allocated for a public volume request.
		...1	Rewind command has been addressed to this magnetic tape device by I/O support.
		 xxxx	I/O supervisor path mask (used where there are two or more paths to a device):
		.... 1...	Primary path to the device is inoperative.
		.... .1..	Optional path 1 to the device is inoperative.
		.... ..1.	Optional path 2 to the device is inoperative.
		1	Optional path 3 to the device is inoperative.
			In multiprocessing systems, bits 4 and 5 represent the paths from CPU A and bits 6 and 7 represent the paths from CPU B.
13(D)	. 3		Unit address (EBCDIC). For the 2305 this is the unit address of the base UCB.
16(10)	4	UCBTYP	Device type. For a description of this field see the publication *OS System Control Blocks,* GC28–6628.
20(14)	2	UCBLTS	Address of the request element used for the last activity on this device.
22(16)	. 2	UCBSNS	Sense information obtained when a sense command was executed.
			1285, 1287, and 1288, Optical Reader Segment
24(18)	4		Address of UCB extension for 1285, 1287, and 1288 Optical Readers.
			2495 Tape Cartridge Reader Segment
24(18)	4		Address of UCB extension for 2495 Tape Cartridge Reader.
			Universal Character Set (UCS) Segment
24(18)	1	UCBNBRSN	Number of sense bytes.
25(19)	3	UCBSNADR	Address of sense information.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
28(1C)	4	UCBXTADR	Address of UCB extension for 1403 and 3211 printers.
			Graphics Devices
24(18)	2		Additional sense information.
26(1A)	. . 1		Use count. Number of DCBs that are currently open for this device.
27(1B)	. . . 1		Graphics control byte for attention handling.
28(1C)	4		Address of task entry (TE) block.
32(20)	4		Restart address. The last start address.
36(24)	1		Device index. Device or devices on a control unit to which buffer sections are assigned.
37(25)	. 3		Buffer table address.
			Magnetic–Tape Devices
24(18)	1		Number of bytes of sense information (devices with extended sense).
24(18)	4		Additional sense information (2400/3400 Series Magnetic Tape Devices).
25(19)	. 3		Address of area containing sense information (devices with extended sense).
28(1C)	6		Volume serial number.
34(22)	. . 1		Status byte B. Volume status.
		x...	Device sharability:
		0...	Sharable.
		1...	Not sharable.
		..1.	Additional volume label processing.
		...1	Private–volume use status.
		.... 1...	Public–volume use status.
		1	If the multiple console support option is in the system, demount or mount messages have been issued and the message IDs are at offset 40 through 45. Data management OPEN routines will delete the messages and turn this bit off.
		.x.. .xx.	(Reserved bits).
35(23)	. . . 1	x...	Volume mount switch. Shows whether a volume has been mounted and the volume label is the type specified by the DD statement parameter. For more information see *OS System Control Blocks,* GC28–6628.
		.xxx xxxx	DCB Count. Number of DCBs open for this volume.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
36(24)	2		Data set sequence count.
38(26)	. . 2		Data set sequence number.
40(28)	6		Before OPEN: Message IDs. See offset 34, bit 7. After OPEN: Data set serial number.
46(2E)	. . 2		(Reserved)
48(30)	1	xxxx x..x	Tape options.
		00..	No error volume analysis and no error statistics by volume.
		01..	Error volume analysis only.
		110.	Error statistics by volume or error volume analysis and error statistics by volume. Records are to be written on the system management facilities data set (SYS1.MAN).
		111.	Error statistics by volume or error volume analysis and error statistics by volume. Records are to be written on the operator's console.
		...1	Error recovery routine is in control.
		.... 1...	End–of–volume condition has resulted in a volume statistics record for this volume.
		1	Unsolicited device end.
		.... .xx.	Reserved.
49(31)	. 3		Address of area containing CCW for opposite direction recovery and volume statistics area.
			2305 Fixed Head Storage and 3330 Disk Storage
24(18)	1		Number of extended sense bytes.
25(19)	3		Address of extended sense information.
			Direct-access devices (Except 2321 Data Cell Drive)
24(18)	4		Additional sense information.
28(1C)	6		Volume serial number.
34(22)	. . 1		Status byte B. Volume status.
		x...	Volume sharability:
		0...	Sharable.
		1...	Non–sharable.
		.xx.	(Reserved bits.)
		...1	Private–volume use status.
		.... 1...	Public–volume use status.
		.... .1..	Storage–volume use status.
		.... ..1.	JOBLIB data set is on this volume.
		1	Control volume. A catalog data set is on this volume.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
35(23)	. . . 1		Number of DCBs open for this volume. When shared DASD option is used, the count increases by 1 for each RESERVE macro issued by the user. Conversely, for each DEQ macro issued, the count is reduced by 1.
36(24)	4		Relative address of the volume table of contents for this volume, in the form TTR0.
40(28)	1		Number of RESERVE macro instructions issued.
41(29)	. 1		Device reservation indicator. In a system that includes the shared DASD option this indicator is set equal to the contents of the preceding field after a successful execution of a start I/O instruction for a direct access storage device (DASD).
42(2A)	. . 2		Save area for RQE address. Contains the address of the request queue element used in verifying the volume serial number in the UCB.
44(2C)	1		Flags/Count:
		1...	The Volume Serial Verification routine has issued a mount message.
		.1..	The Volume Serial Verification routine is in control.
		..1.	Indicates a first–time entry to the Volume Serial Verification routine for this Volume.
		...1	The volume label is on an alternate track. The alternate track procedure is in progress.
		.... 1...	The volume serial number has been verified by the Volume Serial Verification routine.
		xxx	A count of the requests for the device from the first requestor on the logical channel queue for this device.
45(2D)	. 3		Save area for DEB address. Contains the address of the data extent block (DEB) for the first requestor on the logical channel queue for this device.
48(30)	8		Address of last seek.
56(38)	1		Number of current users.
57(39)	. 3		Direct access event control block (ECB) address.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
60(3C)	4		Address of a direct access UCB extension. The first valid field is at offset 104.
			2321 Data Cell Drive
24(18)	4		Additional sense information.
			Error Routine Work Area
28(1C)	12		A work area for the error routine.
40(28)	2		(Reserved.)
42(2A)	. . 2	UCBRQESV	Address of RQE used to verify the volume serial number in the UCB. Set from UCBLTS after an unsolicited device end interrupt.
44(2C)	1	UCBFL4	A flag byte.
		1...	A mount request has been issued by the Volume Serial Verification routine.
		.1..	Volume Serial Verification routine is in control.
		..1.	Indicates a first entry of the volume serial Verification routine for this volume.
		...1	Volume label is on a alternate track; the alternate track procedure is in progress.
		.... 1...	Volume has been verified by the Volume Serial Verification routine.
		xxx	The number of requests for the device from the first user on the queue.
45(2D)	. 3	UCBORSV	Address of the DEB for the first user on the queue for this device.
48(30)	8	UCBSKA	Address for last seek, in the form MBBCCHHR.
			Description of Cell in Bin 0
56(38)	2	DCELBBNR	Bin number.
+2	. . 1	DCELSTAB	Status byte B. Volume status.
		x...	Volume sharability:
		0...	Sharable.
		1...	Not sharable.
		.xx.	(Reserved bits)
		...1	Private–Volume use status.
		.... 1...	Public–Volume user status.
		.... .1..	Storage–Volume use status.
		.... ..1.	JOBLIB data set is on this volume.
		1	Control volume. A catalog data set is on this volume.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
+3	. . 1	DCELSTAT	Cell/bin status.
		1...	Bin is online and normal cell is mounted in it.
		0...	Bin is offline or ballast cell is mounted in it.
		.1..	(Reserved bits)
		..1.	Reserved. Mount status of the cell in this bin.
		...1	UNLOAD operator command has been addressed to this bin; the bin has not yet been unloaded.
		.... 1...	Bin is allocated.
		.... .1..	Permanently resident—the mount status of this cell. If the mount status is neither reserved nor permanently resident, then it is removable.
+4	. 6	DCEVOLI	Volume serial number.
+10	. . 1	DCELJBNR	Internal job number.
+11	. . . 1	DCELDMCT	Number of data sets opened for this cell.
+12	3	DCELVTOC	Address of VTOC, in form TTR.
+15	. . . 1	DCELUSER	Number of data sets allocated to this cell.
			End of description of cell in bin 0.
72(48)	16		Description of cell in bin 1 (same format as description of cell in bin 0).
88(58)	16		Description of cell in bin 2 (same format as description of cell in bin 0).
104(68)	16		Description of cell in bin 3 (same format as description of cell in bin 0).
120(78)	16		Description of cell in bin 4 (same format as description of cell in bin 0).
136(88)	16		Description of cell in bin 5 (same format as description of cell in bin 0).
152(98)	16		Description of cell in bin 6 (same format as description of cell in bin 0).
168(A8)	16		Description of cell in bin 7 (same format as description of cell in bin 0).
184(B8)	16		Description of cell in bin 8 (same format as description of cell in bin 0).
200(C8)	16		Description of cell in bin 9 (same format as description of cell in bin 0).
216(D8)	4		Address of the direct–access UCB extension. First valid field is at offset 104.

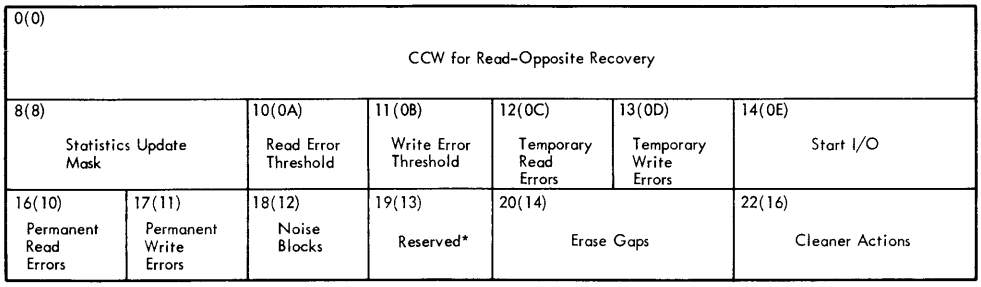
Volume Statistics Table

The volume statistics table contains information and statistics pertaining to volumes on magnetic–tape devices. It contains one entry (Figure 46) for each magnetic tape device in a system.

The address of each entry is contained in the unit control block for the device containing the volume. The entries may or may not be contiguous.

For 2400 series magnetic tape units the format of each entry varies according to the options selected at system generation time. If neither the error volume analysis (EVA) nor the error statistics by volume (ESV) options are selected, an entry will consist of only the first 8 bytes shown in Figure 46. If only EVA was specified, each entry will consist of the first 16 bytes shown. If ESV or both ESV and EVA were specified, the length of each entry will be the full 24 bytes.

For 3400 series magnetic–tape units, the length of each entry is always 24 bytes.



* 'Mode Set' when tape device has extended sense.

Figure 46. Volume Statistics Table Entry

SECTION 6: DIAGNOSTIC AIDS

General Register Assignments

Table 35 shows the general register assignments for the resident parts of the I/O supervisor (EXCP Supervisor, I/O Interruption Supervisor, and Error EXCP Supervisor). Assignments for other routines can be found in the prologs to the routine listings.

Table 35. General Register Assignments

Register	Symbol	Assignment
0	REG0	Temporary storage
1	TSTREG	RQE Address (For assigned but not–queued RQE)
2	IOBREG	IOB address
3	DEBREG	DEB address
4	DCBREG	DCB address
5	BASREG	Base register for I/O supervisor
6	UAREG	Channel and unit address
7	UCBREG	UCB address
8	LNKRG1	Linkage register; second base register when two–base feature is required.
9	ICREG	Work register
10	WKREG1	Work register
11	WKREG2	Work register
	PRFXREG	Prefix storage address register
12	WKREG3 LINKRG3	Spare work/linkage register
13	LCHREG	Logical channel word address
14	LNKRG2	Linkage register
15	APBSRG	Used for calculating addresses of appendages to be invoked and used as a base register for the appendages

System Completion Codes

When a task is terminated abnormally, a three–digit system completion code printed in the storage dump generally indicates why. The publication *OS Messages and Codes*, GC28–6631, contains a complete list of system completion codes. The meanings of the codes produced when abnormal termination results from trouble during input/output processing are shown in Table 36.

Table 36. System Completion Codes for Input/Output Operations

Code	Explanation	Comments
0F1	A program interruption occurred during execution of an instruction in the I/O interruption handler. The interruption probably occurred because an input/output block, data control block, or data extent block was modified after the EXCP macro instruction was issued. Check to determine whether an access method routine was overlaid in the problem program storage area.	The interruption code field of the program old PSW (at location 28) will identify the cause of the interruption. In systems with MFT, the PSW is valid only when the first four digits are 0004.
0F2	A program interruption occurred during execution of an instruction in a type 1 SVC routine. The interruption probably occurred because incorrect parameters were passed to the type 1 SVC routine.	See comments for code '0F1'. Both the EXCP supervisor and the error EXCP supervisor are type 1 SVC routines.
400	The input/output supervisor found one of the following control blocks to be invalid: • Input/output block (IOB). • Data control block (DCB). • Data extent block (DEB). • Event control block (ECB). Information is placed into the first three blocks from the DD statement, the DCB macro instruction, and the macro instruction by which the I/O operation was requested. The DD statement or the macro instructions may have been specified incorrectly. Also, program errors may have caused the control blocks to be modified.	The input/output supervisor's EXCP Validity Check routine (Chart AA) initiated abnormal termination by passing control to the supervisor's ABTERM) routine. For a description of how the control blocks are checked, see the topic "Validating Input Data" in Section 2.

Patch Area at IECINT

At IECINT is a 17–word storage area that can be used for diagnostic work. Since its location is not standard, but differs for each system, the service aid program IMBMDMAP can be used to determine the true location of the label IECINT in the nucleus.

Generalized Trace Facility

Table 37 shows the trace entries for the Generalized Trace Facility that are within the I/O Supervisor.

Table 37. Trace Entries for Generalized Trace Facility

Error ID	Location	Registers	
5FF0	Immediately after an SIO	R1 R6 R10	RQE address Device address SIO condition code
5FEE	I/O interruption without an associated UCB		
2FDF	PCI interruption only	R7	UCB address
5FEF	All other interruptions with associated UCB	R7	UCB address

SECTION 7: APPENDIXES

Appendix A: Supporting SVC Routines

The SVC routines described in this appendix are not generally used during normal processing of requests for I/O operations. They do, however, provide users with a capability for referring to, obtaining, and changing some of the data used in processing the I/O requests.

Purge Routine (SVC 16)

The Purge routine stops the processing of I/O requests by removing request queue elements from queues. Depending upon the options specified in a parameter list which is provided as input (Figure 47), the Purge routine can remove request queue elements from:

- A logical channel queue
- The supervisor's request block queues
- The supervisor's asynchronous exit queue
- The DDR wait queue

The Purge routine can remove the elements representing all requests for a particular data set; or it can remove the elements representing all requests for a particular task. The method to be used is indicated in the seventh bit of the options field in the parameter list. The general flow of control within the Purge routine is shown in Figure 49. The PURGE macro instruction is described in *OS Data Management for System Programmers,* GC28–6550.

0(0) PRGOPT Purge Options	1(1) PRGDEB Address of Data Extent Block
4(4) PRGCOD Completion Code	5(5) PRGTCB Address of Task Control Block
8(8) PRGCTR Quiesce Count	9(9) PRGCHN Address of First Link in Chain
12(0C) * PRGFLG Flags	13 (0D) PRGQPL Address of Quiesce I/O Parameter List

* TSO only

Figure 47. Purge Routine Parameter List

Removing Elements From Logical Channel Queues

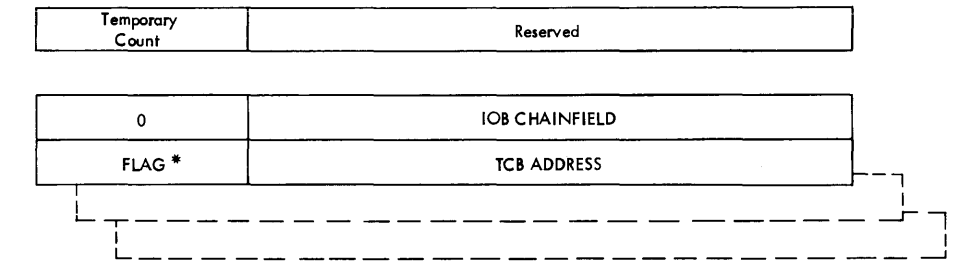
If all requests for a particular data set are to be purged, the Purge routine examines the data extent block (DEB) for the data set, and removes all request queue elements from the logical channel queue for the device or devices whose unit control block (UCB) addresses are contained in the DEB. When an active shared device is allocated with a purged request, the UCB's HIO flag is set by the I/O supervisor to issue a RELEASE to the device if its UCB reserve count field is zero.

When the elements for all requests associated with a particular task are to be purged, the Purge routine scans the entire request elements table to locate and remove the request queue elements for the task.

PURGE ROUTINE PARAMETER LIST

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
0(0)	1	PRGOPT	Purge options.
		0...	Purge request queue elements for all entries in the data extent block (DEB) chain, starting with the DEB whose address is in PRGDEB.
		1...	Purge only the request queue element for the DEB whose address is in PRGDEB.
		.0..	Do not post the event control blocks for the purged request queue elements.
		.1..	Post the event control blocks for the purged RQEs. (A hex 48 completion code is used.)
		..0.	Allow the activity to quiesce.
		..1.	Halt the I/O activity. (The effect of the Halt I/O instruction is simulated if the operation is a seek.)
		...0	Purge all requests.
		...1	Purge only related requests.
		.... 0...	Normal purge.
		.... 1...	Purge TCB list.
		.... .0..	Purge the asynchronous exit queue, the request block queue, the logical channel queue, and the DDR wait queue.
		.... .1..	Purge the logical channel queue and purge the asynchronous exit queue removing only RQEs for requests in error, and the DDR wait queue. Bypass the request blocks.
		.... ..0.	Purge by data extent block.
		.... ..1.	Purge by task control block. When this bit is on, the setting of bit 0 is ignored.
		x	Not used.
1(1)	. 3	PRGDEB	Address of data extent block.
4(4)	1	PRGCOD	Purge routine completion code.
5(5)	. 3	PRGTCB	Address of task control block.
8(8)	1	PRGCTR	Quiesce count. The number of active request queue elements for which I/O activity has not yet been completed.
9(9)	. 3	PRGCHN	Address of the first link in the chain of IOBs which are purged. The first link can be located in the user's area, or in the DEBUSPRG field of the DEB. It will point to the first IOB in the chain. The last IOB in the chain will contain ones in the low–order byte of the restart address (IOBRST) field.

Offset	Bytes and Alignment	Field Name	Field Description, Contents, Meaning
12(C)	1	PRGFLG	Purge flags.
		0...	Purge entry.
		1...	Wait entry.
		.0..	Return before wait.
		.1..	Purge and wait.
		..0.	DEQ before WAIT.
		..1.	No DEQ before WAIT (set before system DEB purged).
		...x	Not used.
		.... x...	Not used.
		.... .x..	Not used.
		.... ..x.	Not used.
		x	Not used.
13(D)	. 3	PRGQPL	Address of quiesce I/O parameter list.



* Field for Last Entry is X '80'

Figure 48. Quiesce I/O Parameter List

QUIESCE I/O PARAMETER LIST (TSO Only)

Offset	Bytes and Alignment	Field Description
0(0)	1	Temporary count field.
1(1)	. 3	Not used.
8(8)	8	First parameter list entry.

Byte	Description
0	Not used.
1–3	IOB chain field.
4	QPL flags.
	0... .... More entries follow.
	1... .... Last entry.
	.0.. .... Not a current entry.
	.1.. .... Current entry.
5–7	Address of TCB to be purged.

Additional parameter list entries may be present.

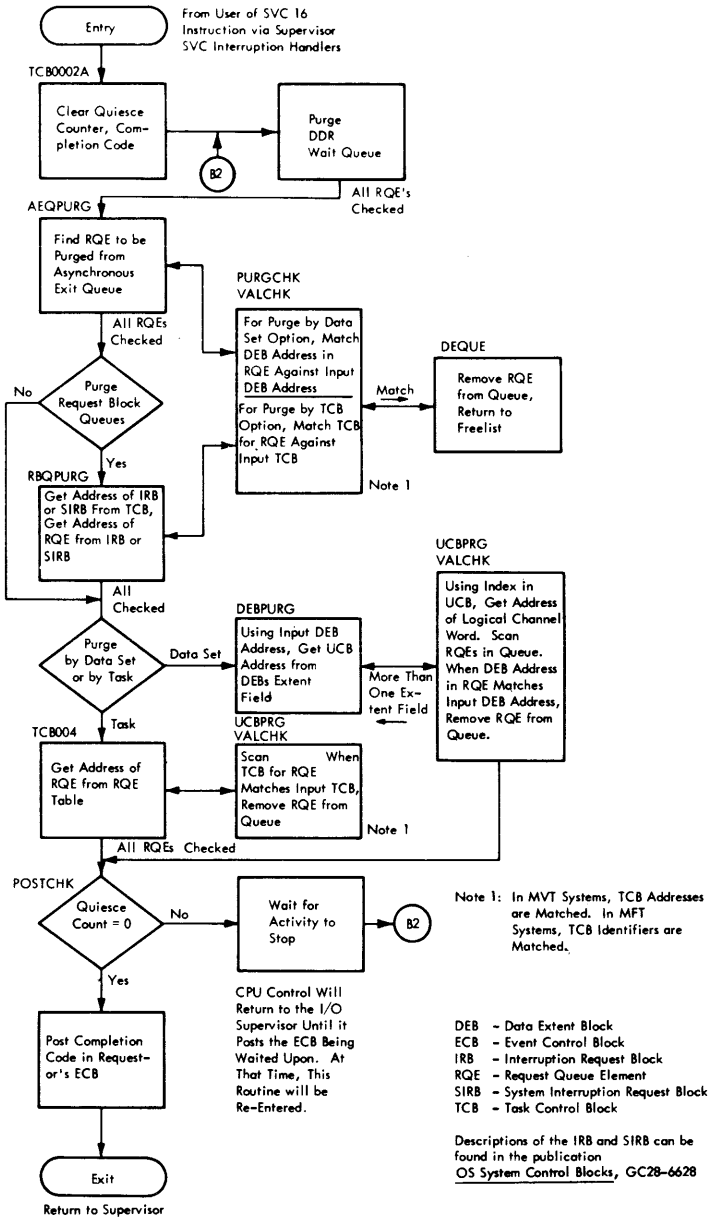


Figure 49. Purge Routine

Removing Elements From the Supervisor's Request Block Queues

To remove elements from a supervisor request block queue, the Purge routine obtains the address of the first request block in the queue from the TCB whose address is passed as input. When no TCB address is passed, it assumes that the current TCB is the input TCB. The Purge routine then scans the entire request block queue. For each system interruption request block (SIRB) and interruption request block (IRB) in the queue, the Purge routine removes the RQEs containing a DEB address which matches the input DEB address (for a purge by data set); or removes the RQEs containing a

TCB address which matches the address of the input TCB (for a purge by task in MVT systems); or removes the RQEs containing a TCB identifier which matches the TCB identifier of the input TCB (for a purge by task in MFT systems).

Descriptions of the SIRB and IRB are contained in the publication *OS System Control Blocks,* GC28–6628.

Removing Elements From the Supervisor's Asynchronous Exit Queues

To remove request queue elements from the supervisor's asynchronous exit queue, the Purge routine first obtains the address of the queue from the communications vector table. It then scans the entire asynchronous exit queue, removing every RQE containing a DEB address which matches the input DEB address (for a purge by data set); or removing every RQE containing a TCB address which matches the address of the input TCB (for a purge by task in MVT systems); or removing every RQE containing a TCB identifier which matches the TCB identifier of the input TCB (for a purge by task in MFT systems). When a TCB address is not passed as input for a purge by task request, the Purge routine uses the current TCB for the matches.

The communications vector table is described in the publication *OS System Control Blocks,* GC28–6628.

The IOB Chain

The Purge routine links the IOBs for purged requests together in a chain beginning at the address specified in the third word of the Purge routine parameter list (Figure 50). A RESTORE macro instruction could then be used to restart the requests. The Purge routine does not create an IOB chain when the halt I/O option is specified with the purge–by–TCB option.

The Quiesce Option

When the quiesce option is specified, the Purge routine increments two counters by one for each I/O request awaiting completion:

- A main purge counter in the parameter list
- A secondary counter in each effected DEB

Thus, if there is a request to quiesce activity for a specific data set, both counters will have a count of one. If there is a request to quiesce the activity on all data sets of a task, however, there will be counts in each DEB counter reflecting the number of not–yet–completed requests for the data sets, and there will be a total count in the main counter.

Every time the Purge routine increments a counter, it places a pointer to the purge parameter list into the 'address of purge parameter list' field of the DEB. Also, after it has put the total count in the main counter, the Purge routine issues a WAIT macro instruction.

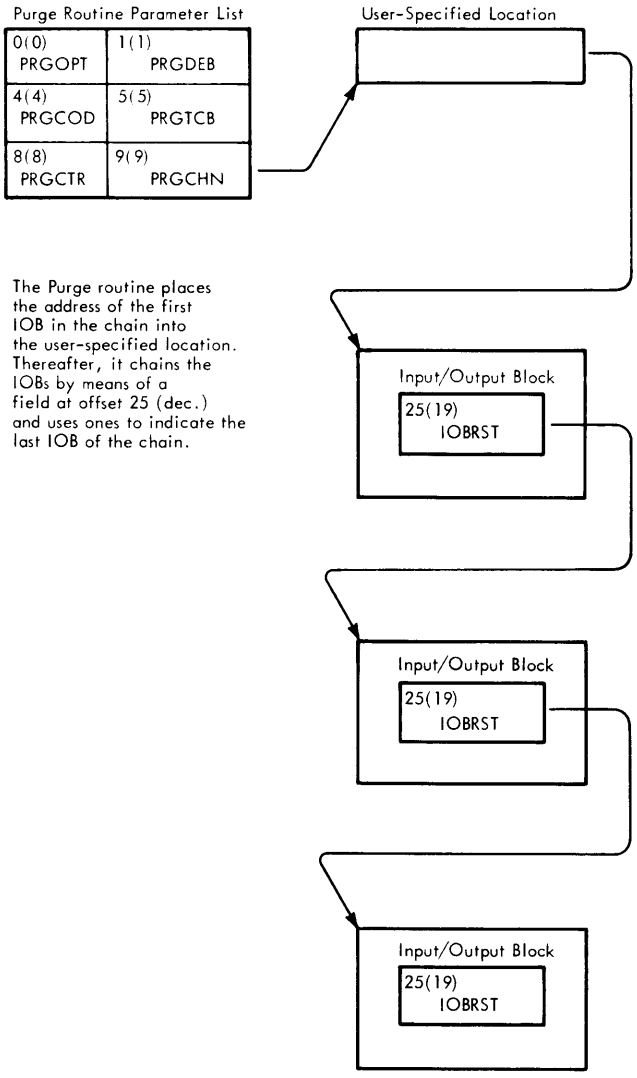


Figure 50. Purge Routine IOB Chain

When I/O activity has been completed for a request, the I/O interruption supervisor will enter its Quiesce Complete subroutine (entry point PRGCOMA or PRGCOMB) if it finds an address in the 'address of purge parameter list' field of the DEB for the newly completed activity. The Quiesce Complete subroutine decrements both the main and secondary counters by one. If a DEB secondary counter is zeroed, the 'address of purge parameter list' field in the DEB is also zeroed. When the main counter in the parameter list is zeroed, indicating the quiesce is complete, the Quiesce Complete subroutine posts the purge ECB. If the main counter is not zeroed, the Quiesce Complete subroutine returns control to the I/O interruption supervisor.

Restore Routine (SVC 17)

The Restore routine restarts the processing of requests that have been dequeued by means of the Purge routine if Halt I/O option was not specified with the purge–by–TCB option. Using a pointer to the first IOB in a chain of IOBs that it receives as input in register 1, the Restore routine issues the EXCP macro instruction for each IOB in the chain.

DEVTYPE Routine (SVC 24)

The DEVTYPE routine supplies information about the characteristics of I/O devices. The instructions in the expansion of the Locate Device Characteristics (DEVTYPE) macro instruction place parameters into general registers, and the DEVTYPE routine uses the parameters to identify the device and to find where it should place the output information.

The DEVTYPE macro instruction is described in the publication *OS Data Management for System Programmers,* GC28–6550.

Using the DD name it receives as input, the DEVTYPE routine finds the corresponding task input/output table (TIOT) entry, and uses it to locate the proper UCB. The DEVTYPE routine then obtains the device type field from the UCB and places it into the first word of the output area.

If the DEVTAB parameter was not specified, the output area will contain two words of information. The DEVTYPE routine determines the maximum block size from the device charactersitics table (if the device is a direct access device) or from internal constants, and moves it to the second word of the output area.

If the DEVTAB parameter was specified in the DEVTYPE macro instruction, and the device is a direct access device, the DEVTYPE routine will provide three additional words of information. The DEVTYPE routine locates the device characteristics table via the communication vector table, moves the appropriate entry into the low order three words of the output area, and moves the blocksize field to the second word of the output area.

Before relinquishing control, the DEVTYPE routine places a return code into register 15. A return code of 00 indicates that the request was completed successfully. A return code of 04 indicates one of the following conditions:

- No output area specified: The area parameter was not included in the DEVTYPE macro instruction.
- DD name not found: No TIOT entry exists that corresponds to the DD name supplied.
- Invalid UCB unit type field: The UCB unit type field (byte 4 of the device code field) does not specify a direct access, tape, or unit record device.

A return code of 08 indicates that an invalid output area address was specified.

IOHALT Routine (SVC 33)

The IOHALT routine stops all activity on the teleprocessing device whose unit control block (UCB) address is passed in register 1. It does not stop activity on nonteleprocessing devices.

The IOHALT routine checks the validity of the UCB address it receives by matching it against the UCB addresses in the UCB lookup table. If the address passed is valid and if the device to be stopped is a teleprocessing device, the IOHALT routine gives control to the resident Halt I/O routine (entry point IECIHIO), which issues a Halt I/O instruction and returns. The IOHALT routine places a completion code into register 15 before relinquishing control:

Code (Hex.)	Meaning
00	The device was stopped.
04	The device is not running.
08	The device was not stopped because it is not a teleprocessing device.
0C	The device was not stopped because the UCB address was invalid.

SYS1.LOGREC Recorder and Statistics Update Routine (SVC 76)

The SYS1.LOGREC Recorder and Statistics Update routine (IFBSTAT) writes records on the SYS1.LOGREC data set, formats records when the End–of–Day (EOD) command is entered, and issues warning and error messages when an I/O error occurs during recording operations or when the SYS1.LOGREC data set is full or nearly full.

The first load module of IFBSTAT receives control from the Outboard Recording routine and the Miscellaneous Data Recording routine when records are to be written on the SYS1.LOGREC data set. It also records data formatted by the second and third load modules of IFBSTAT. The requestor of a recording operation places a pointer to the data to be recorded in register 1 and the twos complement of the record length in register 0.

The second and third load modules of IFBSTAT receive control when an End–of–Day (EOD) command is entered. They build Short OBR records (Figure 40) for each device whose statistical counters contain a nonzero value.

The fourth SVC 76 load module issues environment recording error messages. Diagram 15 illustrates this function.

VOLSTAT Routine (SVC 91)

The first load module of the VOLSTAT routine constructs error–statistics–by–volume (ESV) records and, depending upon what was specified during system generation, writes them on either the console output device or the system management facilities SYS1.MAN data set.

Data management Close and EOV routines pass control to the VOLSTAT routine when the volume is demounted.

VOLSTAT routine obtains error statistics from the volume statistics table, and obtains other identifying information from the UCB, DCB, or JFCB and DEB. After writing an ESV record, the VOLSTAT routine clears the counters in the volume statistics table and returns control to the Close or EOV routine.

The second load module is called to read the buffered log data of an IBM 2305 Fixed Head Storage or an IBM 3330 Disk Storage. This load module is activated when a new volume is mounted or when the operator enters a HALT EOD command.

TCB EXCP (SVC 92) (TSO only)

The TCB EXCP routine allows the user to specify, in register 0, a TCB address associated with the IOB address passed in register 1. The specified TCB will be the one associated with the RQE.

Extended SVC Routine (SVC 109)

An Extended SVC routine (IGX00015) is used by the Task Termination routine to insure that a task does not leave outstanding I/O requests.

The routine checks each RQE in the system, unless outstanding teleprocessing-based I/O is found. If an RQE is assigned, the TCB is checked for an equal condition. If the equal condition is found, the UCB is checked for a teleprocessing-device indicator. If the device indicator is found, an ABEND is issued.

If there are no RQEs assigned for the terminating task, an SVC 3 is issued. If the assigned RQEs do not represent the teleprocessing-associated I/O, the Extended SVC routine issues the PURGE macro to call the Purge routine (SVC 16). If an IOB chain for the Restore routine (SVC 17) results, an ABEND is issued. If no IOB chain is built, an SVC 3 is issued.

Appendix B: Alternate Path Retry

In systems with the alternate path selective retry option, when a device can be reached by more than one path and there is a failure of one of the paths, the others are automatically tried, one by one, either until the operation is successful or until the error is declared permanent. In addition, the operator is provided with a Vary Path command by which he may add or remove paths to a device. The two alternate path retry functions are called 'selective retry' and 'vary path,' respectively.

The Selective Retry Function

Without alternate path retry, each time there is a channel failure and the Test Channel routine is entered preparatory to retrying the I/O activity, it selects a path for the retry from the alternate path table. The selected path may or may not be the failing channel, because the alternate path table is not changed after I/O errors.

With alternate path retry, the Test Channel routine refers to the path mask field of the unit control block for the requested device rather than to the alternate path table, and failing paths are removed from the path mask when channel errors occur.

Error recovery routines pass control to the Alternate Path Retry (Chart EA) before attempting each restart. The Alternate Path Retry routine obtains and saves the original channel mask from the requested device's unit control block in a table called the channel error block table. It then turns off the failing channel's bit in the channel mask field of the unit control block and returns control to the I/O error routine, which begins the retry attempts.

To prevent a situation where all paths would become unavailable, the Alternate Path Retry routine restores the original path mask to the unit control block if the last available path is about to be used. The I/O error routine may then initiate the retry cycle again, depending upon whether the specified number of retries has been reached.

The Vary Path Function

When the operator issues any command, job management command processing routines are entered. For the Vary Path command, the Vary Path Command Processor routine is given control (Figure 51). It adds or removes paths to a device by setting bits in the path mask table of a unit control block on or off.

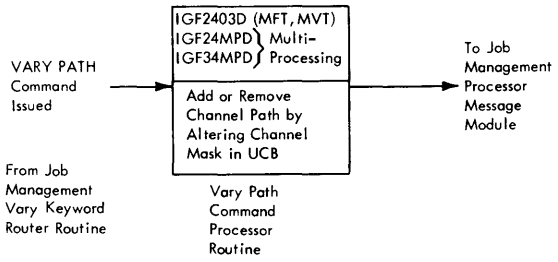


Figure 51. Vary Path Command Processing

Appendix C: Channel Check Handler (IGFCAT)

The Channel Check Handler (CCH) can be used with the System/360 2860, 2870, and 2880 stand–alone channels, and the System/370 135, 145, 155, 165, and 195 integrated channels. Use of CCH is either optional, mandatory, or automatic as follows:

- For Models 65, 75, and 91: CCH may optionally be selected when the system is generated.
- For Model 65 Multiprocessing: CCH must be specified when the system is generated.
- For Models 85, 135, 145, 155, 165, and 195: CCH is automatically included.

CCH consists of one permanently resident module, which is channel—and model—independent, and eight channel–dependent channel error analysis routines—one each for the 2860, 2870, 2880, 135, 145, 155, 165, and 195 channels. The analysis routines reside on SYS1.LINKLIB before nucleus initialization. At nucleus initialization, only those analysis routines needed for the channels in the system and online are made resident in the nucleus. See *OS IPL & NIP Logic,* GY28–6661, for more information about nucleus initialization of CCH.

Channel Logout Pending

If a channel error occurs (asynchronous or associated with an active request) on a 2880 block multiplexor channel or an integrated block multiplexor channel (Models 145 or 155) while IOS is running in a disabled state, and IOS attempts to issue a SIO or HIO instruction to that channel, a channel logout pending condition occurs. The channel presents condition code 1 as initial status for the I/O instruction. A full CSW will be stored. The CSW is all zeros except for bit 5 (channel logout pending) and bit 45 (channel control check). When IOS detects this condition, it enables I/O interruptions, allowing the channel to logout. IOS *fields* the interruption (reflecting the channel error) and after passing control to and receiving it back from CCH, resumes processing any I/O requests that were delayed by the channel logout pending condition (Chart BR).

CCH Processing

CCH is entered at entry point IGFCAT from various routines within the I/O supervisor when a channel check condition is detected (bits 44, 45, or 46 set in the CSW, indicating channel data check, channel control check, and interface control check, respectively).

CCH constructs an error recovery procedure interface block (ERPIB) which contains the information a device–dependent error recovery procedure needs to set up for a retry of the operation by the I/O supervisor. An inboard record for SYS1.LOGREC is also constructed by CCH; it contains the last four bytes of the ERPIB, the channel logout, and other information describing the environment of the channel failure. An operator awareness message is issued by the outboard recorder routine of the I/O supervisor each time an inboard record is written on SYS1.LOGREC.

The I/O supervisor gives control to CCH through the SER interface routine (SERR04). CCH receives control from any one of seven exit points in five routines of

the I/O supervisor. At each exit point, a specific code is passed to CCH. See Table 38.

Table 38. Exit Codes Passed to CCH by I/O Supervisor Routines

I/O Supervisor Routine Exit Point	I/O Supervisor Routine	Decimal Exit Code	Symbolic Entry Point in CCH
Following an SIO instruction	Direct–access start	0	CCHSSK
Following a TIO instruction	Direct–access start	4	CCHTIOSK
Following an SIO instruction	Sense subroutine	8	CCHSNS
Following a TIO instruction	Sense subroutine	12	CCHTIOSN
Following an SIO instruction	Post start I/O	16	CCHSIO
Following an interruption	I/O Interruption supervisor	20	CCHINT
Following an HIO instruction	Halt I/O subroutine	24	CCHHIO

This code is placed into the high–order byte of the CCH base register (register 15) by the I/O supervisor routine in control before any instructions are executed, enabling CCH to determine which routine had control when the channel check interruption was detected. CCH retrieves this code from register 15 and uses it to branch to the appropriate CCH interception–dependent routine (that is, the CCH routine that is later entered depending on which I/O supervisor routine intercepted the channel error).

At various points in its processing, CCH must decide to do one of the following, depending on the type and severity of the failure:

- If recovery from the channel error is possible, control is returned to the I/O supervisor. The I/O supervisor gives control to the appropriate device–dependent error recovery procedure (ERP).
- If recovery from the channel error is not possible (the failure environment is invalid or a system reset has occurred), control is passed to the machine check handler to write the inboard record on SYS1.LOGREC and to place the system in the wait state. If the machine check handler is not in the system, SER0 or SER1 is entered. If no SER is in the system, the wait state is entered.

CCH always produces an ERPIB. This block is intended to be placed in the ERPIB table for use by the appropriate ERP and in the inboard record. However, in some cases (such as catastrophic error, nonretryable condition, or the ERP not needing an ERPIB to set up for retry), the ERPIB is not placed in the ERPIB table but is produced only for inclusion in the inboard record. When a CCH routine determines that the ERPIB is not to be placed in the ERPIB table, the routine sets the record–only switch to indicate to other CCH routines that the ERPIB will be used only for the inboard record.

CCH Routines

The central CCH module (IGFCAT) consists of several routines:

- Initial entry routines. These routines find available ERPIBs and inboard records and fill them with information that is not channel or interception–dependent.
- Interception–dependent routines. The appropriate routine for the error is entered from a branch table. It sets a bit to indicate from where CCH was entered, and then passes control to ERPIBSET. Upon return from ERPIBSET, it passes control to the UCB search routine.
- ERPIBSET routine. This routine fills the ERPIB with more common information. It then passes control to the correct analysis routine to complete the ERPIB.
- UCB search routine. This routine completes the inboard record by filling in the addresses of up to eight devices active on the channel at the time of failure. It then returns control to the I/O supervisor.

The remainder of CCH is composed of the analysis routines. Only the analysis routine for the channel on which the error occurred is entered when a channel fails.

Initial Entry Routines

An initial entry routine gains control first. This routine inserts X'01' into byte 3 of the machine check new PSW. If a machine check interruption occurs during CCH processing, this code indicates to the machine check handler that CCH was in control when the interruption occurred. This initial entry routine then checks for a system termination condition. If one exists, CCH will process the channel error and produce an inboard record to be written by the machine check handler. When no system termination condition is indicated, the ERPIB entry find routine gets control.

The ERPIB entry find routine scans the ERPIB table to find an available ERPIB, and checks to see if a previous error occurred on the failing channel. This routine can also free an ERPIB, if necessary, for placement in an inboard record for the machine check handler to write on SYS1.LOGREC. The data collection routine then gets control.

The data collection routine scans the inboard record area to find an available inboard record. If it finds one, the routine sets a bit in the CCH parameter table for use by the statistic data recorder routine and the statistics update routine of the I/O supervisor. If no inboard record is available, it passes control to the branch table routine. The data collection routine also checks to see if it was entered because a system termination condition exists. If so, this routine frees an inboard record and fills it with common information. The branch table routine then gets control.

The branch table routine routes control to the correct interception–dependent routine. The exit code provided by the I/O supervisor routine is used as an index value into the branch table.

Interception–Dependent Routines

There are four interception–dependent routines:

- Sense interception routine (CCHSN or CCHTIOSN)
- Stand–alone Seek/Start I/O interception routine (CCHSSK, CCHTIOSK, or CCHSIO)

- Interruption interception routine (CCHINT)
- Halt I/O interception routine (CCHHIO)

Each interception–dependent routine sets a bit in the ERPIB to indicate where the channel check was intercepted, and passes control to the ERPIBSET routine to complete the ERPIB. Upon return from ERPIBSET, the interception–dependent routine passes control to the UCB search routine.

- The sense interception routine also checks the termination and sequence codes in the ERPIB (upon return from ERPIBSET) for selective reset and system reset conditions. Either of these conditions, or a fourth entry for a channel control check or an interface control check, causes this routine to set the no–retry bit in the ERPIB to indicate a channel error in the IOB, and to delete the sense operation.
- The interruption interception routine also checks for a special–handling condition to handle asynchronous device and attention interruptions. It then zeros the proper CSW bits.
- The Halt I/O interception routine passes control to the ERPIBSET routine to create an ERPIB for the inboard record only. No error recovery is attempted if a Halt I/O instruction has failed, because a channel error during a Halt I/O operation results in a stopped device.

ERPIBSET Routine

The ERPIBSET routine first moves the UCB address to the ERPIB. The routine then branches to the appropriate channel error analysis routine to complete the ERPIB. Upon return, various conditions are checked. The ERPIBSET routine next moves the ERPIB and the failing CCW into the inboard record. It moves the ERPIB into the ERPIB table, to be used for retry by the error recovery procedure if the error recovery procedure can retry the operation. The ERPIBSET routine then returns control to the interception–dependent routine from which it received control.

UCB Search Routine

The UCB search routine completes the inboard record by moving into it the addresses of up to eight busy units on the channel at the time of failure. It then places multiprocessing information in the inboard record if necessary. The routine cannot complete the inboard record if none is available.

This routine also checks for a system termination condition to determine if a recursion through CCH is needed to construct an inboard record. If a recursion is needed, this routine loads X'0F' at decimal location 115, loads the machine check new PSW, and thus gives the machine check handler control to write the inboard record on SYS1.LOGREC and to terminate the system. If system termination is not required, this routine clears the code at decimal location 115, and reenters the I/O supervisor at the location indicated in register 14.

Channel Error Analysis Routines

CCH has a separate channel error analysis routine for each type of channel.

2860 Channel Error Analysis Routine (IGFCCH60)

The 2860 analysis routine checks the channel logout data at decimal location 304. If the channel logout contains a full word of ones (indicating that the channel failed to log out fully), the routine indicates record–only, system–termination, and no-log conditions. These conditions are checked by other CCH routines. If the channel logged out successfully, the 2860 analysis routine checks the validity of the CSW fields, and sets appropriate bits.

The routine then sets sequence and termination codes in the ERPIB based on the presence of a channel control check or an interface control check. It determines the codes for a channel control check through count and parity checks in the 2860 parity check subroutine. It determines codes for an interface control check directly from the channel logout.

The routine then insures valid unit address parity, and compares the hardware unit address with the unit address passed to it by the I/O supervisor. It indicates the validity of the unit address in the validity indicator byte of the ERPIB. Finally, having completed the ERPIB the routine moves the 2860 channel logout into an available inboard record, sets the logout area to ones, and returns control to the ERPIBSET routine. When no inboard record is available, it returns control directly to the ERPIBSET routine.

2870 Channel Error Analysis Routine (IGFCCH70)

The 2870 analysis routine checks the channel logout data at decimal location 304. If the channel logout contains a full word of ones (indicating that the channel failed to log out fully), or if a system reset exists in the logout, the routine indicates record–only and system–termination conditions. These conditions are checked by other CCH routines. If the channel logged out successfully, the 2870 analysis routine checks the validity of the CCSW fields, and sets appropriate bits.

The routine then sets sequence and termination codes in the ERPIB based on the presence of a channel control check or an interface control check. It determines the codes for a channel control check through parity, count, and/or data transfer checks. It determines codes for an interface control check directly from the channel logout.

The routine then ensures valid unit address parity and compares the hardware unit address with the unit address passed to it by the I/O supervisor. It indicates the validity of the unit address in the validity indicator byte of the ERPIB. Finally, having completed the ERPIB, the routine moves the 2870 channel logout into an available inboard record, sets the logout area to ones, and returns control to the ERPIBSET routine. When no inboard record is available, it returns control directly to the ERPIBSET routine.

2880 Channel Error Analysis Routine (IGFCCH80)

The 2880 analysis routine operates differently from the 2860 and 2870 routines. It analyzes nine words of the 28-word logout and fills the ERPIB with the results of that analysis. It does not indicate termination code 3 (system reset) in the ERPIB because the 2880 channel does not issue system reset to a device. It can issue sequence codes of 0 to 5.

The 2880 analysis routine differs by issuing an "equipment check" for an incomplete channel logout, an unreliable CSW, or a unit address in the PSW that cannot be guaranteed correct. The "equipment check" is similar to a machine check except that it indicates whether the channel represented the correct data to the CPU.

The routine determines the logout address, since it varies depending on the CPU to which the 2880 channel is attached and checks for a no–log condition to determine whether normal operations should continue. If they should, several other tests are performed.

If a channel data check is present, the routine indicates a record–only condition and:

1. Sets a bit in the validity indicator byte
2. Moves the ERPIB to an available inboard record
3. Sets the logout area to ones
4. Returns control to the ERPIBSET routine

If an inboard record is not available, control passes directly to the ERPIBSET routine.

If a channel control check or an interface control check occurred and the channel logout contains a fullword of ones, the routine indicates record–only and system–termination conditions before it

1. Sets a bit in the validity indicator byte
2. Moves the ERPIB to an available record
3. Sets the logout area to ones
4. Returns control to the ERPIBSET routine

The routine then determines the proper sequence and termination codes, checks the command address, unit address, and unit status validity, and indicates a valid retry condition in the ERPIB.

If the no–log switch is set, the routine compares the channel number in the I/O old PSW against the channel number in the channel logout. A match causes normal operations to continue after indicating the no–log conditions. No match means that recovery is impossible, so the routine indicates a system termination condition and:

1. Sets a bit in the validity indicator byte
2. Moves the ERPIB to an available record
3. Sets the logout area to ones
4. Returns control to the ERPIBSET routine

135 Channel Error Analysis Routine (IGFCCH35)

The 135 analysis routine differs from the 2860, 2870, and 2880 analysis routines in that it does not analyze the channel logout; instead, it uses the hardware–generated extended channel status word (ECSW). Since the ECSW contains the same type of information as the last three bytes of the ERPIB, the routine moves the last three bytes of the ECSW from decimal location 176 to the last three bytes of the ERPIB.

If the instruction on which the error occurred was a Test I/O, this routine compares the unit address supplied by the hardware in decimal location 186 with the unit address

passed by the I/O supervisor. If they do not match, the routine sets the unit address valid bit in the work ERPIB to zero.

If there is valid channel logout data and an inboard record is being created, the routine saves the logout in the inboard record. The logout is copied from decimal location 256.

145 Channel Error Analysis Routine (IGFCCH68)

Like the 135 analysis routine, the 145 analysis routine moves the last three bytes of the ECSW from decimal location 176 to the last three bytes of the ERPIB.

If the instruction on which the error occurred was a Test I/O, this routine compares the unit address supplied by the hardware in decimal location 186 with the unit address passed by the I/O supervisor. If they do not match, the routine sets the unit address valid bit in the work ERPIB to zero.

If there is a valid channel logout and an inboard record is being created, the routine saves the logout in the inboard record. The I/O extended logout (IOEL) pointer in decimal location 172 points to the logout area from which the logout can be copied.

155 Channel Error Analysis Routine (IGFCCH48)

Like the 135 and 145 analysis routines, the 155 analysis routine moves the last three bytes of the ECSW from decimal location 176 to the last three bytes of the ERPIB.

If the instruction on which the error occurred was a Test I/O, this routine compares the unit address supplied by the hardware in decimal location 186 with the unit address passed by the I/O supervisor. If they do not match, the routine sets the unit address valid bit in the work ERPIB to zero.

The 155 channels do not log out.

Appendix D: Direct–Access Volume Verification

If the option to verify volume serial numbers is selected during system generation, the input/output supervisor checks the serial numbers of newly mounted volumes against serial numbers in the unit control blocks (UCBs) for the devices containing the volumes. It issues messages to the operator when the wrong volumes have been mounted.

When an operator readies a device after mounting a volume, he causes an I/O interruption and entry to the I/O interruption supervisor. If the UCB for that device contains a volume serial number, the I/O interruption supervisor sets a flag in the UCB for the device to indicate that volume verification is to be performed. The next time there is a request for activity on the device, the I/O supervisor, having checked the flag, schedules module IGE0025E. When IGE0025E gains control, it checks the flag in the UCB to determine if volume verification is required. If it is, control is transferred to module IGE0125E, the first module of the two–module volume verification routine.

Module IGE0125E tests if the UCB volume serial number is zeros or if the data management bit is set. If so, an SVC 15 instruction is issued to execute the user's channel program. If, however, there is a volume serial number in the UCB and the mount bit is not on, module IGE0125E constructs a channel program to read the volume label for the mounted volume and issues an SVC 15 instruction to cause the channel program to be executed. When it receives control a second time, after the volume label has been read, module IGE0125E matches the volume serial number of the mounted volume against the serial number in the UCB for the device. When the serial numbers agree, IGE0125E uses an SVC 15 instruction to cause the originally requested activity to be performed. If the volume serial numbers do not agree, or if the channel program was terminated in error IGE0125E invokes the second module of the Volume Verification routine IGE0225E. The second module issues a demount message for the mounted volume and a mount message for the volume whose serial number appears in the UCB.

If an I/O error occurs during reading of the volume label, 10 retries are attempted. If the condition cannot be corrected, IGE0125E invokes IGE0225E to issue an error message.

Appendix E: Dynamic Device Reconfiguration

In systems with the dynamic device reconfiguration option, a volume mounted and in use on one device can be removed and taken to another device where the activity on the volume will be resumed. Volumes can be moved at the request of an operator or, when there is a permanent I/O error, at the request of the system. Such moves can be made without restarting a job to cause device reallocation by job management routines, because I/O supervisor dynamic device reconfiguration (DDR) routines effectively reallocate by exchanging the device–dependent information in the unit control blocks of the two already allocated devices. The affected devices may be contained in different logical channels, because DDR routines also transfer the request queue elements for any queued requests for the devices to the correct logical channel queues.

The routines that perform dynamic device reconfiguration are shown in Figure 52.

Both the DDR SWAP Command Processor routine and the DDR Central routine perform preliminary work that includes checking the validity of the devices involved in the exchange and making sure they are eligible for the exchange. Either routine then posts a DDR event control block, causing a high–priority DDR TCB to be made ready by the supervisor. In dispatching the DDR task, the supervisor's Dispatcher routine gives control to the DDR Wait routine, which issues an SVC 85 instruction to cause entry to the DDR SVC Router routine. Depending upon the type of request, the DDR SVC Router routine gives control to one of three main DDR routines.

The Operator–Initiated DDR routine, System–Initiated DDR routine, and the DDR Tape Reposition routine direct any input/output activity needed for the volume exchange, find devices for volumes being moved after permanent I/O errors, and perform the exchange of UCB information. They do so indirectly, however, by setting switches to indicate what is to be done and then issuing SVC 15 instructions. The SVC 15 instructions cause entry, via the Error EXCP routine, to the DDR channel end or abnormal end appendages. The appendages check the switches and use the dynamic device reconfiguration vector table (Table 39) to route control to the resident I/O supervisor routines where the needed functions are performed.

Optionally, dynamic device reconfiguration can be specified for system residence devices. When this is the case, separate routines are used (Figure 52), but the logic is basically similar to that used for non–system–residence devices.

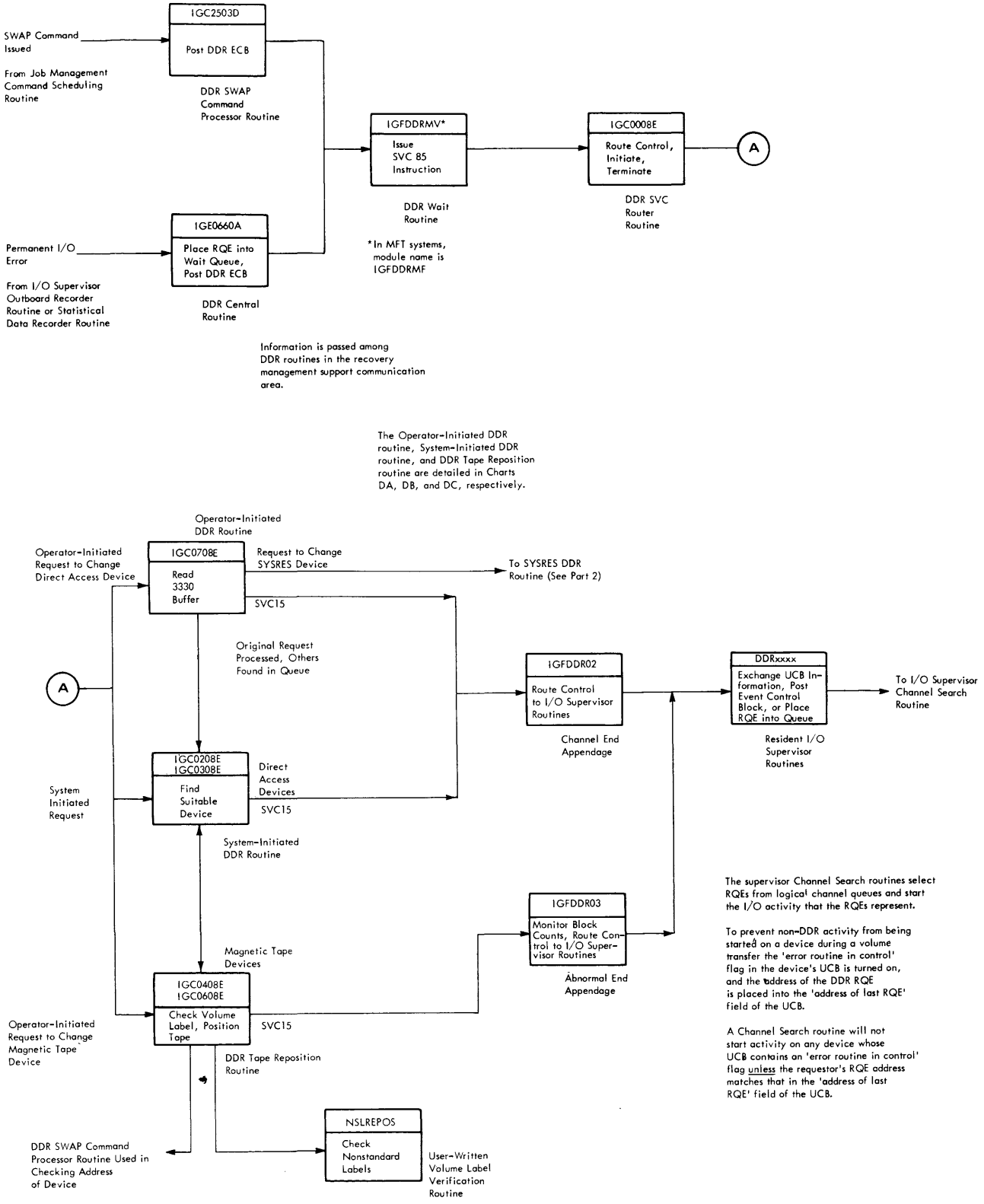


Figure 52 (Part 1 of 2). Performing Dynamic Device Reconfiguration

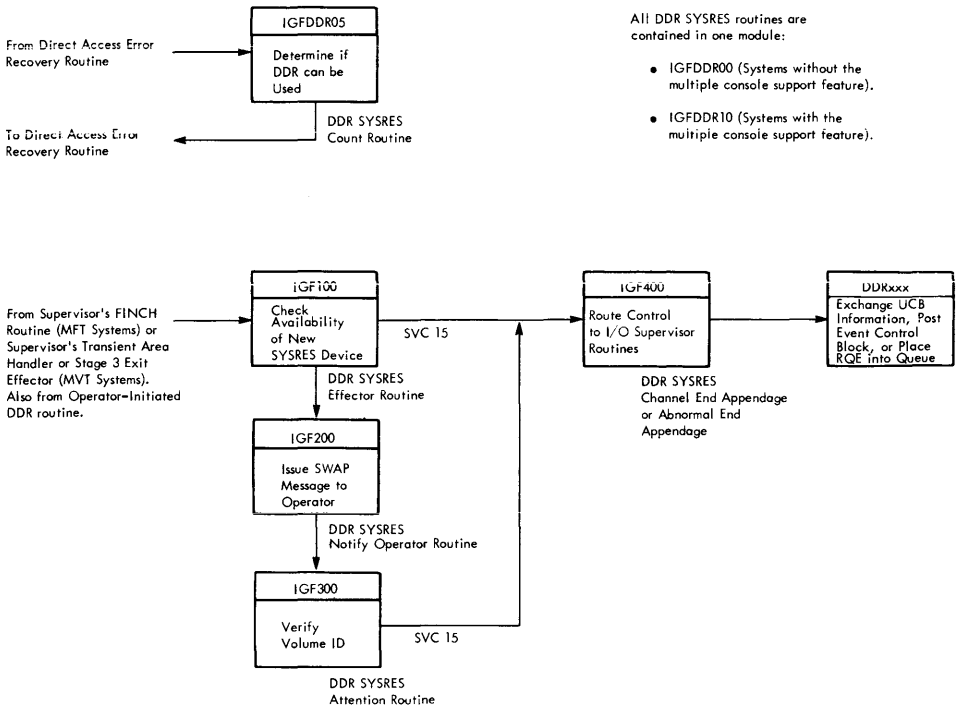


Figure 52 (Part 2 of 2). Performing Dynamic Device Reconfiguration

Table 39. Dynamic Device Reconfiguration Vector Table

Offset	Vector	Description
0		Address of dynamic device reconfiguration (DDR) wait queue.
4	DDRXCPWC	Re–EXCP with control of UCB. The RQE representing the DDR activity is placed into a logical channel queue, and other activity scheduled for the I/O device is prevented from starting. The DDR activity will be the first to be performed on the device. This vector is taken when a sequence of related I/O operations is in progress, as happens during repositioning of magnetic tape volumes.
8	DDRXCPNC	Re–EXCP without control of UCB. The RQE representing the DDR activity is placed into a logical channel queue, where it will be processed in turn.
12	DDRPSTNC	Post DDR without control of UCB. The requestor's ECB is posted and non–DDR activity is permitted to resume on the I/O device.
16	DDRPSTWC	Post DDR with control of UCB. The requestor's ECB is posted but non–DDR activity is prevented from starting on the I/O device. This vector is taken when one of a sequence of related I/O operations is completed (see DDRXCPWC vector).
20	DDRRETRY	Retry user after swap. The requestor's RQE is placed into a logical channel queue and other activity scheduled for the I/O device is prevented from starting. The requestor's activity will be the first to be performed on the device. This vector is taken when a volume has been changed to a second device and activity can be resumed on the new device.
24	DDRSWAP	Swap UCB information. The information in the UCB of one device is exchanged with the information in the UCB of another device. If the devices are not contained in the same logical channel, the RQEs representing requests for the devices are moved to the correct logical channels.
28	DDRCANCL	DDR request cancelled by operator. The RQE is removed from the wait queue and non–DDR activity is permitted to resume on the device. This vector is taken when the operator cancels a request to move a volume to another device.
32	DDRSRCAN	Cancel SYSRES–DDR request. The DDR RQE is removed from the logical channel queue.
36	DDRXCPSR	Retry SYSRES–DDR request after CC3. The UCBASK flag is set to indicate that the seek is complete. Other activity scheduled for the I/O device is prevented from starting.

Appendix F: Multiprocessing Extensions

The I/O supervisor is extended to implement multiprocessing if the M65MP option is selected at system generation. In multiprocessing, I/O devices can be accessible from each CPU through its own channels. If the CPU originating an I/O operation finds that its own channel is not available, it tests the availability of the corresponding channel of the other CPU (all channel–control unit–device addresses are the same for both CPUs). If the other CPU's channel is free, the originating CPU issues a "shoulder tap," causing an external interruption on the receiving CPU, which then initiates the I/O operation.

Tables and Work Areas

The unit control block (UCB) is extended by a full word for multiprocessing. (See Figure 45, Section 5.) The first byte of this word contains flags indicating which CPU started the current operation, if one is in progress. The extension is located "in front of" the UCB, but does not affect the displacement of other UCB fields. It is addressed by subtracting four from the UCB address.

Multiprocessing requires a new channel availability table in the prefixed storage area (PSA) of each CPU. (See Figure 16, Section 5.) A channel is marked unavailable in this table when:

- SIO is issued. This condition is cleared by the I/O interruption supervisor when the I/O operation completes.
- The nucleus initialization program determines that the channel is not operational or not included in the system.
- A VARY CHANNEL or VARY CPU command from the operator places the channel offline.

Extended Test Channel Logic

The Test Channel Common routine (XCPTCH) of the EXCP supervisor, under multiprocessing, makes a second test after finding that the requested physical channel is busy or not available. The Test Channel Common routine determines whether the corresponding channel of the other CPU is free by testing the channel availability table in the other CPU's prefixed storage area. If the table shows the channel is free, the Shoulder Tap Interface subroutine (XCPSTI) is given control. The subroutine sets a flag in the shoulder tap control word (STMASK), then branches to the Shoulder Tap routine (SHOLDTAP). The Shoulder Tap routine issues the Write Direct instruction to notify the other CPU. On return from the Shoulder Tap Interface subroutine, the I/O request element is queued to that channel, where the other CPU will find it after the I/O supervisor is unlocked by the requesting CPU (only one CPU executes the I/O supervisor at a time).

If neither CPU has an available channel, the request element is queued pending an interruption on either CPU.

Multiprocessing Subroutines

The following subroutines (with entry points in parentheses) are included in the I/O supervisor for the multiprocessing option:

- Shoulder Tap Interface—Sending. This subroutine sets a flag (in the shoulder tap control word in the PSA of the sending CPU) that indicates to the receiving CPU the channel for which an I/O operation is requested. The subroutine branches to a common system routine to execute the Write Direct instruction causing an external interruption on the other CPU.
- Shoulder Tap Interface—Receiving (IECISHTP). This routine receives control from the external FLIH after an I/O shoulder tap. It goes to the Channel Restart routine of the I/O interruption supervisor to start any request that has been placed on the channel queue by the sending CPU.
- VARY Interface (IECTIOMP and IECTCHMP). This subroutine issues the Test I/O and Test Channel instructions for the VARY command handling routines.
- Accessibility Test. This code is part of the test channel code (XCPTCH2). It tests the path accessibility flags (UCBCHM) of the UCB to ensure that a CPU about to start an I/O operation has access to the device. A CPU does not have access to the other CPU's console, and only one CPU has access to teleprocessing devices.
- Halt I/O Check (IECMPHIO). An I/O operation can be halted only by the CPU that initiated it. The PSA of each CPU contains a unique identifier that is placed in the UCB extension whenever SIO is issued for a device. When a Halt I/O is requested, this routine compares the identifier of the executing CPU to the identifier in the UCB extension. If they are the same, control is returned to the resident HIO routine. If different, flags are set in the shoulder tap control word in the UCB prefix segment, and a shoulder tap is performed.
- Shoulder Tap Halt I/O (HLTIOUNT). This routine receives control following a shoulder tap for Halt I/O. It searches the flags set by the Halt I/O Check routine, and passes control to the Resident HIO routine.

Appendix G: Program Check Recovery Subroutine (PCRS)

The Program Check Recovery Subroutine is assembled within I/O supervisor code for MFT, MVT, and M65MP systems. It acts in conjunction with the optional Program Check Handler to handle program check errors. The Program Check Subroutine works with the two sections of the Program Check Handler, Prolog and Abterm, to clean up the I/O supervisor control blocks and queues, and to terminate tasks. The Program Check Recovery Subroutine gains control from the Prolog section of the Program Check Handler when a program check error occurs in a task in the I/O supervisor, its appendages, or any routine branched to by the I/O supervisor. See Figure 53 for the general flow of control.

Preparations for processing a program check begin before an error occurs. The I/O supervisor, when it first gets control of an RQE, saves the address of the RQE in a special save area LTSVALSV. This allows the Program Check Recovery Subroutine to determine the interrupted task without depending on the passing of registers between the routines which gain control at a program check. The Program Check Recovery Subroutine dequeues the RQE from its logical channel queue by using the address at LTSVALSV, and sets the flags in UCBFL1 to zero, to clear them for the next RQE. Finally, the Program Check Recovery Subroutine determines the associated TCB for the task, checks its validity, and determines the proper ABEND code. Control passes from the Program Check Recovery Subroutine to the Abterm section of the Program Check Handler, which schedules the termination. The program check error handling ends when Abterm gives control back to to the I/O supervisor which places the RQE in the freelist and exits either to the SVC First Level Interruption Handler, if the program check occurred during an SVC 0, or to the Channel Restart, if the program check occurred during an SVC 15 or an I/O interruption. Now the I/O supervisor readies itself for a new RQE by zeroing out the special save area LTSVALSV.

Two exceptional conditions may arise: there may be no RQE associated with the program check, indicated by the save area LTSVALSV being zero, and a recurrence may occur in the Program Check Recovery Subroutine.

When there is no valid RQE, the Program Check Recovery Subroutine determines if an SVC 0 was in process, and if so, the task pointed to by the current TCB is abnormally terminated with the appropriate completion code (400 or 0F2). If there is no valid RQE and either an SVC 15 or interrupt is in process, abnormal termination is not attempted.

In case of recurrence, the Program Check Recovery Subroutine determines if there is a valid RQE, and if so, determines if there is a valid TCB. If a valid RQE and TCB can be determined, the task is abnormally terminated with the appropriate completion code. If there is no valid RQE or no valid TCB, processing is handled the same way as when there is no valid RQE.

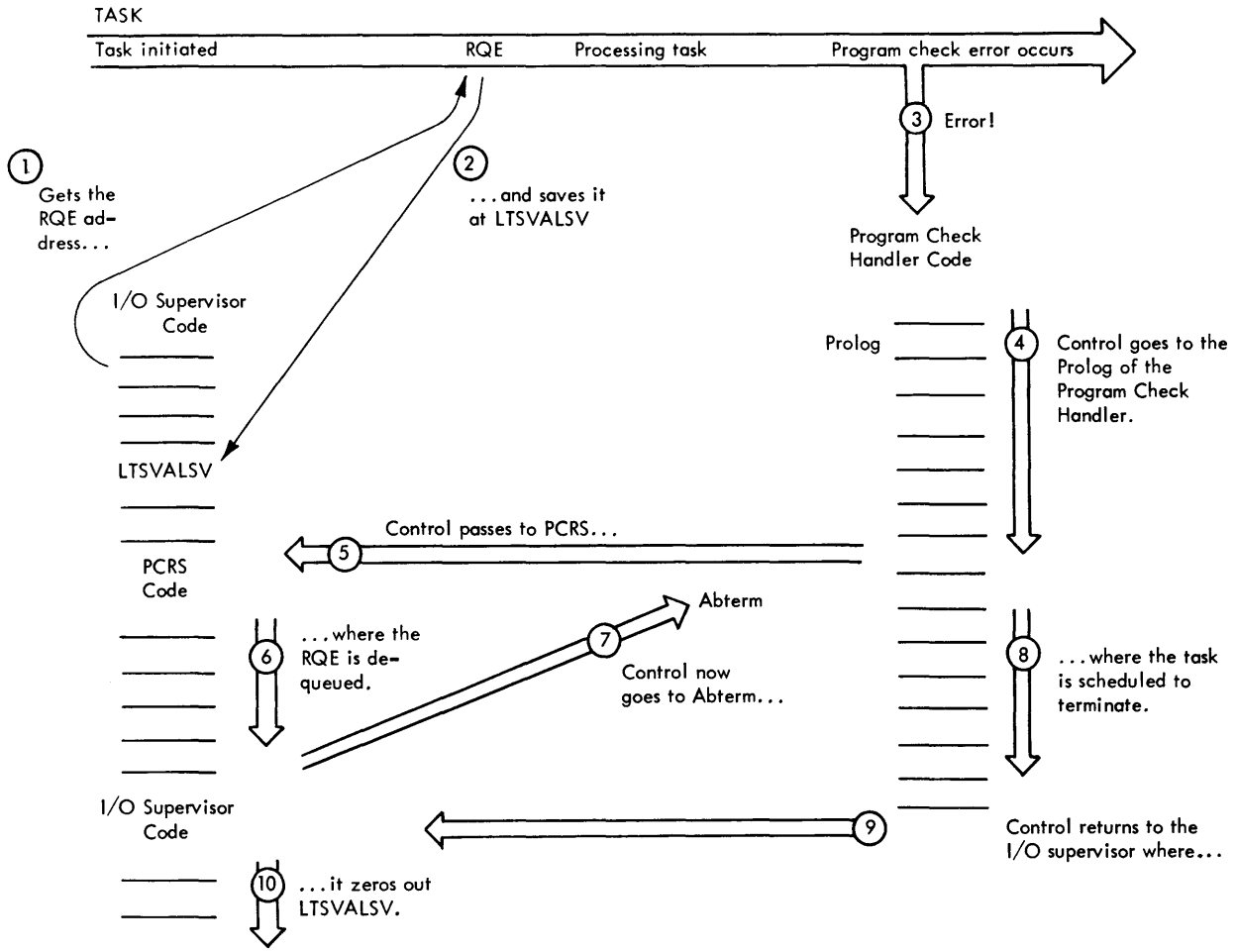


Figure 53. Operation of the Program Check Recovery Subroutine During a Program Check

Appendix H: Shared Direct–Access Storage Device

The Shared DASD option allows one direct–access device to be shared between two CPUs. The I/O supervisor must, therefore, provide special code to allow successful data transfer between the device and each CPU. Since a program seeking access to a shared–file device may require either exclusive use of the device or shared use of the device, the I/O supervisor uses two special command codes, RELEASE and RESERVE. RESERVE (X'B4') manipulates the swithcing device to allow exclusive use of the device by the CPU; RELEASE (X'94') manipulates the switching device to allow shared use of the device by the CPU. A program requiring exclusive use of the shared device must issue a RESERVE macro. This causes the RESERVE count in the UCB to be incremented. Once the RESERVE command is issued, the other CPU has no access to the device until a RELEASE command is issued to the device. The I/O supervisor issues a RELEASE command if the RESERVE count field is zero. This count field is decremented each time the user issues a DEQ macro.

Regardless of whether or not the user has issued a RESERVE macro, the I/O supervisor must also issue a RESERVE command with every stand–alone seek, regardless of the value in the RESERVE count fields. This prevents the other CPU from moving the access mechanism once it has been positioned for the first CPU. In the event the RESERVE count is zero, a RELEASE is issued with the data transfer channel program to free the device for the other CPU.

If a unit check or a channel error requires a sense operation to be done, a read home address and record zero channel program is chained to the sense command; if the RESERVE count in the UCB is zero, the sense command is changed to a RELEASE command—a special type of sense command. The home address and record zero data, read into the UCB's work area, is required by the device–dependent error recovery procedure. The RELEASE command frees the device for possible use by the second CPU during the first CPU's error recovery cycle.

If an active shared device is associated with a purged request, the UCB's HIO flag is set by the PURGE routine. This causes the I/O supervisor to issue a RELEASE to the device, if its RESERVE count is zero.

Appendix I: I/O Supervisor Messages

The I/O supervisor can write the following messages to the operator:

- IEA000A Intervention required
- IEA000I Uncorrectable input/output error
- IEA001I Inoperative path
- IEA604A Demount volume
- IEA605A Mount volume
- IEA606I Bad volume label
- IFB001I I/O error during SER
- IFB003I SER recording area full
- IFB002I Channel detected error
- IFB004I SER disk area format error

For complete descriptions of these messages, see the publication *OS Messages and Codes,* GC28-6631.

The first three messages shown above are handled similarly. When an I/O error routine determines that a message is needed, it invokes the I/O supervisor's Write-to-Operator routine, which composes the text of the message and issues an SVC 35 instruction. Actual writing of the message is performed by the system Write-to-Operator SVC routine.

The next three messages in the list are produced by the optional Volume Verification routine, which checks serial numbers of newly mounted volumes.

The last four messages in the list above are written by the System Environment Recording Message routine, which is invoked when one of the environment data recording routines cannot write into the SYS1.LOGREC data set.

Appendix J: I/O Supervisor—OLTEP Synchronizing Module–IECIOLTS

OLTEP requires the following special support from the I/O supervisor:

- Attention–interruption posting
- Device–end posting when device–end occurs separately from channel–end
- Return SIO condition codes when either of above functions is active
- Exclusive use of a channel by OLTEP
- Bypassing of the system channel programs for tape devices and direct access devices
- Specific exposure path selection for multiple exposure devices

The I/O supervisor maintains the module IECIOLTS which coordinates the I/O supervisor functions requested by OLTEP. The address of this routine is contained in the I/O supervisor–OLTEP vector table, IECOLTVT.

To indicate that OLTEP requires assistance from the I/O supervisor, the SVC 59 instruction sets a series of switches in the IECOLTSW field of IECOLTVT. The I/O supervisor exits from four places in its code to check these switches:

- It exits during the Test Channel routine.
- It exits during the Halt I/O routine.
- It exits during the Start I/O routine.
- It exits during the SIO module for multiple exposure devices.

If OLTEP indicates a channel function on a 2880 channel, control passes from the Test Channel routine in the I/O supervisor to the subroutine in IECIOLTS at label OLTCHN. Processing in that subroutine determines whether or not OLTEP has exclusive control of a channel.

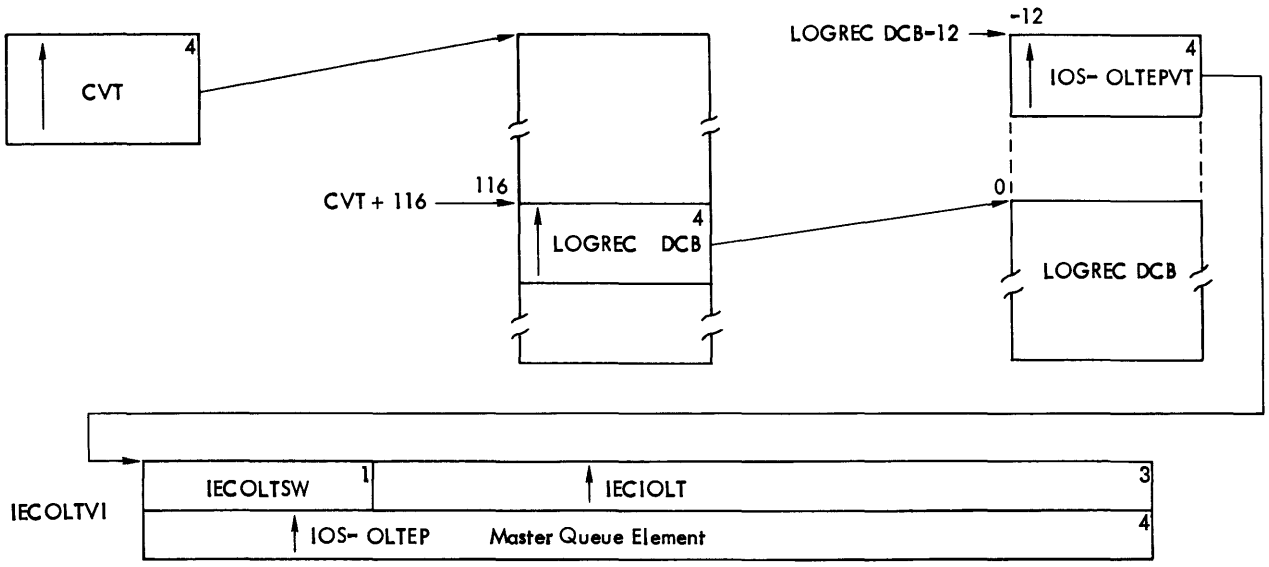
The SIO appendage in IECIOLTS at label SIOAPP is entered normally. This appendage checks the bypass function bit. If it is on, normal I/O channel programs are bypassed and OLTEP operations continue on that channel.

If OLTEP indicates either device–end or attention posting, control passes from the halt I/O routine in the I/O supervisor to the subroutine in IECIOLTS at label OLTHLT This subroutine determines if IOS may issue an HIO on the input device.

Special OLTEP multiple exposure device code in the I/O supervisor exits to IECIOLTS at label OLTEXP to select a specific–exposure access path for OLTEP.

More information about the routines and appendages in IECIOLTS can be found in *OS OLTEP Logic,* GY28–6651.

The I/O supervisor uses the addressing scheme shown in Figure 54 to gain access to IECOLTVT.



Byte	Bit		Bit checked by
1	1...	Channel function	Test channel routine in I/O supervisor
	.1..	Device-end posting	Halt I/O routine in I/O supervisor
	..1.	Attention posting	Halt I/O routine in I/O supervisor
	...1	Bypass function	SIO appendage in IECIOLTS
	.... 1...	Exposure function	Exposure selection routine in IECIOLTS

Figure 54. IECIOLTS Addressing Scheme and Bit Settings

Appendix K: Functionally Equivalent Devices

I/O Device	Equivalent Device	Description
2319 Disk Storage	2314 Disk Storage	The 2319 is specified as a 2314 in system generation. It is also specified as a 2314 in JCL. Any routines described in this publication as applicable to the 2314 also apply to the 2319.
3333 Disk Storage and Control	3330 Disk Storage	The 3333 is specified as a 3330 in system generation. It is also specified as a 3330 in JCL. Any routines described in this publication as applicable to the 3330 also apply to the 3333. See *Reference Manual for IBM 3333 Disk Storage and Control,* GA26-1615, for more information about the 3333.

Appendix L: List of Abbreviations

APR	alternate path retry
ASCII	American National Standard Code for Information Interchange
BSAM	basic sequential access method
BTAM	basic teleprocessing access method
CAW	channel address word
CC	condition code; chain command
CCC	channel control check
CCH	channel check handler
CCW	channel command word
CD	chain data
CEB	channel error block
CPU	central processing unit
CRC	cyclic redundancy check
CSW	channel status word
CUA	channel and unit address
DASD	direct access storage device
DCB	data control block
DDR	dynamic device reconfiguration
DEB	data extent block
DSCB	data set control block
EBCDIC	extended binary–coded–decimal interchange code
ECB	event control block
EOD	end of day
EOF	end of file
EOV	end of volume
ERG	error record gap
ERP	error recovery procedure
ERPIB	error recovery procedure interface block
EXCP	execute channel program
FIFO	first–in first–out
FLIH	first level interruption handler
HA	home address
HEX	hexadecimal
ICC	interface control check
ILC	instruction length code
I/O	input/output
IOB	input/output block
IOS	input/output supervisor
IPL	initial program loading
LCH	logical channel
MFT	multiprogramming with a fixed number of tasks
MVT	multiprogramming with a variable number of tasks
M65MP	Model 65 Multiprocessing
NIP	nucleus initialization program
NRZI	non-return-to-zero inverted recording
OBR	outboard recorder, outboard recording
OLTEP	online test executive program
PCI	program controlled interruption
PCP	primary control program
PCU	primary control unit

PLM	program logic manual
PL/I	Programming Language I
PSA	prefixed storage area
PSW	program status word
QSAM	queued sequential access method
QTAM	queued teleprocessing access method
RQE	request queue element
R0	record zero
SCU	secondary control unit
SER	system environment recording
SIO	start input/output
SLI	suppress length indication
SMF	system management facilities
SVC	supervisor call
TCB	task control block
TCH	test channel
TIC	transfer in channel
TIE	track in error

Appendix M: Glossary

The following terms are defined as they are used in this book. If you do not find the term you are looking for, refer to the index or to the *IBM Data Processing Glossary,* GC20–1699.

access arm: A part of a disk storage unit that is used to hold one or more reading and writing heads.

access mechanism: A group of access arms that move together as a unit.

access method: Any of the data management techniques available to the user for transferring data between main storage and an input/output device.

alternate track: For direct access devices, a track designated to contain data in place of a defective primary track.

asynchronous: Without regular time relationship; unexpected or unpredictable with respect to the execution of a program's instructions.

auxiliary storage: Data storage other than main storage.

basic access method: Any access method in which each input/output statement causes a corresponding machine input/output operation to occur. (The primary macro instructions used are READ and WRITE.) Contrast with *queued access method.*

basic telecommunications access method (BTAM): A basic access method that permits a READ/WRITE communication with remote devices.

burst mode: A means of transferring data to or from a particular I/O device on either the multiplexor or selector channel. All channel controls are monopolized for the duration of data transfer.

bus lines: The lines of communication between a channel and a control unit. Bus–out lines carry information from a channel to a control unit; bus–in lines carry information from a control unit to a channel.

byte mode: See *multiplex mode.*

CAW (channel address word): A word in main storage at location 72 that specifies the location in main storage where a channel program begins.

CCW (channel command word): A double word at the location in main storage specified by the CAW. One or more CCWs make up the channel program that directs channel operations.

central processing unit (CPU): The unit of a computing system that contains the circuits that control and perform the execution of instructions.

channel: A hardware device that connects the CPU and main storage with the I/O control units.

channel command: An instruction that directs a channel, control unit, or device to perform an operation or set of operations. A channel command (an 8–byte data field in main storage) consists of a command code, a main storage address, a flag field, and a count.

channel program: One or more channel command words (CCWs) that control(s) a specific sequence of channel operations. Execution of the sequence is initiated by a single Start I/O instruction.

compile: To prepare a machine language program from a computer program written in a high–level source language by generating more than one machine instruction for each symbolic statement (sometimes with an intermediate generation of assembler language instructions).

compiler: A program that compiles.

control block: A storage area through which a particular type of information required for control of the operating system is communicated among its parts.

CPU: (See central processing unit.)

CSW (channel status word): A double word in main storage at location 64 that provides information about the termination of an input/output operation.

cylinder: The tracks of a direct access device that are accessible with one positioning of the access mechanism.

DASD: A direct–access storage device.

data control block (DCB): A control block used by access method routines in storing and retrieving data.

data set control block (DSCB): A data set label for a data set in direct access storage.

DCB: See data control block.

direct access: Retrieval or storage of data by a reference to its location on a volume, rather than relative to the previously retrieved or stored data.

direct–access device: A device in which the access time is effectively independent of the location of the data.

disabled (masked): A state of the CPU that prevents the occurrence of certain types of interruptions.

disk storage: A storage device that uses magnetic recording on rotating disks.

dispatcher: In the Operating System, a supervisor routine of the control program. The dispatcher passes control to the next executable task by issuing a Load PSW instruction that specifies an old PSW, stored either in a request block or in a permanent location in main storage.

dispatching: In multitasking, the passing of control to the current executable routine of the next task to be activated. (This routine may be the same one that was previously being executed.)

drum storage: A direct access storage device which uses a rotating cylinder on which data is recorded magnetically. A type of addressable storage associated with some computers.

event: An occurrence of significance to a task; typically, the completion of an asynchronous operation, such as input/output.

event control block (ECB): A control block used to represent the status of an event.

extent: An area of storage on a direct access device. A specific extent is delimited by a starting track address and an ending track address; it always consists of one or more full tracks.

freelist: The chain of all free, or available, request queue elements.

immediate I/O operations: Those I/O operations for which an I/O device signals the channel–end condition immediately upon receipt of the command code. No transfer of data takes place when immediate operations are performed.

inboard record: A record on the SYS1.LOGREC data set containing information about a channel failure.

indexed sequential organization: A data organization that allows access to any record without reading the preceding record or maintaining a separate record that gives the position of the desired record. The locating of each record in the data set depends on the contents of a key portion of the record.

initial program loading (IPL): As applied to the operating system, the initialization procedure which loads the nucleus and begins operations.

innerrecord gap: On a storage medium, an area used to indicate the end of a record.

input–output error: A general term used to denote any of the conditions that would preclude normal (or successful) completion of an input/output operation. Input–output errors are generally a result of malfunctioning input/output devices.

intercepted I/O request: A request for I/O activity on which processing has been suspended so that an I/O error routine could be used to process an error that occurred after channel end for the last activity on the needed device.

IPL: See *initial program loading.*

logical channel: The set of all physical channels by which a device may be reached.

logical channel queue: A queue into which request elements are placed when I/O activity cannot be started immediately. There is one logical channel queue for each logical channel.

logical channel word: An eight–byte data area that contains the addresses of the first and last request elements in a logical channel queue. There is one logical channel word for each logical channel.

logical channel word table: A term used when referring collectively to all of the logical channel words in a system.

logout: Twenty–four bytes of status information which are sent to main storage locations 30410 to 32710 by a channel following a channel control check.

macro instruction: A general term used to collectively describe a macro instruction statement, the corresponding macro instruction definition, the resulting assembler language statements, and the machine language instructions and other data produced from the assembler language statements; loosely, any one of these representations of a machine language instruction sequence. A shorthand form of coding.

multiplex mode: A means of transferring records to or from low–speed I/O devices on the multiplexor channel, by interleaving bytes of data. The multiplexor channel sustains simultaneous I/O operations on several subchannels. Bytes of data are interleaved and then routed to or from the selected I/O devices or to and from the desired locations in main storage. Multiplex mode is sometimes referred to as byte mode.

multiplexor channel: A channel designed to operate with a number of I/O devices simultaneously on a byte basis. That is, several I/O devices can be transferring records over the multiplexor channel, time–sharing it on a byte basis.

nonshared subchannel: A subchannel that can service only one I/O device.

nucleus: That portion of the control program that is loaded into the fixed area of main storage from SYS1.NUCLEUS at IPL time and is never overlaid by another part of the operating system.

nucleus initialization program (NIP): The program that initializes the resident control program. It allows last minute changes to certain options specified during system generation. The operator makes these changes through the console.

outboard record: A record on the SYS1.LOGREC data set containing information about an I/O device failure.

permanent error: An input/output error that either cannot be corrected or remains uncorrected after error recovery procedures have been used.

prefixed storage area: A 4096–byte main storage area in each of the two CPUs of Model 65 Multiprocessing systems, used for storing CPU–related information.

primary track: For direct–access devices, the original track on which data could be stored.

processing program: Any program capable of operating in the problem program mode. This includes IBM–distributed language processors, application programs, service and utility programs, and user-written programs.

program status word: A double word in main storage used to control the order in which instructions are executed, and to hold and indicate the status of the system in relation to a particular program.

queued access method: An access method that automatically governs the movement of data between the program using the access method and input/output devices. (The macro instructions used are GET and PUT.)

related I/O request: A request for I/O activity that is not to be honored unless the preceding activity for the effected data set has been completed successfully.

routine, subroutine: Sequences of instructions that perform distinguishable operations. The term subroutine is most often used where a hierarchy exists, as when there is a need to distinguish between a major operation (performed by a routine) and a subordinate operation (performed by a subroutine).

shared subchannel: A subchannel that can service more than one I/O device.

subchannel: The channel facilities required to sustain an I/O operation. Selector channels have one subchannel; multiplexor channels have multiple subchannels.

supervisor call (SVC): An instruction which causes an SVC interruption in the hardware to give control to a control program routine (called an SVC routine) for some specific action, such as reassigning parts of main storage or retrieving data from an I/O device.

SVC routine: A control program routine that performs or initiates a control program service specified by a supervisor call.

system data sets: The data sets that make up the Operating System.

system macro instruction: A predefined macro instruction that provides access to operating system facilities.

system output unit: An output device, shared by all jobs, onto which specified output data is transcribed.

SYS1.LOGREC: The system data set used to record statistical data about machine malfunctions.

SYS1.SVCLIB: The partitioned system data set that contains the nonresident SVC routines, nonresident error–handling routines, and access method routines.

task control block (TCB): The control block containing control information related to a task.

track (direct–access devices): The portion of a direct–access device recording surface available to a single read/write head at each access mechanism position.

track address: In direct access devices, an address made up of a cylinder number and a read–write head number. Every track of a direct–access device has a unique track address.

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OS I/O SUPERVISOR LOGIC

This technical newsletter, a part of Release 21.7 of OS, provides replacement pages for the subject publication. These replacement pages remain in effect for subsequent releases unless specifically altered. Pages to be inserted and removed are:

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Each technical change is marked by a vertical line to the left of the change.

Summary of Amendments

- A new module, IGX00015, has been added to IOS. This module is used by the Task Termination routine to insure that a task does not leave outstanding I/O requests.
- IOS now fully supports the 3333 Disk Storage and Control. The 3333 is functionally equivalent to the 3330 Disk Storage. Any reference to the 3330 also apply to the 3333.

Note: Please file this cover letter at the back of the publication to provide a record of changes.

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