Impact of Processing Technology on DRAM Sense Amplifier Design

by

Jeffrey Carl Gealow

Submitted to the Department of Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
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Abstract

Sense amplifier design is critical to DRAM performance. As DRAM chip capacity has increased, different sensing schemes have been employed. The purpose of this work is to explain impacts of processing technology on DRAM sense amplifier design and to identify design strategies suitable for 64M DRAM sense amplifiers. DRAM performance and processing technology evolution are reviewed. Sense amplifier operation is examined analytically. Sense amplifiers used in 4K and higher density DRAMs are studied. 64M DRAM processing technology features and performance specifications are projected. Finally, alternative design approaches for 64M DRAM sense amplifiers are compared and evaluated.

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Chapter 1

Introduction

Since the early 1970's, high density dynamic random access memory (DRAM) chips have been based on the one-transistor cell array, patented by Dennard in 1968 [1]. As shown in Figure 1.1, each cell comprises a single access transistor and a single storage capacitor. Binary information is represented by the state of the storage capacitors. Each cell holds a single bit. Typically, a high stored potential represents a '1' and a low stored potential represents a '0'. Cells must be periodically refreshed to prevent loss of data due to charge leakage.

Wordlines connect the access transistor gates of each cell row. Activating a wordline turns on the access transistors, connecting the cell storage capacitors to bitlines. Data may then be read from or written to the cells through the bitlines. Each bitline serves a column of cells. Deactivating the wordline isolates the storage capacitors from the bitlines.

Before activating a wordline to read or refresh a cell row, the bitlines are precharged to a common potential. Activation of the wordline causes charge sharing to occur between cell storage capacitors and bitlines. Small signals reflecting cell states are produced on each bitline. The signals must be amplified, and the original state of the storage capacitors must be restored. These functions are performed by sense amplifiers.

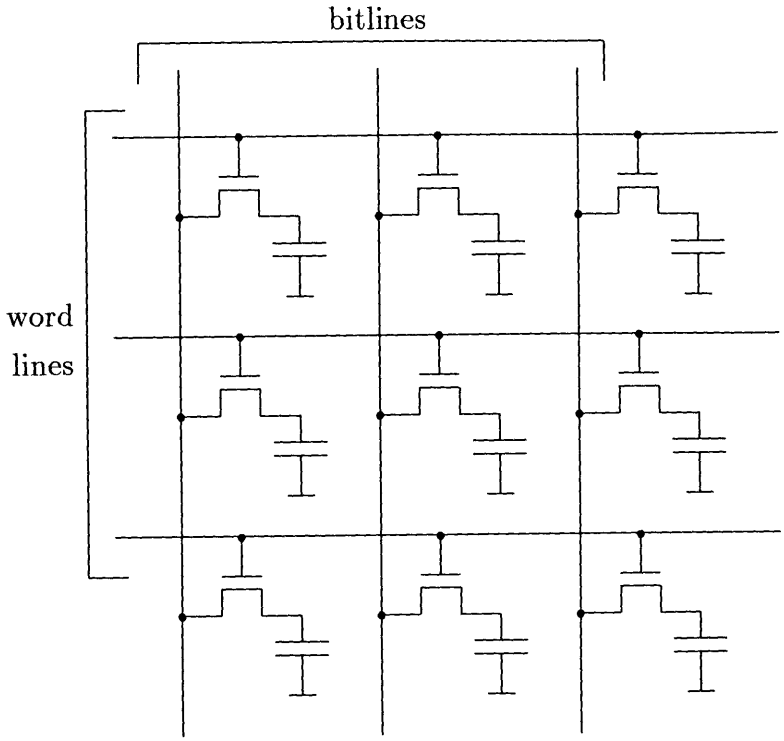

Figure 1.1: DRAM Array

Sense amplifier design is critical to DRAM performance. Key DRAM characteristics, including speed, power dissipation, and error rate depend on sense amplifier features. The goal of this research is to identify the impact of processing technology parameters on sense amplifier design and to propose designs suitable for 64 Megabit DRAMs.

1.1 Divided Bitline Architecture

The 2K DRAM introduced by Cohen *et al.* in 1971 [2] was the first published DRAM using a single-transistor cell. This chip, and a few early 4K DRAMs, employed continuous bitlines and single-ended sense amplifiers. Singe-ended sensing involved either precharging the bitlines to the switching threshold of an inverter [3],[4], or sampling the bitline voltages just before activating the wordline [5]. The former approach incurs static power dissipation through the amplifier during the precharge interval. The latter approach requires several sensitive clock signals and is susceptible to common mode noise introduced after bitline voltage sampling.

In 1972, Stein *et al.* proposed the divided bitline architecture [6],[7]. As shown in Figure 1.2, each bitline is split into two matched segments, one on each side of the sense amplifier. Differential sense amplifiers are employed, avoiding many of the difficulties of single-ended sensing. Using this architecture, Hoffman and Kalter achieved quantity production on an 8K DRAM in 1973 [8],[9]. 16K and higher density DRAMs have been based on the divided bitline architecture.

Read and refresh cycles of DRAMs using the divided bitline architecture proceed as follows. First, the bitline segments are precharged to a common potential, V_{PC}. Next, the selected wordline is activated. Bitline segments on the same side of the sense amplifiers as the wordline are connected to cell storage capacitors. Assuming the activated wordline is driven sufficiently high, the potentials of the selected cell storage

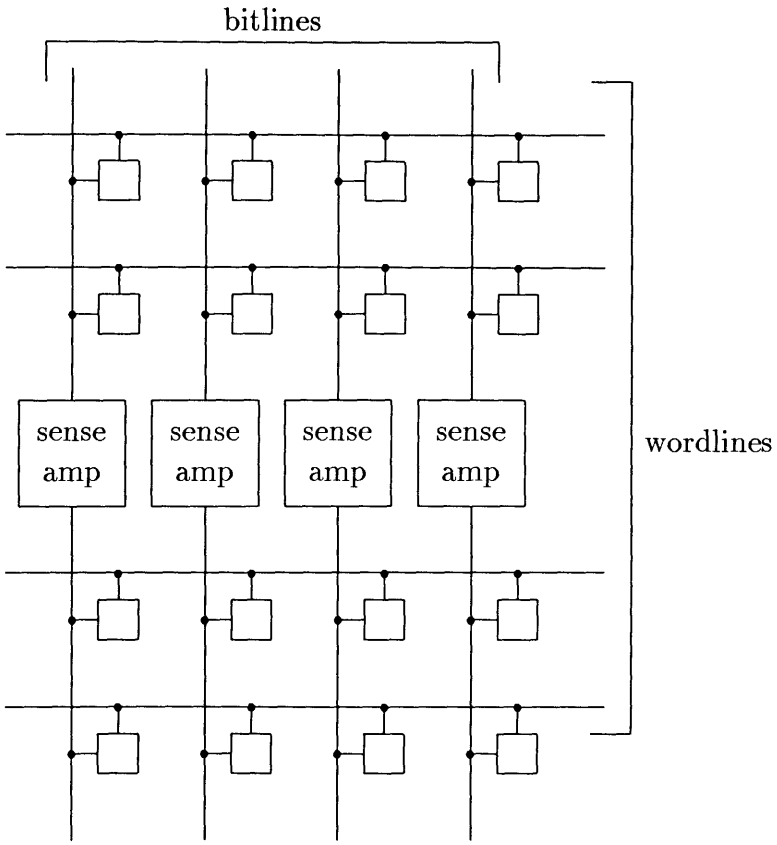

Figure 1.2: Divided Bit Line Architecture

capacitors and their corresponding bitline segments are equalized. The potential of bitline segments connected to cells storing a '1' is

$$V_{BL1} = \frac{V_{PC}C_{BT} + V_{S1}C_S}{C_{BT} + C_S}, \tag{1.1}$$

while the potential of bitline segments connected to cells storing a '0' is

$$V_{BL0} = \frac{V_{PC}C_{BT} + V_{S0}C_S}{C_{BT} + C_S}. \tag{1.2}$$

V_{S1} and V_{S0} are the stored '1' and '0' potentials. Commonly $V_{S1} = V_{DD}$ and $V_{S0} = 0$ (ground). C_{BT} is the total effective bitline segment capacitance, excluding storage cell capacitance. C_S is the storage cell capacitance.

On the opposite bitline segments, a reference potential, midway between V_{BL1} and V_{BL0}, must be present. This can be accomplished either by setting the precharge potential, V_{PC}, midway between V_{S1} and V_{S0} or by employing dummy cells as suggested by Stein *et al.* [6], [7]. The sense circuitry amplifies the potential differences between the two bitline segments in each column and recharges the storage capacitors to full '1' and '0' potentials.

The initial sense amplifier signal magnitude is limited by the ratio of the bitline capacitance to the storage cell capacitance. The raw signal developed across the sense amplifiers is

$$\Delta V = \frac{V_{BL1} - V_{BL0}}{2} = \frac{1}{2}\frac{(V_{S1} - V_{S0})}{(C_{BT}/C_S + 1)}. \tag{1.3}$$

Typically the transfer ratio, C_{BT}/C_S, is in the 5-20 range. As the number of cells per bitline increases, maintaining a constant transfer ratio requires decreasing the bitline capacitance per bit and/or increasing the storage cell capacitance.

1.1.1 Signal Loss Due to Incomplete Charge Transfer

The above analysis assumed the activated wordline is driven sufficiently high to equalize the potentials of the selected cell storage capacitors and their corresponding bit-

line segments. In some DRAM designs, this assumption is invalid. For example, if $V_{S0} = 0$, $V_{PC} = V_{DD}$ and the wordline is not driven above V_{DD} during signal development, n-channel transfer devices accessing a stored '0' will shut off when the storage cell potential reaches $V_{DD} - V_T$, where V_T is the transfer device threshold voltage.

Equations (1.1), (1.2), and (1.3) can be modified to encompass cases involving incomplete equalization. After signal development is complete, the potential of bitline segments connected to cells storing a '1' is

$$V_{BL1} = \frac{V_{PC}C_{BT} + V_{S1}C_S - (V_{C1} - V_{BL1})C_S}{C_{BT} + C_S}, \tag{1.4}$$

where V_{C1} is the final potential of the '1' storage cells. The potential of bitline segments connected to cells storing a '0' is

$$V_{BL0} = \frac{V_{PC}C_{BT} + V_{S0}C_S - (V_{C0} - V_{BL0})C_S}{C_{BT} + C_S}, \tag{1.5}$$

where V_{C0} is the final potential of the '0' storage cells. Thus, the raw signal developed across the sense amplifiers is

$$\Delta V = \frac{1}{2}\frac{(V_{S1} - V_{S0}) - (V_{C1} - V_{BL1}) - (V_{BL0} - V_{C0})}{(C_{BT}/C_S + 1)}. \tag{1.6}$$

1.1.2 Dummy Storage Cells

Unless the bitline precharge potential is midway between V_{BL1} and V_{BL0}, dummy cells must be used. A single row of dummy cells is placed on each side of the sense amplifier. The basic structure of the dummy cells is identical to the normal storage cell structure. Dummy wordlines connect the access transistor gates of each dummy cell row. The dummy storage capacitors are precharged to a common potential. When the selected wordline is activated, the dummy wordline on the opposite side of the sense amplifier is also activated.

The dummy storage capacitor precharge potential and capacitance are designed to produce the proper bitline segment reference potential. Two schemes are common. In the first scheme, the dummy cell capacitance is equal to the normal storage cell capacitance. The dummy storage capacitors are precharged to a potential midway between V_{S1} and V_{S0}. In the other arrangement, the bitlines are precharged to V_{S1}. The dummy cell capacitors, with about one-half the capacitance of the normal storage cell capacitors, are precharged to V_{S0}. When the wordline and dummy wordline are activated, the potentials of bitline segments connected to cells storing a '1' remain at V_{S1}. The potentials of segments connected to cells storing a '0' drop to $V_{S1}C_{BT}/(C_{BT} + C_S)$. The potentials of segments connected to dummy cells drop to $V_{S1}C_{BT}/2(C_{BT} + C_S)$.

The first scheme allows use of any bitline precharge potential but requires precharging the dummy storage cell capacitors to an intermediate potential. A dummy cell precharge voltage generator may be needed. The second scheme constrains the bitline precharge potential and requires a unique dummy storage cell capacitance. It also creates an imbalance in the bitline segment node capacitances during sensing.

1.2 Noise Sources

A wide variety of phenomena, commonly referred to as "noise sources," may degrade signals presented to the sense amplifiers. Equations (1.3) and (1.6) do not account for these phenomena. Yet the noises produced are often of such magnitude that they may not be safely neglected.

Bitline, storage cell, and dummy cell capacitance variations alter the bitline potentials produced by signal development. Process tolerances and mismatches must both be considered. Capacitances may vary both globally, from chip to chip, and locally, from cell to cell or bitline to bitline.

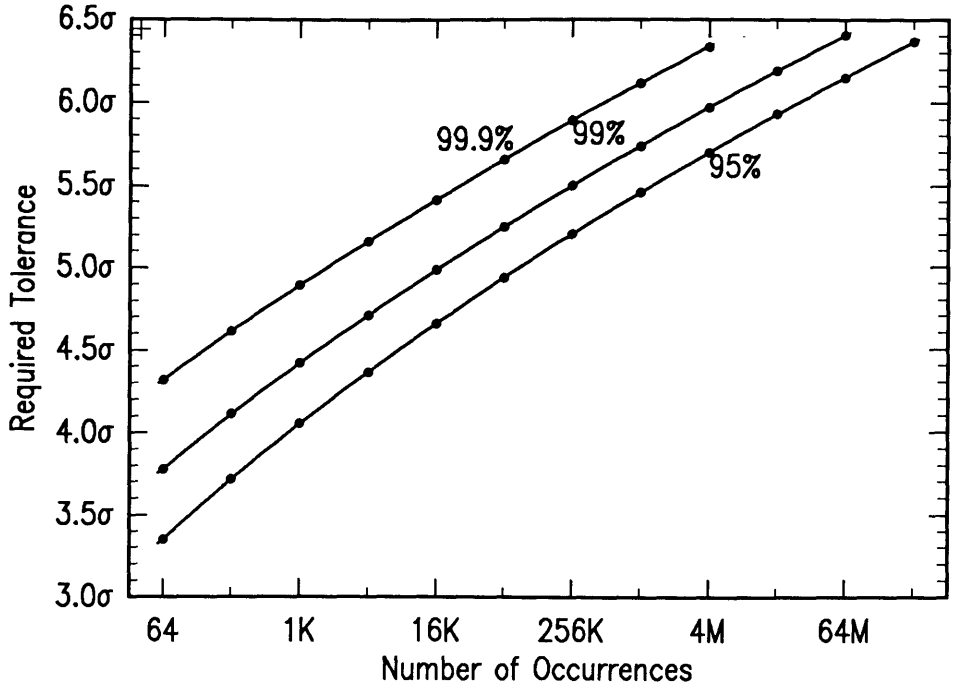

Figure 1.3: Required Tolerance versus Number of Occurrences. 95%, 99%, and 99.9% Chances of All Occurrences Falling Within Tolerance.

As DRAM chip capacity grows, the number of cell and sense amplifier related structures increases. As a result, to maintain constant yield, process tolerances related to these structures must be increased. Figure 1.3 illustrates this relationship. A Gaussian distribution is assumed.

Voltages which are ideally constant may vary, resulting in signal loss. Fluctuations in the storage capacitor plate potential may result from supply voltage skew, wordline-plate coupling, or bitline-plate coupling. Stored '0' and '1' and dummy storage capacitor potential variations may be caused by incomplete charge storage, supply voltage skew, storage capacitor leakage, or subthreshold transfer device leakage. If a dummy storage capacitor precharge voltage generator is used, non-ideal operation of the voltage generator may also cause precharge voltage variations. Local differences in bitline segment precharge potentials may result from incomplete precharge, supply voltage skew, or bitline charge leakage. Global precharge potential variations,

important in designs not employing dummy cells, may be caused by supply voltage skew or, if a bitline precharge voltage generator is employed, non-ideal operation of the voltage generator.

Injection of minority carriers into the bulk region of the array may cause signal loss. Charge injection can occur as a result of alpha particle radiation or chip input undershoot or overshoot. Injected charge collected by cell storage capacitors may alter the stored potentials. In addition, during signal development injected charge may be collected by the bitline segments, altering the bitline potentials.

Electrical coupling within the array affects signal development. Changes in wordline potential can result in storage cell state-dependent changes in bitline and storage capacitor potentials. Bitline to bitline coupling results in pattern-dependent effective bitline capacitance changes. Bitline potential changes during signal development may induce changes in wordline, bulk, or plate potentials. These changes may, in turn, alter the bitline potentials.

1.3 Folded Bitline Architecture

In the conventional divided bitline arrangement shown in Figure 1.2, matched bitline segments extend from opposite sides of the sense amplifiers. This arrangement is used in most 16K DRAMs. The folded bitline architecture, shown in Figure 1.4, is used in many 64K and higher density DRAMs. It requires a more complex cell structure, but offers several advantages over the conventional open bitline architecture.

With open bitlines, differential column I/O sensing requires placement of column decode circuits between the sense amplifiers and the array. Use of folded bitlines allows placement of column decode circuitry at the ends of the bitlines, reducing bitline capacitance and eliminating coupling between the bitlines and the column address lines [10], [11], [12].

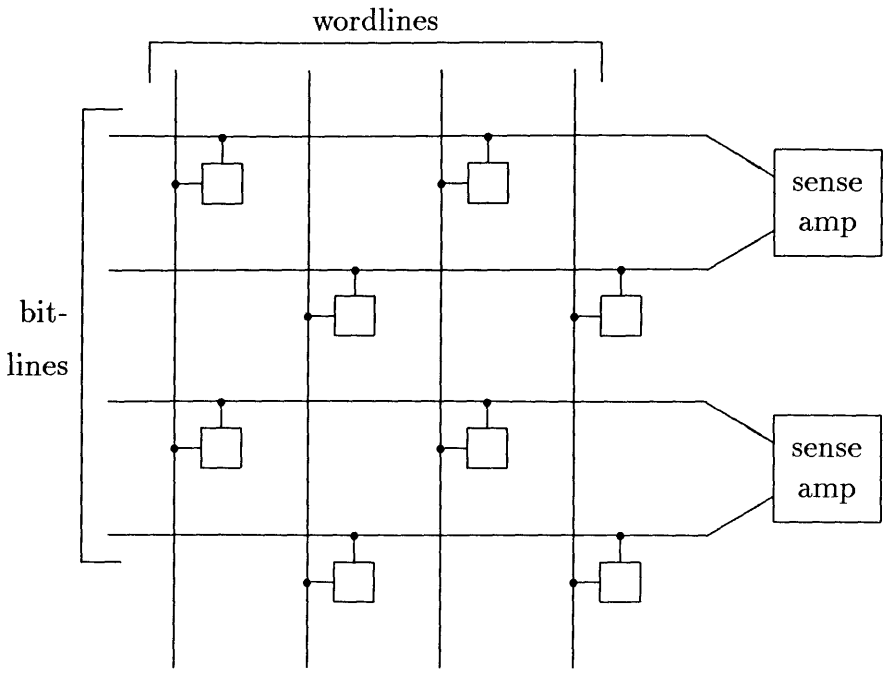

Figure 1.4: Folded Bit Line Architecture

The folded bitline architecture reduces the sense amplifier pitch constraint from one bitline segment pitch to two bitline segment pitches. In many cases, this may allow more efficient sense amplifier layout [13].

Employing folded bitlines may help improve noise rejection. Some mechanisms which introduce differential mode noise in open bitline designs may produce only common mode noise in folded bitline configurations [14], [15].

The folded bitline architecture reduces the physical distance between paired bitline segments. Thus folded arrays are, in general, less sensitive to spatial bulk and plate potential variations. In addition, during signal development, roughly equal amounts of injected charge may be collected by neighboring bitline segments. Thus, charge injection during signal development may produce smaller changes in potential between paired bitline segments in a folded bitline arrangement.

In open bitline configurations, the average bitline potential change in each storage cell array is highly dependent on the stored pattern. In most folded configurations, the average bitline potential change is independent of the stored pattern. Thus, in a folded bitline architecture, differential plate, bulk, and wordline potential changes resulting from coupling to bitlines may be reduced.

1.4 Balanced Flip-Flop Sense Amplifier

The differential sense amplifiers used in modern DRAMs are variations of the balanced flip-flop sense amplifier presented by Stein *et al.* in 1972 [6],[7]. The circuit is shown in Figure 1.5. During the precharge period ϕ_1 and ϕ_2 are high, $\overline{\phi_2}$ is low, and both dummy wordlines are activated. The bitline and dummy cell potentials are set to the switching threshold of the flip-flop. After the precharge voltage is established, ϕ_1 and ϕ_2 go low, $\overline{\phi_2}$ goes high, and the dummy wordlines are deactivated. When a wordline is activated, the dummy wordline on the opposite side of the sense amplifier is also activated. Offset introduced by capacitive coupling of bitline segments to the active wordline is compensated by coupling of the opposite segments to the active dummy wordline. Driving ϕ_2 high and $\overline{\phi_2}$ low activates the flip-flop, initiating sense signal amplification. The lower potential bitline segment is discharged through one of the cross-coupled transistors. The higher potential segment is pulled up through one of the load transistors.

In 16K and higher density DRAMs, sense amplifier performance is improved by keeping static load transistors off during signal amplification and by driving the source of the cross-coupled pair slowly during initial sensing as suggested by Lynch and Boll [16]. If static load transistors are activated at the same time as the cross-coupled device pair, current flows through a load device into the lower potential bitline segment, unproductively dissipating power. In addition, the load device current going into the

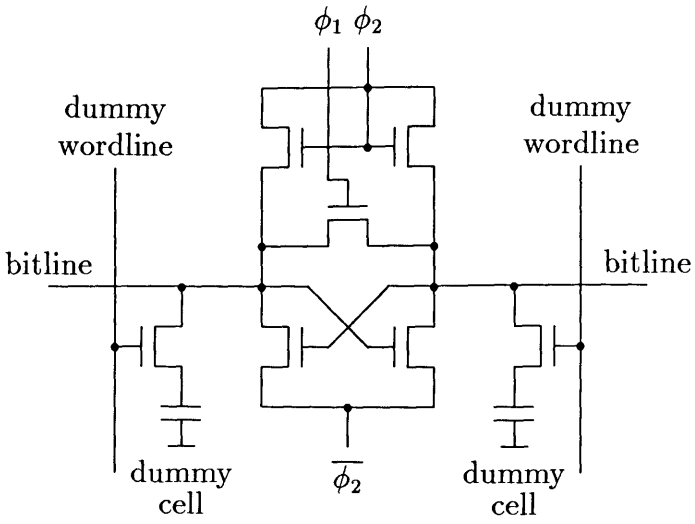

Figure 1.5: Stein *et al.* Balanced Flip-Flop Sense Amplifier

lower potential bitline is greater than the current going into the higher potential bitline. This difference hinders signal amplification. Keeping the load devices off until amplification of the sense signal through the cross-coupled pair is complete reduces power dissipation, speeds amplification, and eliminates offset due to load transistor mismatch. Driving the cross-coupled pair source node slowly during initial sensing reduces and can even eliminate current flow from the higher potential bitline segment through the flip-flop. As a result, power dissipation is lower, and a greater potential difference between the bitline segments can be developed. In addition, sense amplifier operation will be less sensitive to bitline capacitance imbalances and to geometry mismatches between the cross-coupled transistors [17], [18], [19].

1.5 DRAM Evolution

Over the last two decades, DRAM chip capabilities have dramatically improved. Advances in circuit and processing technology have produced a new DRAM generation,

with 4x greater chip capacity, every 2-4 years. 4M DRAMs are now in production. As shown in Figure 1.6, access time has gradually improved. Large decreases in power dissipation per bit, shown in Figure 1.7, have limited increases in chip power.

Increased chip capacity has been achieved primarily by decreasing cell size and increasing chip area. As shown in Figure 1.8, chip area has increased approximately 1.5x per generation. Cell area decreased by approximately 2.5x per generation as shown in Figure 1.9. Together, these two trends account for over 90% of the increase in chip capacity with each generation.

The decrease in cell area has been obtained by reducing feature sizes and by employing new cell structures. As shown in Figure 1.10, feature sizes have been reduced by about 1.4x per generation. This reduction accounts for a 2.1x reduction in cell area per generation. The remaining 1.2x cell area reduction has been produced through cell structure innovation.

The need to preserve charge capacity constrains cell evolution. Charge capacity is the difference in stored charge between '0' and '1' cell capacitor states, and is given by

$$Q_C \equiv \int_{V_{S0}}^{V_{S1}} C_S(V_S)\, dV_S \sim C_S \Delta V_S \tag{1.7}$$

where ΔV_S is the potential difference between stored '0' and '1' levels. Maximum sense signal magnitude is related to charge capacity by

$$\Delta V = \frac{1}{2} \frac{Q_C}{C_{BT} + C_S} \simeq \frac{1}{2} \frac{Q_C}{C_{BT}} \tag{1.8}$$

As chip capacity increases, decreases in bitline capacitance per bit are generally accompanied by increases in the number of cells per bitline. As a result, bitline segment capacitance remains roughly constant. Thus, charge capacity must be conserved in order to maintain adequate sense signal magnitude.

Particle-induced soft error rate considerations also discourage charge capacity re-

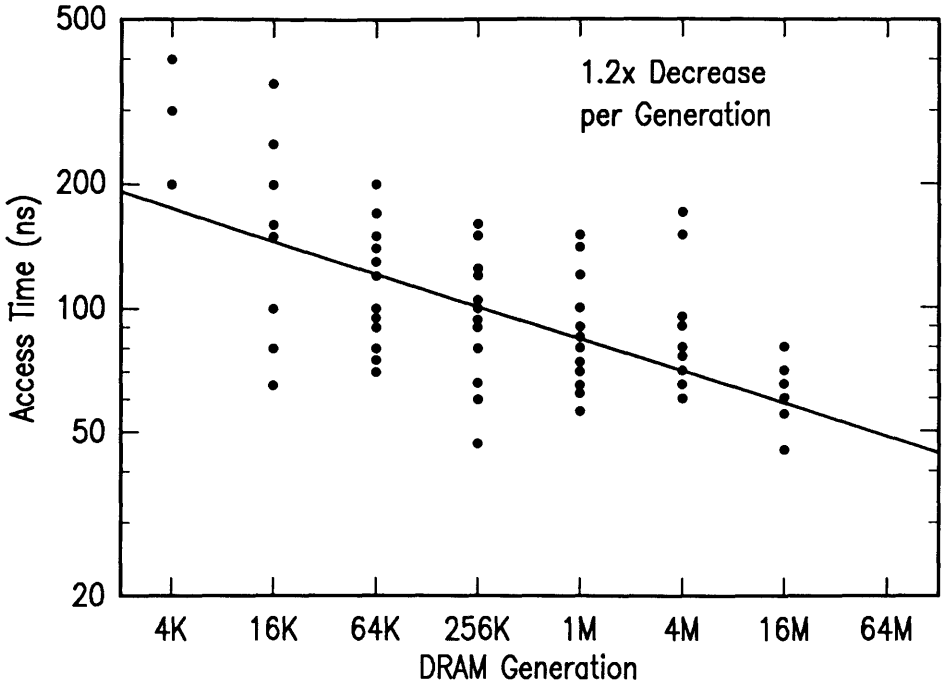

Figure 1.6: Access Time versus DRAM Generation

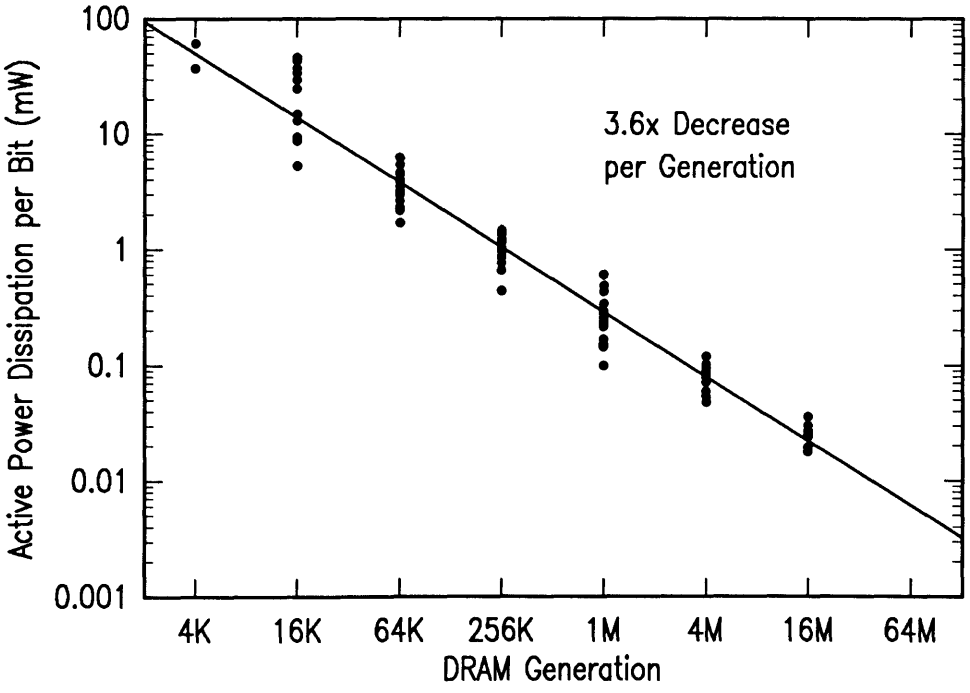

Figure 1.7: Power per Bit versus DRAM Generation

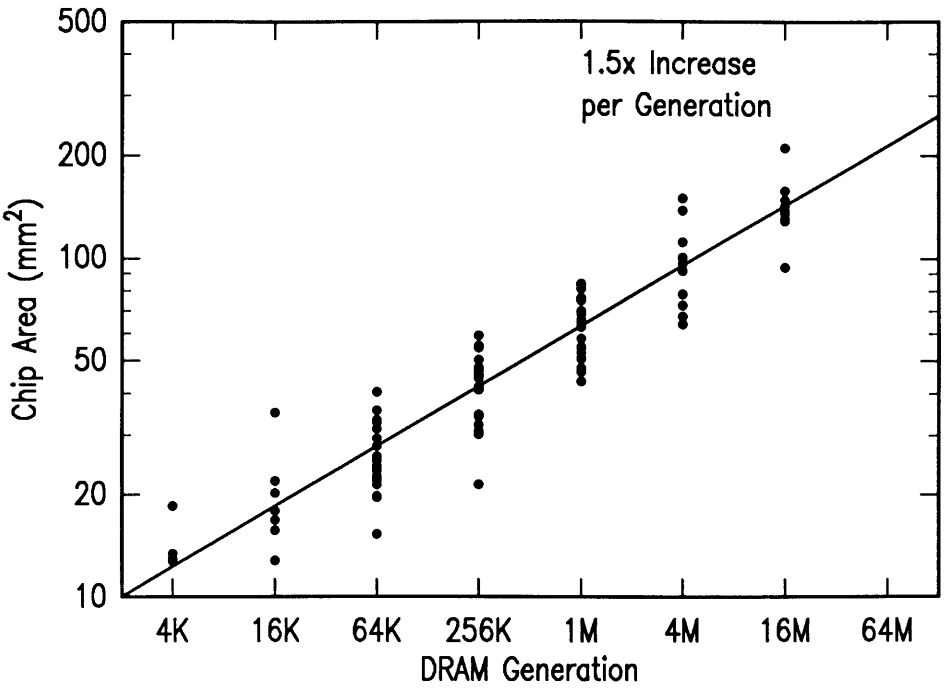

Figure 1.8: Chip Area versus DRAM Generation

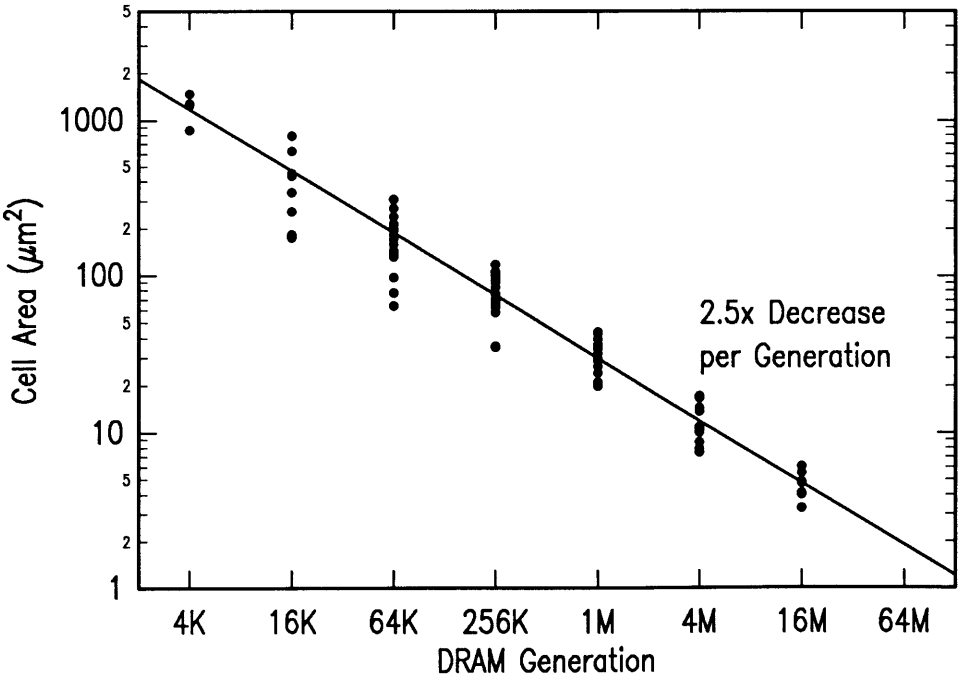

Figure 1.9: Cell Area versus DRAM Generation

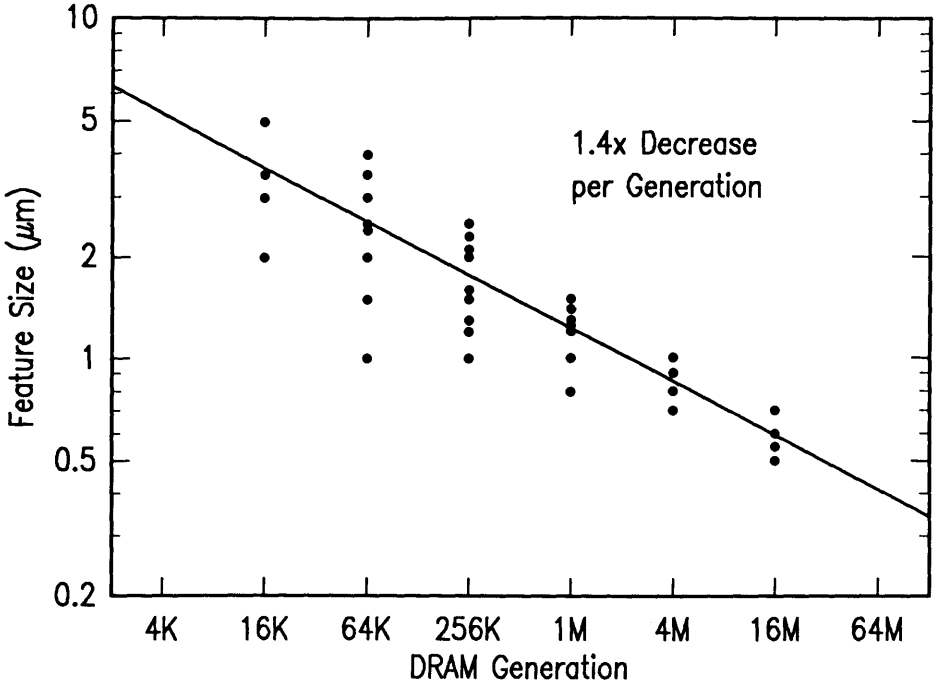

Figure 1.10: Feature Sizes versus DRAM Generation

duction. Soft errors occur when energetic particles upset stored data. Soft error sensitivity depends on the critical charge, the amount of charge needed to change the state of a cell. Critical charge is equal to the difference between the cell charge capacity and the amount of charge needed to guarantee proper sense amplifier operation, assuming nominal noise levels. For a given sense amplifier latch requirement and nominal noise level, decreasing cell charge capacity decreases critical charge. Soft error rates increase exponentially with decreasing critical charge [20].

Insulator properties limit charge capacity per unit capacitor storage area. For storage capacitors formed using MOS structures, charge capacity is related to cell design by

$$Q_C \sim \frac{\epsilon A_S}{d} \Delta V_S \tag{1.9}$$

where ϵ is the insulator dielectric constant, A_S is the capacitor storage area and d is the insulator thickness. $\Delta V_S/d$ must be restricted to avoid excessive leakage current

4K
planar cell
metal wordlines
diffused bitlines
single-level poly

16K
planar cell
metal wordlines
diffused bitlines
double-level poly

64K
planar cell
poly Si wordlines
metal bitlines
double-level poly

256K
Hi-C planar cell
polycide wordlines
metal bitlines
double-level poly

1M
Hi-C planar cell
1/2 V_{DD} plate
poly Si wordlines
metal bypass wordlines
polycide bitlines
triple-level poly

4M,16M
trench or stacked
capacitor cell
poly Si wordlines
metal bypass wordlines
polycide bitlines

Table 1.1: DRAM Cell Evolution

and insulator breakdown due to high electric fields. Thus, charge capacity per unit storage area, Q_C/A_S, is limited by the product of the dielectric constant and the maximum electric field, $\epsilon\mathcal{E}_{max}$.

Design advances have increased cell charge capacity per unit cell area, enabling cell area to be reduced with each new DRAM generation. Table 1.1 shows the evolution of typical cell structures. Rideout [21] has provided an excellent review of cell structures used in 4K and 16K DRAMs. Asai [22] and Sunami [23], [24] have published overviews of cell design trends. Noble [25] has examined cell design constraints. Stacked capacitor and trench capacitor cells suitable for high-density DRAMs have been reviewed by Lu [26] and Maes [27].

Table 1.2 shows the development of typical DRAM process features. Device length,

	4K	16K	64K	256K	1M	4M	16M
Technology	PMOS/ NMOS	NMOS	NMOS	NMOS	NMOS/ CMOS	CMOS	CMOS
Internal Supply Voltage(s) (V)	12,5, -3	12,5, -5	5	5	5	5	3.3-4
Device Length (μm)	7	5-6	2-3	1.5	1.2	1.0	0.6
Gate Oxide Thickness (Å)	1000	1000	500	350	250	200	150

Table 1.2: DRAM Process Evolution

gate oxide thickness, and internal supply voltages have been reduced as chip capacity increases. In addition, CMOS has supplanted NMOS as the dominant technology.

Chapter 2

Theoretical Analysis of Sense Amplifier Operation

Theoretical analysis of the sensing operation is useful for understanding circuit performance. While computer simulation may provide more precise results, theoretical analysis gives a much clearer picture of design and process parameter influences.

This chapter will focus on the operation of the cross-coupled MOS transistor pair. The circuit, shown in Figure 2.1, is the core of all modern DRAM sense amplifiers. Two issues will be addressed. First, given device parameters, what is the optimal latching pulse, $V_S(t)$? Second, given device parameters and constraints on the latching pulse, what is the sensitivity of the amplifier circuit?

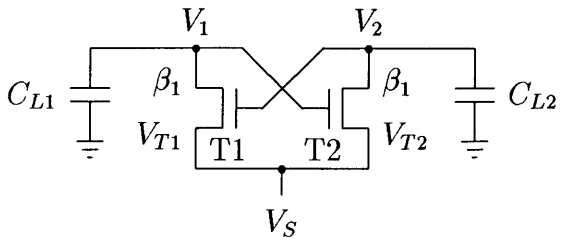

Figure 2.1: Cross-Coupled n-channel MOSFET Sense Amplifier Circuit

The following first-order MOS transistor current expressions will be used:

$$I_{DS} = \begin{cases} \beta(V_{GS} - V_T - \frac{1}{2}V_{DS})V_{DS}, & V_{DS} \leq V_{GS} - V_T \\ \frac{1}{2}\beta(V_{GS} - V_T)^2. & V_{DS} > V_{GS} - V_T \end{cases} \tag{2.1}$$

V_{GS} is the gate-source voltage, V_{DS} is the drain-source voltage, and V_T is the threshold voltage. β is the transistor gain factor and is given by

$$\beta \equiv \frac{W}{L}\mu_{eff}C_{ox} \tag{2.2}$$

where W and L are the transistor lengths and widths, respectively, μ_{eff} is the effective channel mobility, and C_{ox} is the gate oxide capacitance per unit area.

2.1 Latching Pulse Optimization

Sense amplifier performance depends on characteristics of the latching pulse, $V_S(t)$. Following the analysis of Lynch and Boll [16], the optimal latching pulse will be derived, given the constraint that no current may flow through the "off-side" (T2) of the flip-flop. Perfect matching will be assumed, giving

$$\begin{aligned} (W/L) &= (W/L)_1 = (W/L)_2, & \beta &= \beta_1 = \beta_2, \\ V_T &= V_{T1} = V_{T2}, & C_L &= C_{L1} = C_{L2}. \end{aligned} \tag{2.3}$$

Gate-source capacitances will be neglected for $V_{GS} < V_T$. They will be assumed constant for $V_{GS} \geq V_T$. A constant, C_C, will be used to model the capacitance between the two signal nodes. Variations in threshold voltages with device operating points will be ignored.

Prior to the start of the sensing operation, $V_1 = V_0$ and $V_2 = V_0 + v$, where v is the magnitude of the signal presented to the amplifier. $V_S > V_0 - V_T + v$, keeping both T1 and T2 off. Amplification begins, at $t = 0$, when the latch node potential, V_S, is driven below $V_0 - V_T + v$, turning on T1.

To maximize sensing speed, V_S should decrease as quickly as possible. Preventing off-side conduction requires $V_1 - V_S \leq V_T$. Thus, maximum sensing speed without off-side conduction is achieved when

$$V_S(t) = V_1(t) - V_T. \tag{2.4}$$

Initially, the optimal latching pulse is a negative step to $V_0 - V_T$. T1 will conduct, reducing V_1. V_S should decrease with V_1, always keeping T2 marginally off. As V_S decreases, the overdrive on T1 increases, and consequently V_1 decreases more rapidly. Thus, after the initial step, V_S will decrease at a progressively increasing rate.

Though T2 is always kept off, V_2 decreases as a result of capacitive coupling between the two signal nodes and T1 gate-source coupling. For $V_2 - V_S \geq V_T$, charge conservation requires

$$(V_0 + v)C_L + vC_C = V_2(t)C_L + [V_2(t) - V_1(t)]C_C + [V_2(t) - V_S(t) - V_T]C_{GS} \tag{2.5}$$

where C_{GS} is the gate-source capacitance. Using (2.4) in this expression gives an equation for $V_2(t)$:

$$V_2(t) = V_S(t) + V_T + f_1[V_0 - V_S(t) - V_T] + f_2 v \tag{2.6}$$

where

$$f_1 \equiv \frac{C_L}{C_L + C_C + C_{GS}} \quad \text{and} \quad f_2 \equiv \frac{C_L + C_C}{C_L + C_C + C_{GS}}. \tag{2.7}$$

Assigning $t = 0$ at the instant immediately before V_S begins decreasing, the node potentials at $t = 0^+$, immediately after the negative V_S step, are given by

$$\begin{aligned} V_1(0^+) &= V_0 \\ V_2(0^+) &= V_0 + f_2 v \\ V_S(0^+) &= V_0 - V_T. \end{aligned} \tag{2.8}$$

While $V_1 > V_2 - V_T$, T1 operates in the saturation regime and

$$-C_L \frac{dV_1(t)}{dt} - C_C \left[\frac{dV_1(t)}{dt} - \frac{dV_2(t)}{dt}\right] = \frac{\beta}{2}[V_2(t) - V_S(t) - V_T]^2. \tag{2.9}$$

Using (2.4) and (2.6) in (2.9) gives a differential equation for $V_S(t)$:

$$-(C_L + f_1 C_C)\frac{dV_S(t)}{dt} = \frac{\beta}{2}\{f_1[V_0 - V_S(t) - V_T] + f_2 v\}^2. \tag{2.10}$$

The solution to (2.10) with the initial condition given by (2.8) is

$$V_S(t) = V_0 - V_T - \frac{[\beta/2(C_L + f_1 C_C)]f_2{}^2 v^2 t}{1 - [\beta/2(C_L + f_1 C_C)]f_1 f_2 v t}. \tag{2.11}$$

Equation (2.11) is valid until, at $t = t_{sat}$, T1 goes into the linear operation regime. t_{sat} is defined by

$$V_1(t_{sat}) = V_2(t_{sat}) - V_T. \tag{2.12}$$

Using (2.4), (2.6), and (2.11) in (2.12) gives

$$t_{sat} = \frac{2(C_L + f_1 C_C)}{\beta f_1 f_2 v}\frac{(V_T - f_2 v)}{V_T} = \frac{2(C_L + 2C_C + C_{GS})}{\beta f_2 v}\frac{(V_T - f_2 v)}{V_T}. \tag{2.13}$$

Substituting (2.13) in (2.11) gives

$$V_S(t_{sat}) = V_0 - V_T - \frac{1}{f_1}(V_T - f_2 v). \tag{2.14}$$

Once T1 is operating in the linear regime

$$-(C_L + f_1 C_C)\frac{dV_S(t)}{dt} = \beta\left\{V_2(t) - V_S(t) - V_T - \left[\frac{V_1(t) - V_S(t)}{2}\right]\right\}[V_1(t) - V_S(t)]. \tag{2.15}$$

Using (2.4) and (2.6) in (2.15) gives a differential equation for $V_S(t)$:

$$-(C_L + f_1 C_C)\frac{dV_S(t)}{dt} = \beta V_T\left\{f_1[V_0 - V_S(t) - V_T] + f_2 v - \frac{V_T}{2}\right\}. \tag{2.16}$$

The solution to this equation with the initial condition given by (2.14) is

$$V_S(t) = V_0 - V_T - \frac{1}{f_1}(V_T - f_2 v) + \frac{V_T}{2f_1}\left\{1 - \exp\left[\frac{\beta f_1 V_T(t - t_{sat})}{C_L + f_1 C_C}\right]\right\}. \tag{2.17}$$

The latch node potential rapidly falls according to (2.17) until V_S reaches ground. At this point the sensing operation can be considered complete. V_2 will remain

constant while V_1 decreases towards ground. The length of the sensing operation, t_{sense}, is defined by

$$V_S(t_{sense}) = 0. \tag{2.18}$$

Substituting (2.17) in (2.18) gives

$$t_{sense} - t_{sat} = \frac{C_L + f_1 C_C}{\beta f_1 V_T} \ln \left[\frac{2f_1(V_0 - V_T) - V_T + 2f_2 v}{V_T} \right]. \tag{2.19}$$

After V_S reaches ground, conduction through T1 continues pulling V_1 towards ground. The final node potentials are given by

$$\begin{aligned} V_1(\text{final}) &= 0 \\ V_2(\text{final}) &= f_1 V_0 + f_2 v + (1 - f_2) V_T \\ V_S(\text{final}) &= 0. \end{aligned} \tag{2.20}$$

The total reduction of the high signal node potential, V_2, resulting from the sensing operation is given by

$$\Delta V_2[\text{coupling}] = \frac{C_C + C_{GS}}{C_L + C_C + C_{GS}} V_0 - \frac{C_{GS}}{C_L + C_C + C_{GS}} (V_T - v) \tag{2.21}$$

Examples of optimal $V_S(t)$ waveforms are shown in Figure 2.2. Since, for practical parameter values, $t_{sense} \approx t_{sat}$, several conclusions may be drawn from (2.13) and (2.21):

- for $C_{GS} \ll C_L + C_C$, t_{sense} is approximately proportional to $(C_L + 2C_C + C_{GS})$;
- t_{sense} is approximately inversely proportional to the transistor gain factor, β;
- for $v \ll V_T/f_2$, t_{sense} is approximately inversely proportional to the initial signal, v; and
- for $V_0 \gg (V_T - v)$, $\Delta V_2/V_2(\text{initial})$ is approximately equal to $(C_C + C_{GS})/(C_L + C_C + C_{GS})$.

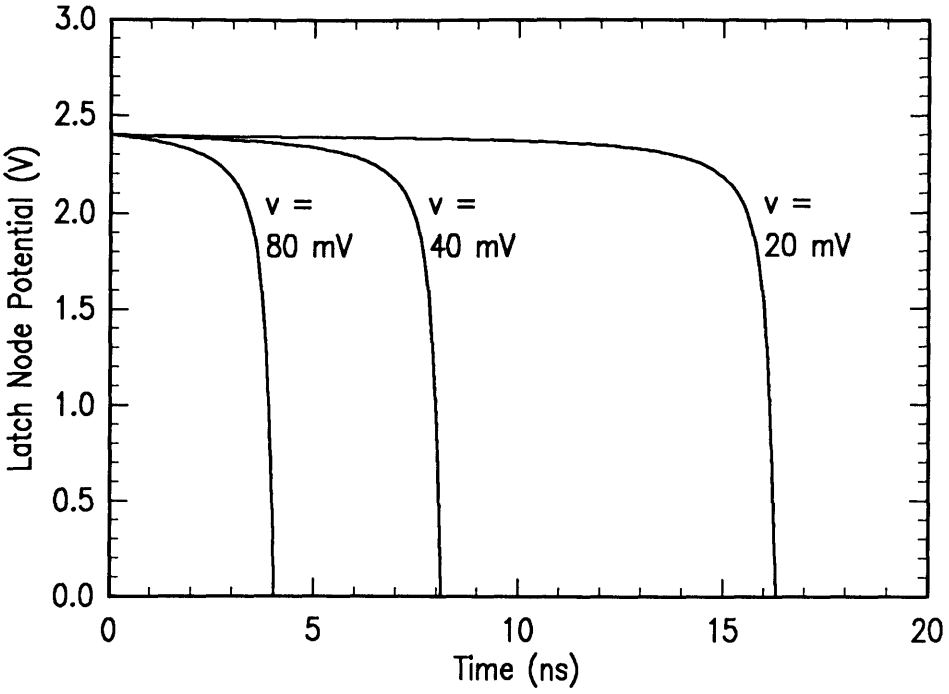

Figure 2.2: Optimal Latching Pulse Waveforms

Sensing speed can be increased by allowing off-side conduction. The consequence of off-side conduction is a reduction of the final voltage of the higher potential signal node, V_2. Lynch and Boll [16] derived expressions for the optimal latching pulse assuming constant off-side current. Their analysis shows that t_{sat} is given by

$$t_{sat} = \frac{C_L}{\beta f V_C} \ln \left[\frac{V_T}{V_T + 2V_C} \frac{fv + 2V_C}{fv} \right] \tag{2.22}$$

where

$$f \equiv \frac{C_L}{C_L + C_{GS}}. \tag{2.23}$$

V_C is the constant gate-source overdrive of transistor T2. Signal node coupling was neglected.

If $V_C < 5fv$ and $V_C \ll V_T$

$$\ln \left[\frac{V_T}{V_T + 2V_C} \frac{fv + 2V_C}{fv} \right] \approx 2 \left[\frac{\frac{fv+2V_C}{fv} - 1}{\frac{fv+2V_C}{fv} + 1} \right] = 2 \frac{2V_C}{2fv + 2V_C}. \tag{2.24}$$

Using this equation in (2.22) gives

$$t_{sat} \approx \frac{2C_L}{\beta f(fv + V_C)} \quad \text{for } V_C < 5fv \text{ and } V_C \ll V_T. \tag{2.25}$$

Comparing this equation and (2.13) shows that for small off-side conduction levels, the effect of increasing V_C on the length of the optimal latching pulse is similar to the effect of increasing the initial signal v. The reduction in the final voltage of the higher signal node potential due to off-side conduction is given by

$$\Delta V_2[\text{conduction}] = \frac{\beta {V_C}^2 t_{sense}}{2(C_L + C_{GS})} \approx \frac{\beta f {V_C}^2 t_{sat}}{2C_L}. \tag{2.26}$$

Substitution of (2.25) into (2.26) gives

$$\Delta V_2[\text{conduction}] \approx \frac{{V_C}^2}{(fv + V_C)} \quad \text{for } V_C < 5fv \text{ and } V_C \ll V_T. \tag{2.27}$$

For low conduction levels, the reduction in the final high signal potential is less than the "off" transistor overdrive, V_C. Thus, significant increases in sensing speed can be achieved with only small reductions in the final high signal potential. For example, sensing with $V_C = v$ is approximately two times faster than sensing without off-side conduction. Yet the additional drop in the final high signal potential is less than v.

2.2 Sensitivity

One of the most important sense amplifier performance characteristics is sensitivity. Loosely defined, the sensitivity is the minimum detectable signal presented to the sense amplifier. Natori [28] more precisely defines the sensitivity as the minimum initial signal, v, needed to insure that the resulting drop in the final high-level signal node potential due to off-side conduction, ΔV_2, will not prevent correct subsequent circuit operation.

Sense amplifier sensitivity may be characterized by two components, offset and minimum overdrive. The offset voltage is the initial signal which results in precisely

equal signal node potential changes during amplifier operation. The offset voltage of a perfectly balanced sense amplifier is zero. The minimum overdrive voltage is the minimum difference between the initial signal and the offset voltage needed to insure that the final high-level signal node potential will permit correct subsequent circuit operation. Sensitivity can be expressed as

$$v_S = v_{OS} + v_{OD,min} \tag{2.28}$$

where v_{OS} is the offset voltage and $v_{OD,min}$ is the minimum overdrive voltage.

Because the sensing operation outcome depends on the shape of the latching pulse, $V_S(t)$, and the initial signal, v, characterization of sensitivity is very difficult. In whatever manner the problem is addressed, simplifying assumptions must be employed to make the analysis tractable. For any single approach, the assumptions required cast significant doubt on the general validity and applicability of the solution. However, by examining the results of several different analyses, some important conclusions can be made with a good degree of confidence.

Sensitivity will be examined in the following manner. First, the physical origins of electrical mismatches will be summarized. Then, the results of published analyses will be reviewed. Next, sense amplifier sensitivity will be related to the dc offset voltage of the MOS source-coupled pair. Finally, some general conclusions will be presented.

2.2.1 Sense Amplifier Circuit Mismatches

Sensitivity is commonly characterized using electrical mismatch parameters ΔV_T, $\Delta\beta$, ΔC_L, and ΔC_{GS}. These parameters are defined by the following expressions:

$$\begin{aligned} V_{T1} &= V_T + \Delta V_T/2, & V_{T2} &= V_T - \Delta V_T/2, \\ \beta_1 &= \beta - \Delta\beta/2, & \beta_2 &= \beta + \Delta\beta/2, \\ C_{L1} &= C_L + \Delta C_L/2, & C_{L2} &= C_L - \Delta C_L/2, \\ C_{GS1} &= C_{GS} + \Delta C_{GS}/2, & C_{GS2} &= C_{GS} - \Delta C_{GS}/2. \end{aligned} \tag{2.29}$$

Many process variations result in threshold voltage mismatches. The nominal threshold voltage, V_T, is given by

$$V_T = \phi_{MS} - \frac{Q_{SS}}{C_{ox}} - \frac{Q_i}{C_{ox}} + 2\phi_f + \gamma\sqrt{V_{SB} + 2\phi_f}. \tag{2.30}$$

ϕ_{MS} is the metal-silicon work-function difference. Q_{SS} is the surface-state charge. Q_i is the effective surface charge density per unit area due to threshold adjustment implants. The oxide capacitance per unit area, C_{ox}, is given by

$$C_{ox} = \epsilon_{ox}/t_{ox} \tag{2.31}$$

where ϵ_{ox} is the permittivity of the gate oxide and t_{ox} is the gate oxide thickness. The bulk Fermi potential, ϕ_f, is given by

$$\phi_f = \frac{kT}{q} \ln\left(\frac{N}{n_i}\right) \tag{2.32}$$

where N is the bulk doping. The bulk threshold parameter, γ, is given by

$$\gamma = \frac{1}{C_{ox}}\sqrt{2q\epsilon_{Si}N} \tag{2.33}$$

where ϵ_{Si} is the permittivity of the silicon. From (2.30), (2.31), (2.32), and (2.33) it is apparent that variations in oxide thickness, surface-state charge, threshold adjustment implant, and bulk doping result in threshold voltage mismatches. In addition, variations in channel length may also result in threshold mismatches due to short channel effects.

The transistor gain factor, β, is given by (2.2). Channel width, channel length, oxide thickness, and effective mobility variations result in β mismatches.

In saturation, the intrinsic gate-source capacitance is given by

$$C_{GS} = \frac{2}{3}WLC_{ox}. \tag{2.34}$$

Thus, device width, device length, and oxide thickness variations result in C_{GS} mismatches.

The total signal node to ground capacitance, C_L, includes capacitances in the sense amplifier, and unless the bitlines are completely isolated from the sense amplifier during sensing, capacitances in the storage cell array. A major component of the sense amplifier contribution is the depletion region capacitances between the bulk and drain regions of the cross-coupled devices. Bulk doping variations result in C_L mismatches. In addition, misalignment of gate and diffusion masks may create differences in cross-coupled device drain areas, resulting in capacitance mismatches. The array contribution to the signal node to ground capacitance is subject to mismatches due to a variety of process variations including differences in transfer device diffusion capacitance, differences in isolation thickness, and differences in bitline width and height.

2.2.2 Published Sensitivity Analyses

Ieda *et al.* [17], [18] analyzed sense amplifier offset using computer simulation. They assumed that the latching pulse is given by

$$V_S(t) = V_0 - V_{T2} - Kt \tag{2.35}$$

where K is constant. They obtained the following empirical expression for sense amplifier offset:

$$v_{OS} = A\sqrt{\frac{C_L K}{\beta}}\left[\frac{\Delta\beta}{\beta} + \frac{\Delta C_L}{C_L}\right] + \Delta V_T. \tag{2.36}$$

A is a constant. Signal node coupling capacitance was neglected. C_{GS} variations were apparently ignored.

Masuda *et al.* [15] examined sense amplifier offset analytically. They assumed that the latch node potential, V_S, decreases linearly with time until both transistors turn

on. Once both transistors begin conducting, the latch node potential was assumed to decrease in such a manner that the low signal node potential, V_1, decreases linearly with time according to

$$\frac{dV_2(t)}{dt} = \alpha K \tag{2.37}$$

where α and K are constants. They derived the following expression for sense amplifier offset:

$$v_{OS} \approx \sqrt{\frac{C_L \alpha K}{2\beta}} \left[\frac{\Delta\beta}{\beta} + \frac{\Delta C_L}{C_L} \right] + \Delta V_T. \tag{2.38}$$

Signal node coupling capacitance and gate-source capacitances were apparently ignored.

Kraus [29] also examined sense amplifier offset analytically. Like Ieda *et al.* , he assumed that the latch node potential decreases linearly with time:

$$V_S = V_S(0) - kt. \tag{2.39}$$

He obtained the following expression for sense amplifier offset:

$$v_{OS} \approx \Delta V_T + \sqrt{\frac{2C_{L1}k}{\beta_1}} - \sqrt{\frac{2C_{L2}k}{\beta_2}}. \tag{2.40}$$

Signal node coupling capacitance and gate-source capacitances were apparently ignored. If $\Delta\beta/\beta \ll 1$ and $\Delta C_L/C_L \ll 1$ this expression reduces to

$$v_{OS} \approx \Delta V_T + \sqrt{\frac{C_L K}{2\beta}} \left(\frac{\Delta\beta}{\beta} + \frac{\Delta C_L}{C_L} \right). \tag{2.41}$$

Natori [28] derived a general expression for sensitivity. He began by deriving expressions for the optimal latching pulse assuming constant off-side current. He observed that the variations in optimal $V_S(t)$ waveforms are mostly due to changes in t_{sat}. Arbitrary $V_S(t)$ waveforms, he argued, can be characterized by one parameter, t_{sat}, and therefore matched with an optimal $V_S(t)$ waveform. Using results of his

optimal $V_S(t)$ analysis, he derived the following equations for sensitivity:

$$v_S = 2V_T\zeta + \frac{1}{f}\sqrt{\frac{2(C_L + C_{GS})\Delta V_2}{\beta t_{sat}}}\frac{2 - a_0[2(1-f)\eta + (3-2f)\xi - \mu]}{a_0 - 1} \tag{2.42}$$

$$a_0 = \left(1 + \frac{2}{V_T}\sqrt{\frac{2(C_L + C_{GS})\Delta V_2}{\beta t_{sat}}}\right)\exp\left(\sqrt{\frac{2\beta t_{sat}\Delta V_2}{C_L + C_{GS}}}\right). \tag{2.43}$$

The asymmetry parameters ζ, μ, ξ, and η are defined by

$$\begin{aligned} \zeta &= \Delta V_T/2V_T, \\ \mu &= -\Delta\beta/2\beta, \\ \xi &= \Delta C_L/2C_L, \\ \eta &= \Delta C_{GS}/2C_{GS}. \end{aligned} \tag{2.44}$$

ΔV_2 is the maximum drop in the final high level signal node due to off-side conduction that will not prevent correct subsequent circuit operation. Signal node coupling capacitance was ignored. Offset and minimum overdrive contributions to sensitivity are given by:

$$v_{OS} = 2V_T\zeta + \frac{1}{f}\sqrt{\frac{2(C_L + C_{GS})\Delta V_2}{\beta t_{sat}}}\frac{a_0}{a_0 - 1}, \tag{2.45}$$

$$v_{OD,min} = \frac{1}{f}\sqrt{\frac{2(C_L + C_{GS})\Delta V_2}{\beta t_{sat}}}\frac{4}{a_0 - 1}. \tag{2.46}$$

For $2\beta t_{sat}\Delta V_2/(C_L + C_{GS}) \gg 1$, (2.42) and (2.43) reduce to

$$v_S \approx \Delta V_T + \frac{1}{f}\sqrt{\frac{2(C_L + C_{GS})\Delta V_2}{\beta t_{sat}}}\left[(1-f)\frac{\Delta C_{GS}}{C_{GS}} + \frac{(3-2f)}{2}\frac{\Delta C_L}{C_L} + \frac{1}{2}\frac{\Delta\beta}{\beta}\right]. \tag{2.47}$$

2.2.3 Source-Coupled Pair Offset

The MOS source-coupled pair is shown in Figure 2.3. The input referred dc offset voltage, defined as the differential input voltage required to make $V_O = 0$, is analogous to offset voltage of the cross-coupled pair. Because dc source-coupled pair offset depends only on dc circuit parameters, it is much easier to analyze than cross-coupled pair offset, which depends on $V_S(t)$.

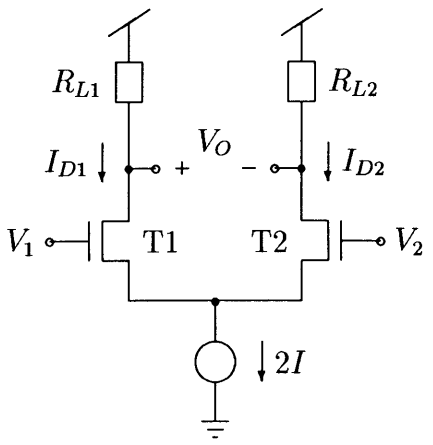

Figure 2.3: Source-Coupled MOSFET Pair

Source-coupled pair performance characteristics are derived in [30]. Mismatch parameters are defined by

$$\begin{array}{rclrcl} V_1 &=& V_I + \Delta V_I/2, & V_2 &=& V_I - \Delta V_I/2, \\ I_{D1} &=& I + \Delta I_D/2, & I_{D2} &=& I - \Delta I_D/2, \\ V_{T1} &=& V_T + \Delta V_T/2, & V_{T2} &=& V_T - \Delta V_T/2, \\ \beta_1 &=& \beta - \Delta\beta/2, & \beta_2 &=& \beta + \Delta\beta/2, \\ R_{L1} &=& R_L - \Delta R_L/2, & R_{L2} &=& R_L + \Delta R_L/2. \end{array} \tag{2.48}$$

The dc offset voltage is given by

$$V_{OS} = \Delta V_T + \frac{I}{G_m}\left(\frac{\Delta\beta}{\beta} + \frac{\Delta R_L}{R_L}\right). \tag{2.49}$$

The transconductance of the source coupled pair, G_m, is given by

$$G_m \equiv \left.\frac{\partial \Delta I_D}{\partial \Delta V_I}\right|_{\Delta V_I = 0} = \sqrt{2I\beta}. \tag{2.50}$$

A key source-coupled pair design parameter is the G_m/I ratio. This ratio is inversely proportional to the square root of I and is proportional to the square root of β. The $\Delta\beta$ and ΔR_L components of the offset are inversely proportional to G_m/I. Thus, source-coupled pair offset can be reduced by operating the pair at low currents and by increasing the W/L ratio of the transistors. If G_m/I is sufficiently large, $V_{OS} \approx \Delta V_T$.

These results suggest a tradeoff between cross-coupled pair sensing speed and sensitivity. To increase sensing speed, $V_S(t)$ must decrease more rapidly, resulting in greater on-side and off-side currents. Higher currents imply a smaller G_m/I ratio. Thus, increasing sensing speed will likely result in greater offset.

2.2.4 Design Impacts

A speed versus power and sensitivity tradeoff is inherent to the cross-coupled pair. A faster latch node potential reduction increases sensing speed but also increases off-side current and reduces sensitivity.

In general, overall performance can be improved by reducing the total signal node capacitance. Signal node capacitance can be reduced by isolating the signal nodes from the bitlines during sensing. Equations (2.13) and (2.22) show that for a fixed off-side current level, reducing C_L will increase sensing speed. Equations (2.36), (2.38), (2.41), and (2.47) suggest that for a fixed sensing speed, reducing C_L will improve sensitivity.

Reducing C_L is not always beneficial. Unless C_L is large relative to C_C and C_{GS}, performance may be degraded. As C_L is reduced, the high signal potential drop due to coupling increases according to Equation (2.21). If C_L and $(C_C + C_{GS})$ are comparable, the increase may be substantial.

Increasing device widths, W, improves amplifier performance at the expense of additional circuit area. Increasing W increases β. Equations (2.13) and (2.22) show that for a fixed off-side current level, increasing β will increase sensing speed. Equations (2.36), (2.38), (2.41), and (2.47) suggest that for a fixed sensing speed, increasing β will improve sensitivity. In addition, since for a given process ΔW is likely independent of W, a larger absolute W value should produce a smaller $\Delta W/W$ ratio, improving sensitivity.

A β and circuit area verses ΔV_T and $\Delta L/L$ tradeoff must be made in selecting device lengths. Short channels give higher β values and reduce circuit area. However, short channel devices exhibit a strong threshold voltage dependence on channel length due to short channel effects. In addition, a larger absolute L value should produce a smaller $\Delta L/L$ ratio.

Chapter 3

Sense Amplifier Design Evolution

3.1 4K DRAM Generation

The 4K DRAM Generation represents the emergence of modern DRAM design. In this generation NMOS technology supplanted PMOS technology, the single transistor cell replaced the three-transistor cell, and the divided bitline architecture and balanced flip-flop sense amplifier were first employed. Mostek introduced address multiplexing, reducing package size.

3.1.1 Texas Instruments

The 4K DRAM published by TI in 1973 [31] is one of the first commercial DRAMs to use the divided bitline architecture and balanced flip-flop sense amplifiers. The TI DRAM, like many other 4K DRAMs, employs a single polysilicon cell with diffused bitlines and metal wordlines. Three power supplies are required: +12 V for all circuits except the output buffer, +5 V for the output buffer, and -3 V for substrate biasing. Though each bitline segment has only 32 cells, the large bitline junction capacitance results in a sense signal of only 200 mV. The storage capacitance is approximately 100 fF and the cell area is approximately 1300 mm^2.

The TI 4K DRAM sense amplifier is shown in Figure 3.1. During standby the

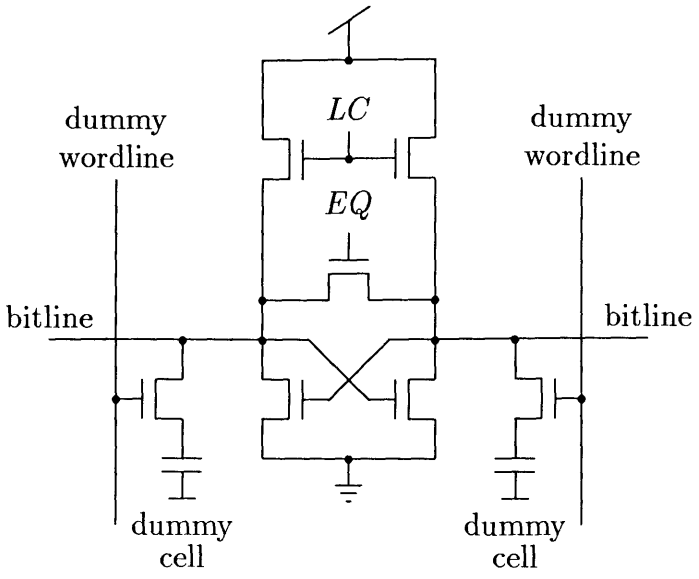

Figure 3.1: TI 4K DRAM Sense Amplifier

load clock, LC, is low and the equalization clock, EQ, is high, shorting the two bitline segments together. The cross-coupled transistor pair pulls the segments down to $+1$ V_T above ground. The segments may float below this potential. The dummy storage capacitors, equal in capacitance to the cell storage capacitors, are precharged to a potential approximately midway between the stored '0' and '1' voltage levels. After EQ is pulled down, the selected wordline and dummy wordlines are activated. Driving LC high turns on the load transistors, activating the flip-flop. Initially both signal node potentials rise. The difference in signal node potentials causes a difference in load currents which tends to equalize the potentials. As the signal node potentials rise above V_T, the difference in driver transistor currents increases. Amplification begins when the difference in driver transistor currents exceeds the difference in load transistor currents. Eventually, the flip-flop reaches a stable state.

The TI sense amplifier circuit requires only two clock signals, LC and EQ. These

signals carry current only when charging or discharging sense amplifier device gates. Employing clock signals to drive the sources of the cross-coupled transistors would require a substantial increase in chip area to accommodate the clock drivers.

To minimize signal loss due to load current differences, LC should have a short rise time. As the load device overdrives increase, the ratio of the current difference to the common-mode current decreases. Thus, less signal is lost as the common-mode bitline potentials increase.

Because the bitline precharge voltage is not midway between the '0' and '1' potentials, the use of dummy cells is necessary to produce reference potentials on bitline segments opposite the segments connected to the selected cells. A voltage generator provides a dummy storage capacitor precharge potential which tracks the supply voltage and the threshold voltage.

Selection of load transistor dimensions involves a tradeoff between amplifier speed and power. Load transistor currents are proportional to the W/L ratio of the devices. Higher current levels produce a faster increase in the high bitline potential. Lower currents limit dynamic and static power dissipation.

Amplifier sensitivity depends on the ratio of the driver and load transistor gain factors, β_D and β_L. The load and driver transistor current differences are proportional to β_L and β_D, respectively. Load transistor current differences work to reduce the signal. Unless β_D is several times larger than β_L, the common-mode bitline potential at which the driver transistor current difference begins to exceed the load transistor current difference will be quite large. As a result, the initial signal will be significantly reduced before amplification begins.

The final high and low bitline potentials also depend on the β_D/β_L ratio. A larger β_D/β_L ratio will give a lower final low bitline potential. As long as the final low potential is less than $+1\ V_T$, the final high potential will approach $V_{DD} - V_T$.

The β_D/β_L ratio can be increased either by increasing the width of the driver transistors or decreasing the W/L ratio of the load transistors. Increasing the width of the driver transistors requires additional layout area. Decreasing the W/L ratio of the load transistors reduces amplifier speed.

The low bitline precharge potential compromises sensitivity. Load transistor currents must increase the common-mode bitline potential before amplification begins. Even if the amplifier is perfectly balanced, load transistor current differences will reduce the signal. Load transistor mismatches may increase the current difference. In addition, bitline capacitance variations may increase the difference in the rate at which the bitline potentials rise. These problems are accentuated if the bitline potentials float below $+1$ V_T during precharge.

Because of the low bitline precharge potential, signal development is relatively fast. In the worst case, signal development begins when the wordlines reach $+2$ V_T. In addition, the maximum transfer device overdrive is large. Signal development would be even faster if the bitlines were precharged to ground. However, a larger increase in the common-mode bitline potential would be required to initiate signal amplification. Thus, sensitivity would be degraded.

A higher bitline precharge potential would improve sensitivity and reduce the load current required to increase the high bitline potential. However, if a higher precharge potential were employed the sources of the cross-coupled transistors could not be tied directly to ground. In addition, signal development would be slower.

3.1.2 Microsystems International

Foss and Harland published a Microsystems International 4K DRAM design in 1975 [32], [33], paying particular attention to sense amplifier design. Like the TI 4K DRAM, the Microsystems International DRAM employs a single polysilicon cell with

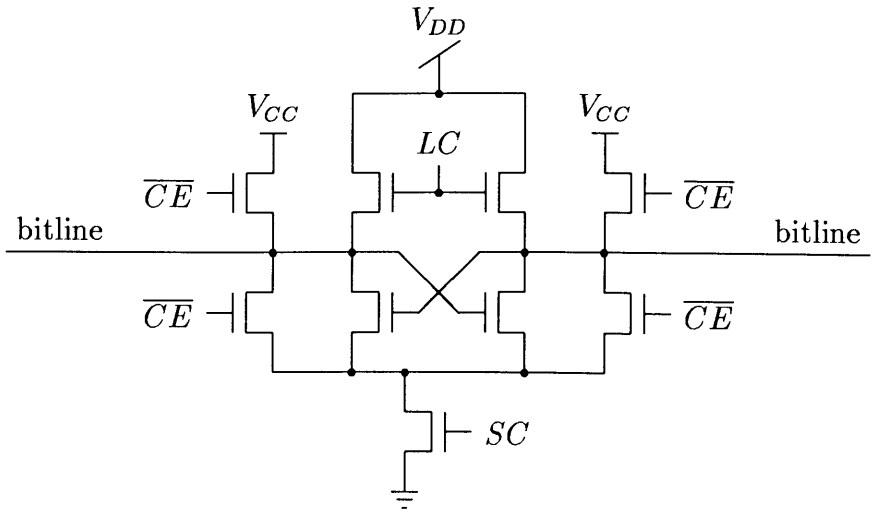

Figure 3.2: Microsystems International 4K DRAM Sense Amplifier

diffused bitlines and metal wordlines. +12 V V_{DD} and +5 V V_{CC} supplies are used. A 120 fF storage capacitance is achieved with an approximately 1250 μm^2 cell area. Each bitline segment includes 32 cells, resulting in a 1 pF bitline segment capacitance. Chip area is about 13 mm^2.

The sense amplifier is shown in Figure 3.2. During standby the load clock, LC, and the set clock, SC, are low. $\overline{CE}$ is high, precharging the bitlines and the latch node to V_{CC}. A read operation begins with $\overline{CE}$ going low. The selected wordline is activated. The potentials of bitline segments connected to cells storing a '1' increase. The potentials of segments connected to cells storing a '0' decrease. Bitline segments on the side of the sense amplifier opposite the selected wordline remain at V_{CC}.

Once signal development is complete SC rises, gradually pulling the latch node towards ground. While the higher signal node potential remains near V_{CC}, the lower node potential decreases towards ground. As the lower potential node reaches ground, LC goes high, slowly pulling the higher potential node to $V_{DD} - V_T$.

The sensitivity and speed of the amplifier depend on the rise time of the set clock.

A slower rise time reduces susceptibility to circuit mismatches. A faster rise time improves amplifier speed.

The column access circuits are designed to read the selected column before the high potential bitline segments are pulled up by the load transistors. As a result, chip access time is independent of load transistor operation. In addition, because the load transistors are not active during initial sensing, load transistor mismatches will not significantly degrade amplifier sensitivity.

A tradeoff must be made between cycle time and power dissipation. A larger load transistor W/L ratio reduces the time required to restore '1' cell potentials. A smaller W/L ratio reduces sense amplifier power dissipation.

The sensing scheme does not employ dummy cells. As a result, the bitline precharge potential determines the '0' and '1' signal magnitudes. Charge injected from the wordline to the selected bitline segment must be considered when choosing the precharge potential. The benefits of avoiding dummy cells include reduced chip complexity and layout area savings.

Use of the V_{CC} supply voltage for the bitline precharge potential avoids the complexity and layout area of an internal voltage generator and is convenient for signal margin testing. However, the precharge potential will not track other internal voltages and circuit parameters. As a result, the signal margin may be reduced.

Separate transistors are used to pull down each latch node. An alternative to this approach is to connect all the latch nodes together and use a single shared pull down circuit. If a shared pull down circuit is employed, sense amplifier operation is sensitive to the total current in the latch node set bus and is therefore sensitive to the stored data pattern. Use of separate transistors allows better latch node control and avoids the need for a latch node driver capable of carrying large currents. However, extra sense amplifier layout area for the latch node pull down and precharge devices

is required.

3.2 16K DRAM Generation

Power dissipation considerations played a key role in 16K DRAM design. Typical 4K DRAMs have only 64 sense amplifiers. In typical 16K DRAMs, 128 sense amplifiers are active during read cycles. The increase in the number of active sense amplifiers necessitated substantial reduction in power dissipation per sense amplifier.

Activating static load devices during sensing results in significant off-side current. Most 16K DRAM designs precharge bitlines to V_{DD} in order to minimize, if not eliminate, activation of load devices during sensing.

3.2.1 Intel

The Intel 16K DRAM published in 1976 [34], [35], [36] introduced the planar, double-polysilicon cell used in most 16K DRAMs. The cell employs diffused bitlines and metal wordlines. The Intel DRAM requires three power supplies: +12 V, +5 V, and -5 V. The memory is divided into two 8K arrays. In normal operation, only one array is active, reducing power consumption. Each bitline segment serves only 32 cells. Bitline segment capacitance is 500 fF. Cell storage capacitance is 30 fF. Cell area and chip area are approximately 455 μm^2 and 22 mm^2, respectively.

The Intel DRAM sense amplifier is shown in Figure 3.3. The dummy storage capacitance is half the ordinary cell storage capacitance. During standby, the latch node, SA, is allowed to float. $\overline{CE}$ is high, equalizing the bitline segment potentials and precharging the dummy storage capacitors to ground. The load clock, LC, is high, precharging the bitline segments to a potential near V_{DD}. $\overline{CE}$ and LC go low at the beginning of a read operation. When the selected wordline is activated, the dummy wordline on the opposite side of the sense amplifier is also activated. After signal development is complete, the latch node is gradually pulled down to ground,

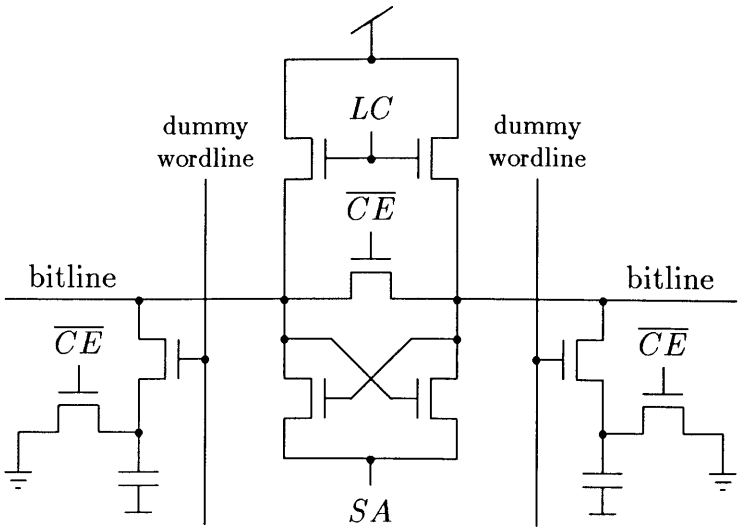

Figure 3.3: Intel 16K DRAM Sense Amplifier

amplifying the signal. Once initial amplification is complete, LC is pulsed high, restoring the high bitline potential near V_{DD}.

The half-capacitance dummy cell technique is simple and efficient. However, differences in dummy cell and storage cell capacitances create mismatches between signal node capacitances, reducing amplifier sensitivity.

Use of clocked load devices enables active restoration of full signal levels without incurring power dissipation through the loads during primary sensing. Circuitry required to generate and drive the load clocks is shared by all sense amplifiers. Thus, with many active sense amplifiers, the price of load device clock generation per sense amplifier is fairly low.

The high bitline precharge potential has important benefits. The time and power required to pull up high potential bitline segments are minimized. In addition, load devices can be used to precharge the bitline segments, conserving layout area.

The high precharge potential results in relatively low precharge device overdrive, lengthening the interval required to precharge the bitlines. The use of a device to

short the bitline segments speeds potential equalization, mitigating this disadvantage. Without an equalization device, incomplete bitline precharge would likely result in differences between bitline segment potentials, causing significant signal loss.

In the Intel DRAM, each 8K array has a common latch node, SA. As a result, independent latch node set devices need not be included in each amplifier. This saves sense amplifier area and permits more complex set clock timing.

The latch node decrease rate depends on the total capacitance seen by the driver. Until the latch node is pulled $+1$ V_T below a bitline potential, the driver does not see the bitline capacitance. Suppose one sense amplifier is detecting a '1' and all other amplifiers are detecting a '0', the average bitline segment potential of the '1' column will be greater than that of the '0' columns. As SA falls, the '1' column sense amplifier will be activated before the '0' column sense amplifiers. Until the '0' column sense amplifiers are activated, the capacitance seen by the driver is relatively low and SA decreases rapidly. Therefore, initial sensing by the '1' column sense amplifier occurs with SA decreasing rapidly. This degrades the sensitivity of the amplifier and increases the high bitline segment potential reduction during sensing.

3.2.2 Mostek

The Mostek 16K DRAM, presented in 1977 [37], [38], [39] became a de facto industry standard. The DRAM employed the same double-polysilicon cell structure used by Intel. It required three power supplies: +12 V, +5 V, and -5 V. The memory consists of a single 16K array with 64 cells per bitline segment. Bitline segment capacitance is 800 fF. The 435 μm^2 cell provides a 40 fF storage capacitance. Chip area is about 20 mm^2.

The Mostek DRAM sense amplifier, shown in Figure 3.4, introduced the use of isolation devices to partially decouple the sense amplifier signal nodes from the bitline

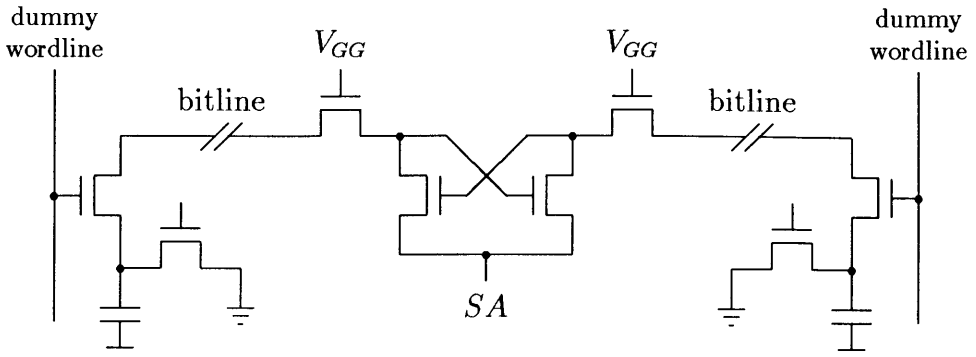

Figure 3.4: Mostek 16K DRAM Sense Amplifier

segments. The gates of the isolation devices are tied to an internal 16 V supply, V_{GG}.

During signal development, the bitline segment capacitance and the sense node capacitance are in series. Thus, the effective signal development time constant is small even though the isolation device resistance is substantial. During the sensing operation, the bitline segment capacitance and the isolation device resistance are in series, reducing the effective capacitance of the sense amplifier signal nodes and therefore improving amplifier speed and sensitivity.

The bitlines are precharged to V_{DD} (+12 V). Dummy storage capacitors, with half the ordinary cell capacitance, are precharged to ground. The appropriate dummy wordline is activated along with the selected wordline. After signal development is complete, the shared latch node, SA, is slowly pulled down. As the low signal node potential falls, the gate-source voltage of the isolation device separating the signal node and the bitline segment increases. As a result, the effective resistance of the device decreases, helping the sense amplifier pull the low-level bitline down.

All 16K and higher density DRAMs use address multiplexing. After the row address is received, the selected row is accessed and the sense amplifiers are activated. Later, after the column address is received, the column I/O circuitry either reads

from or writes to the selected sense amplifier. Thus, internally, write cycles amount to read-modify-write cycles.

In 4K DRAMs and many 16K DRAMs, column I/O circuitry is placed on one side of the arrays, providing access to only one side of the sense amplifiers. Sense amplifiers must include load devices in order to write '1' potentials to bitline segments opposite the column I/O circuitry. Inherent in the use of enhancement load devices is a speed-power tradeoff.

In the Mostek 16K DRAM, column I/O circuitry is placed between the sense amplifiers and the storage cell arrays. Access is provided to both sides of the sense amplifiers. Load devices are not needed to perform writes. The speed-power tradeoff is avoided, resulting in higher write speed and lower power dissipation [38].

Placement of the column I/O circuitry between the sense amplifiers and the memory arrays lengthens the bitlines somewhat, increasing bitline capacitance. In addition, since the column address lines must cross the bitlines, extreme care must be exercised to avoid destroying the small signals provided by the memory array.

Since load devices are not used during sensing, sense amplifier power dissipation is very low. However, the latch node potential must be reduced sufficiently slowly to prevent significant reduction of the high bitline potential.

3.3 64K DRAM Generation

The 64K DRAM Generation manifests many design variations. A key design problem was maintaining adequate sense signals. 5 V- only DRAMs superseded designs requiring multiple external power supplies. The elimination of high voltage V_{DD} supplies reduced the difference between stored '1' and '0' potentials. The elimination of substrate bias supplies necessitated use of on-chip voltage generators to bias the substrate. Several designs abandoned diffused bitline cells in favor of lower capacitance metal bitline cells. Many designs employed folded bitlines. Wordlines were often bootstrapped to enable storage of a V_{DD} as the '1' potential. Particle-induced soft errors were a major design problem [20]. Word and column redundancy were introduced to improve yield [40], [41].

3.3.1 IBM

The IBM 64K DRAM, presented in 1979 [42], employs unique processing technology and sense amplifier circuitry. Volume production of the chip began in January 1978 [43]. The DRAM is built using a polysilicon field shield, metal gate technology. The cell employs metal wordlines and diffused bitlines. Three power supplies are required: +8.5 V (V_{DD}), +4.25 V, and -2.2 V. The cell and chip area are 166 μm^2 and 36.6 mm^2, respectively. The memory is divided into two 32K blocks. Each block has 256 bitlines and 128 wordlines. Each bitline segment serves 64 cells.

The sense amplifier circuit is shown in Figure 3.5. It is based on the cross-coupled charge-transfer sense amplifier presented by Heller in 1979 [44]. Cross-coupled charge-transfer devices separate the bitline segments from the second cross-coupled pair. At the end of a chip cycle, $PC1$ is pulsed high, shorting all the bitlines together through the balance bus, $BBUS$. $PC2$ is then pulled up sufficiently high to precharge the

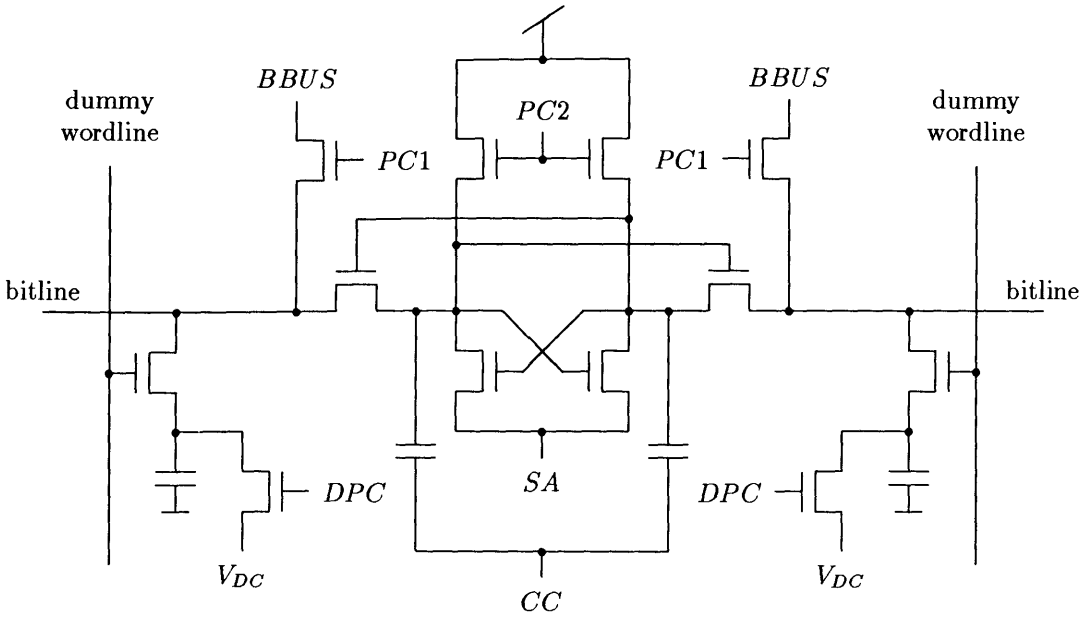

Figure 3.5: IBM 64K DRAM Sense Amplifier

bitlines to V_{DD} minus the V_T of their respective charge-transfer devices. The dummy storage capacitors are precharged to V_{DC}. The precharge is terminated at the end of the minimum cycle time. This prevents drops in V_{DD} from trapping the bitlines at a high potential.

At the beginning of a read cycle, CC and $PC1$ are low. Activation of the wordline and dummy wordline initiate sense node signal development. CC slowly rises to V_{DD}, amplifying the signal through the cross-coupled charge-transfer devices. SA is then pulled down, latching the datum.

The sense amplifier is capable of detecting extremely small signals and is insensitive to most device and capacitance mismatches, including threshold variations. While other 64K DRAMs required more complex processing technology with lower C_{BT}/C_S ratios, the IBM DRAM was produced with a relatively simple process. The C_{BT}/C_S ratio of the IBM DRAM is almost 30.

While much more sensitive than conventional sense amplifiers, the cross-coupled charge-transfer sense amplifier is also much slower. The rise time of the CC pulse during initial signal amplification is 85 ns. When precharging the bitlines the bucket devices operate in a slow source-follower configuration. The IBM 64K DRAM has a 440 ns access time and a 980 ns cycle time.

3.3.2 Texas Instruments

The Texas Instruments 64K DRAM, first published in 1978 [45], [46], used a double-polysilicon cell structure similar to those commonly used in 16K DRAMs. The chip operates from a single 5 V power supply. In contrast with most other 5 V- only 64K DRAMs, the TI DRAM employs a grounded substrate. The memory is organized as a single block with 256 sense amplifiers and 256 wordlines. Each sense amplifier serves 128 cells. Cell and chip area are approximately 170 μm^2 and 22 mm^2, respectively.

The TI 64K DRAM sense amplifier circuit is shown in Figure 3.6. Bitlines are precharged to V_{DD}. When the wordline and dummy wordline are activated, $PC2$, $R1$, and $R2$ are low. T is high. After signal development is complete, T dips low, partially isolating the sense nodes from the bitline capacitances. SA is then pulled down to amplify the signal. T goes high and the low potential bitline is pulled to ground by the cross-coupled pair. Finally, the high bitline segment is restored to V_{DD}.

The high potential bitline segment is restored to V_{DD} using active loads. First, $R1$ goes high, grounding the gate of the restore transistor on the low side of the sense amplifier and charging the gate of the restore transistor on the high side. $R1$ then goes low enough to isolate the gates of both restore transistors from the bitline segments. $R2$ is pulled up, pushing the gate of the restore transistor on the high side above V_{DD} and charging the high potential bitline segment to V_{DD}. The wordlines are bootstrapped above V_{DD}, writing a maximum (V_{DD}) '1' potential.

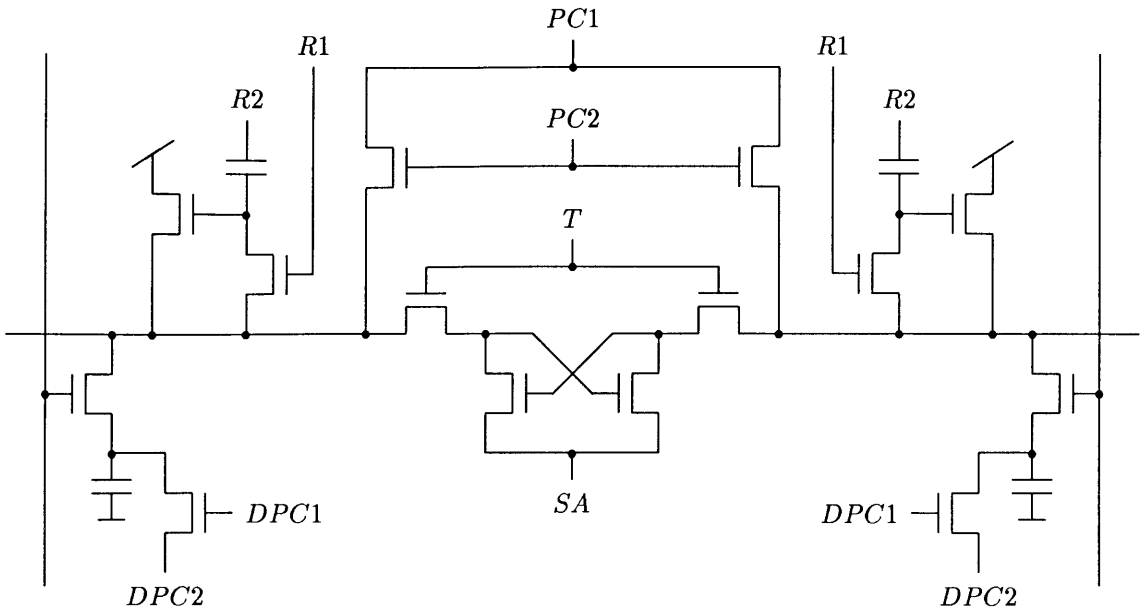

Figure 3.6: TI 64K DRAM Sense Amplifier

Active loads maximize the final bitline segment potential difference without causing static power dissipation. However, they require substantial increases in the complexity and area of the sense amplifier. Two clock signals and several devices are required. Unlike static load circuits, active load circuits do not allow single ended write access. Column I/O circuitry must access both sides of the sense amplifiers.

In general, the TI sense amplifier design seems to optimize sense amplifier performance at the expense of substantial layout area and complexity. Such a strategy may be justified by characteristics of the storage cell array. More specifically, if the initial signal presented to the sense amplifier is relatively small, perhaps as a result of a high C_{BT}/C_S ratio, steps taken to maximize the difference between stored '0' and '1' potentials and to improve the sensitivity of the sense amplifier may be necessary.

3.3.3 Fairchild

The Fairchild 64K DRAM, presented in 1980 [47], uses a variation of the folded bitline array architecture. The memory is divided into four 16K blocks. Each block is divided into two sections with 64 shared sense amplifiers placed between the sections. Each section contains 128 wordlines and 128 bitline segments. Thus, each bitline segment serves only 64 cells.

The Fairchild DRAM employs a double-polysilicon cell with polysilicon wordlines and metal bitlines. Cell area is 170 μm^2. Cell storage capacitance is 50 fF. Bitline segment capacitance is 600 fF. The chip requires a single 5 V power supply. Chip area is 23.5 mm^2.

The Fairchild 64K sense amplifier, published by Barnes and Chan in 1980 [48], is shown in Figure 3.7. Depletion devices are used to isolate bitline segments from the sense nodes. PC rises to about 7 V to precharge the bitlines to V_{DD}. For simplicity, assume cells on the selected wordline are connected to one of the top bitline segments. $T0$ goes low, isolating the bottom bitline segments from the sense nodes. The wordline and dummy wordline rise to 7 V, allowing complete equalization of the storage capacitor and bitline segment potentials. After signal development is complete, $T1$ goes low to temporarily isolate the bitline segments from the sense nodes. Next, the boost capacitor clock, CC, rises, amplifying the signal and pushing the sense nodes above V_{DD}. When preamplification is complete, the latch node, SA, is pulled down, latching the datum. $T0$ and $T1$ rise, allowing the flip-flop to pull the low level bitline segment to ground.

The shared sense amplifier architecture has several important features. For a given number of bitline segments, the architecture halves the number of sense amplifiers required compared with the conventional folded bitline architecture. For a given

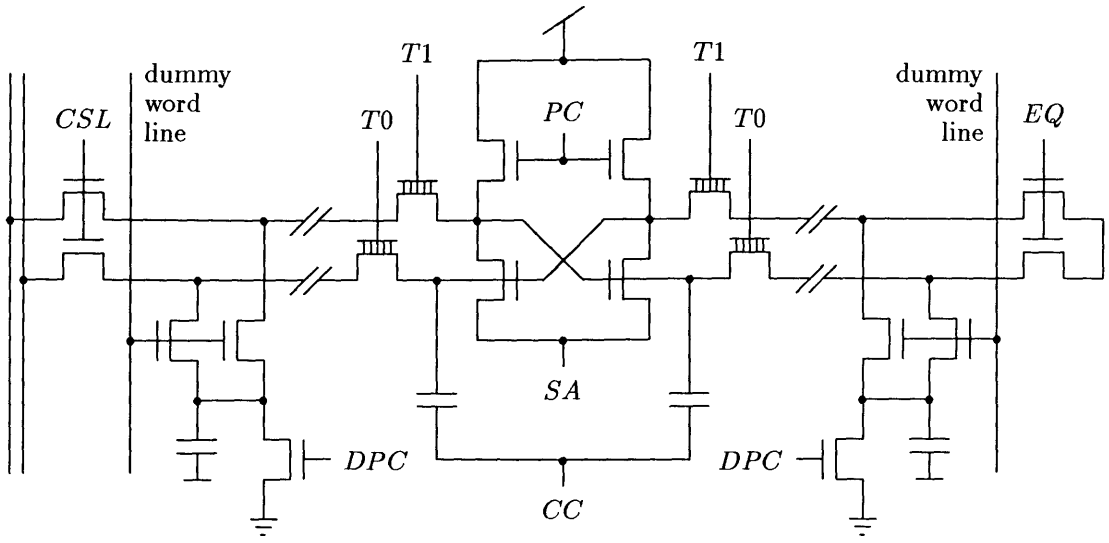

Figure 3.7: Fairchild 64K DRAM Sense Amplifier

number of sense amplifiers, the shared sense amplifier architecture halves the number of cells per bitline segment, reducing the C_{BT}/C_S ratio. The architecture requires the use of isolation devices. Finally, since column I/O circuitry accesses bitline segments on only one side of the sense amplifier, all four bitline segments must be active when reading from or writing to cells on bitline segments opposite the I/O circuitry.

The preamplification scheme insures that the high-level bitline potential will not fall below V_{DD}. Since the wordlines are bootstrapped to 7 V, full V_{DD} '1' potentials will be stored. In addition, preamplification allows relatively fast pull-down of the latching node without significantly degrading amplifier sensitivity. Preamplification speed, rather than latching speed is critical to sensitivity.

The preamplification circuit requires relatively little layout area. Only two additional devices per sense amplifier are needed: the two boost capacitors. Active restore circuits require six devices. The preamplifier circuit requires one clock signal. Active restore circuits require two.

Use of depletion isolation devices avoids the need for gate potential above the high level bitline potential. However, the provision of depletion devices in the DRAM process was undoubtedly warranted by other considerations.

3.4 256K DRAM Generation

By the mid-1980s, features added to improve performance had made NMOS processes nearly as complex as CMOS processes. CMOS offers several advantages [49] over NMOS including lower power dissipation, better clock drivers, and reduced circuit complexity. Though most 256K DRAMs employ NMOS technology, several use CMOS.

Almost all 256K DRAMs operate from a single 5 V power supply. Most employ a Hi-C [50], [51] storage cell. Polycide or silicide wordlines are commonly used to reduce wordline delay.

3.4.1 Hitachi

The Hitachi 256K NMOS DRAM, published in 1984 [52], [53], typifies the 256K generation. A Hi-C planar storage capacitor is used with polycide wordlines and folded metal bitlines. The memory is divided into four 64K blocks. Cell and chip area are 95 μm^2 and 44.1 mm^2, respectively.

The Hitachi 256K DRAM sense amplifier is shown in Figure 3.8. Bitlines are precharged to V_{DD}. During signal development, the wordline is boosted above V_{DD} to obtain maximum signal. After signal development is complete, the latch node, SA, is pulled down, latching the datum. $R1$ goes high, discharging the low-level bitline segment restore device gate and charging the high-level bitline segment restore device gate. Next, $R1$ goes high, pushing the high-level restore device gate above V_{DD}. The restore device charges the high-level bitline segment to V_{DD}.

A full V_{DD} '1' potential can be stored in NMOS DRAMs either by employing capacitors to boost the bitline segment potentials or by using active restore circuits. The Hitachi sense amplifier employs an active restore circuit, avoiding degradation

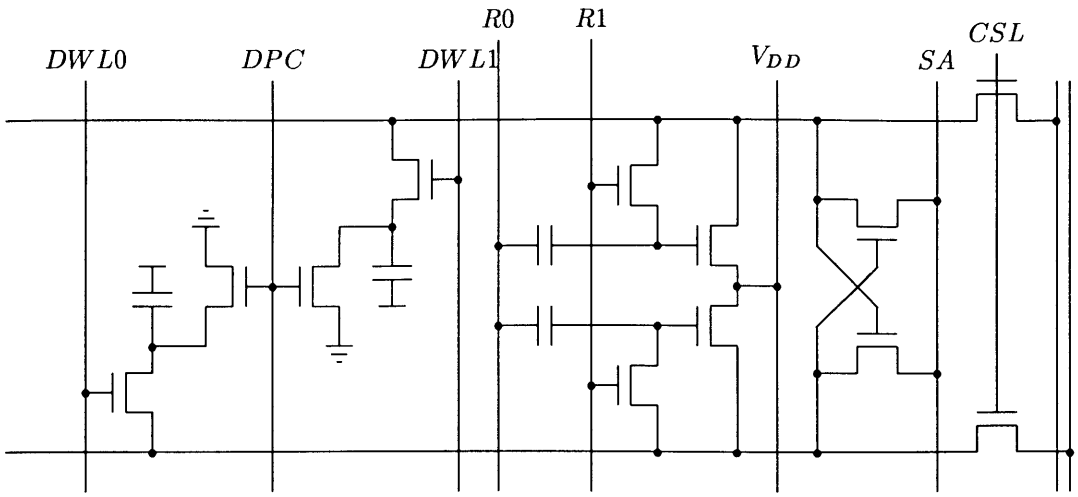

Figure 3.8: Hitachi 256K DRAM Sense Amplifier

of the transfer ratio and guaranteeing the restored '1' level will always be V_{DD}, never higher nor lower.

Aside from the active restore circuits, the Hitachi sense amplifier is quite simple. Isolation devices are not employed, saving area and eliminating the need for a clock signal.

3.4.2 Intel

The Intel 256K DRAM, presented in 1984, [54], [55], [56], employs n-well CMOS technology. p-channel Hi-C cells are placed in an n-well. The n-well isolates the cells from minority carriers in the substrate, reducing thermal leakage and particle-induced soft errors. The 70 μm^2 cells, with polysilicon wordlines and folded metal bitlines, have 55 fF storage capacitors. The memory is divided into eight 32K blocks, each with 256 wordlines and 128 sense amplifiers. The sense amplifiers, placed in the middle of the blocks, each serve four bitline segments. Chip area is about 41 mm^2.

The Intel sense amplifier is shown in Figure 3.9. CMOS technology allows active

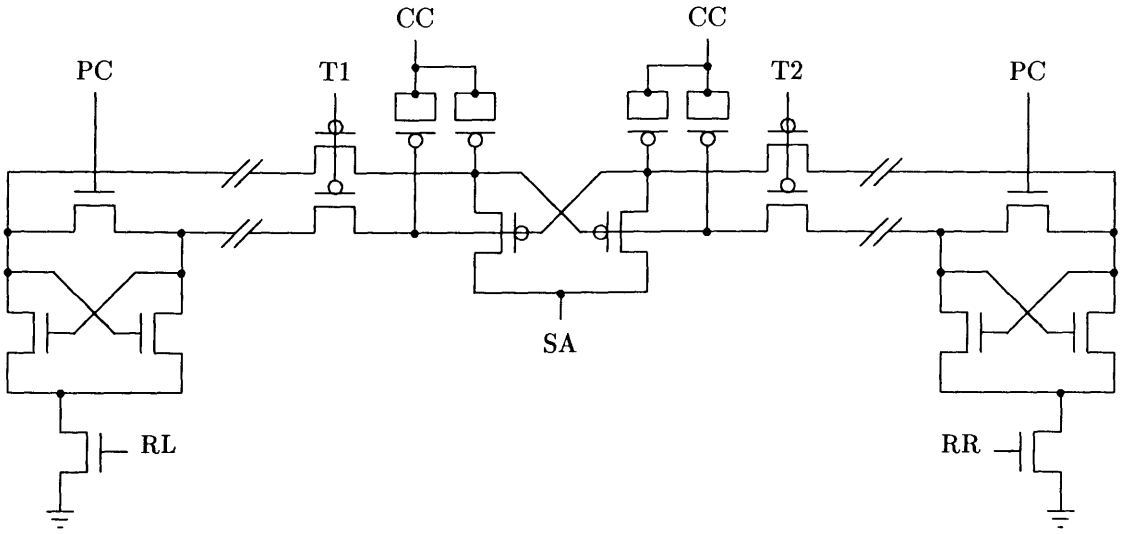

Figure 3.9: Intel 256K DRAM Sense Amplifier

bitline restoration using a simple cross-coupled pair. Bitline segments are held at V_{DD} or ground until the beginning of a cycle. Then the segments are shorted together, precharging them to $1/2\,V_{DD}$. $T1$ or $T2$ goes low to isolate the unselected block half from the p-channel cross-coupled pair. After signal development is complete, the cross-coupled pair is isolated from both bitline segment pairs. CC is activated, boosting the signal node potentials and amplifying the signal. Then the p-channel latch is set. Finally, the n-channel cross-coupled pairs are activated.

Most 16K and higher density NMOS DRAM sense amplifier designs precharge bitlines to V_{DD}. Precharging the bitlines to a lower potential reduces the overdrive on the n-channel latch, decreasing the rate at which the low-level bitline can be pulled to ground. Restoring a bitline precharged below V_{DD} to V_{DD} requires either static loads or active restore circuits. Static loads dissipate much power. Active restore circuits require several sensitive clock signals, use a large amount of area, and may not have very good current driving capabilities.

Many disadvantages of low bitline precharge potentials do not apply to CMOS designs. In CMOS DRAMs, '0' and '1' potentials can be restored using a cross-coupled pair. Restoration can begin before the low-level bitline segment reaches ground. Intel used half-V_{DD} sensing to eliminate the need for dummy cells and reduce bitline charging and discharging power. Other benefits of half-V_{DD} sensing are detailed in [57].

The Intel sense amplifier uses a p-channel cross-coupled pair to latch the datum. Since the bitlines are precharged to $1/2\ V_{DD}$, an n-channel cross-coupled pair could have been used to latch the signal, with p-channel pairs employed to restore the '1' potentials. Since n-channel devices have greater mobility, using n-channel devices of equal area as the p-channel devices should reduce the offsets due to process variations. The advantage of using p-channel devices in the Intel sense amplifier is a reduced soft error rate. Because the Intel DRAM is fabricated using an n-well process with a p-channel array, the p-channel cross-coupled device pair can be embedded in the array n-well. The n-well acts as a barrier to carriers generated in the substrate.

The two bitline segment pairs are serviced by separate n-channel cross-coupled pairs. Instead, a single n-channel cross-coupled pair could probably be placed in the center of the blocks, along with the p-channel cross-coupled pair. Use of separate n-channel pairs allows activation of the restore devices to be staggered, reducing peak current.

3.5 1M DRAM Generation

The 1M DRAM generation represents the midpoint of the transition from NMOS to CMOS technologies. Almost all CMOS 1M DRAMs precharge bitlines to 1/2 V_{DD}. To reduce wordline delays, 1M DRAMs commonly employ polysilicon wordlines strapped by metal bypass wordlines. Polycide is often used for bitlines. To maintain adequate charge capacity, Hi-C planar cells are used with 1/2 V_{DD} biased plates.

3.5.1 Toshiba

The Toshiba 1M CMOS DRAM, presented in 1985 [58], [59], [60], is typical of 1M CMOS DRAMs. The 34.2 μm^2 planar cell provides a 42 fF storage node. The cell plate is biased to 1/2 V_{DD}. Polycide bitlines and polysilicon wordlines are employed. The polysilicon wordlines are connected to metal bypass wordlines at 64-bit intervals. The folded bitline architecture is used; bitline segments each serve 128 cells. Chip area is 62.5 mm^2.

The Toshiba sense amplifier is shown in Figure 3.10. At the beginning of the cycle, a pair of dummy wordlines, $DWL0$ and $\overline{DWL0}$ or $DWL1$ and $\overline{DWL1}$, are selected. Upon wordline activation, one of the selected dummy wordlines goes from V_{PC} to V_{DD}, the other goes from V_{PC} to ground. The dummy wordlines couple to the bitline segments through capacitors with approximately half the capacitance of the cell storage capacitor. Thus, if V_{PC} drifts above or below 1/2 V_{DD} the change in potential caused by activation of the dummy wordlines will compensate, preventing signal loss. After the cells are restored, EQ goes high, precharging the bitlines. A voltage generator is tied to V_{PC}.

In a 1/2 V_{DD} precharge scheme, equalizing the bitlines at the end of the cycle risks signal loss. If a long time elapses before the beginning of the next cycle terminates

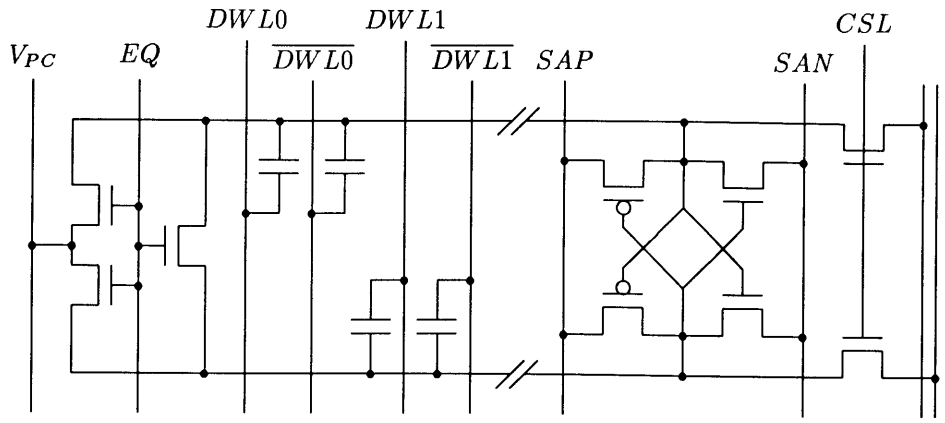

Figure 3.10: Toshiba 1M DRAM Sense Amplifier

the precharge period, the bitline potentials may drift from $1/2\ V_{DD}$. If dummy cells are not used or if the dummy wordlines are activated through the entire precharge interval, an offset may be introduced. If the bitline and dummy storage capacitor potentials move above $1/2\ V_{DD}$, '1' signals will be reduced. If the potentials move below $1/2\ V_{DD}$, '0' signals will be reduced. If the bitlines are held at V_{DD} and ground until the beginning of the next cycle, access time will suffer.

The complementary capacitor-coupled dummy cell and the bitline precharge voltage generator prevent signal loss while allowing bitline precharge to take place at the end of the cycle. The generator suppresses fluctuations in bitline potentials during precharge. The complementary capacitor-coupled dummy cell adjusts the reference bitline segment potential during signal development to compensate for precharge potential variations.

There are important drawbacks to the Toshiba sense amplifier design. The bitline precharge voltage generator undoubtedly requires significant power and layout area. Process variations and supply voltage fluctuations may significantly degrade the accuracy of the generator. Traditional dummy cell structures are very much like the

storage cells structures. As a result, cell process variations are often compensated by similar variations in the dummy cells. The complementary capacitor-coupled dummy cell structure is quite different from the storage cell structure and therefore may not offer the same degree of tracking.

3.5.2 Texas Instruments

The Texas Instruments 1M CMOS DRAM, presented in 1986, [61], [62], employs a unique architecture to accommodate a unique trench cell and reduce the C_{BL}/C_S ratio. The memory is divided into four 256K blocks, each with 512 rows and 512 columns. The trench cell employs diffused bitlines and polycide wordlines. Each column contains eight diffused bitline segments, placed end-to-end. Each segment connects to 32 cells. Two metal bitlines run parallel to the diffused bitline segments. A segment select line runs perpendicular to the bitlines at each inside bitline segment end. When the segment select line is activated, one segment is connected to each metal bitline.

The trench storage capacitance is 50 fF. Bitline segmentation gives a C_{BL}/C_S ratio of only 8. Cell area and chip area are approximately 21 μm^2 and 50 mm^2, respectively.

The Texas Instruments sense amplifier, shown in Figure 3.11, uses full-size dummy storage capacitors, precharged to V_{DC}. Bitline segments are precharged to 1/2 V_{DD}. Before the wordline and dummy wordline are pulled up, the isolation device clock, T, and the appropriate segment select line are activated. After signal development is complete, T falls, isolating the flip-flop from the bitlines. After the selected sense amplifier is read from or written to, the isolation device clock, the selected segment line, and the wordline are bootstrapped above V_{DD}, restoring the cells to full V_{DD} and ground potentials.

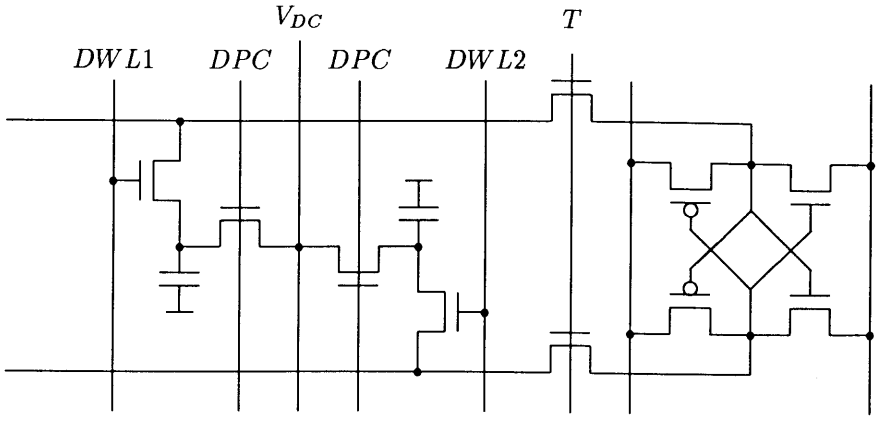

Figure 3.11: TI 1M DRAM Sense Amplifier

While not strictly required with 1/2 V_{DD} precharged bitlines, the use of independently precharged dummy cells prevents signal loss due to variations in the bitline precharge potential. Access time can be minimized by initiating bitline precharge at the end of the cycle.

A voltage generator is employed to establish the dummy storage capacitor precharge potential, V_{DC}. Because of differences in transfer device overdrive, in an n-channel array '0' signals develop faster than '1' signals. The TI DRAM uses a precharge potential slightly below 1/2 V_{DD} allowing sensing to begin before signal development is entirely complete. Access time is reduced with minimal signal loss.

Like the shared sense amplifier architecture, bitline segmentation increases the number of bitline segments per sense amplifier. Bitline segmentation requires two bitline levels, increasing array complexity. The shared sense amplifier architecture requires active use of unselected bitline segments to transmit data to the I/O circuitry, increasing bitline charging and discharging power.

The use of isolation devices allows the sense amplifier to be read before the bitlines are driven to full '0' and '1' potentials. Access time is reduced, but at the cost of

additional layout area and circuit complexity.

3.6 4M DRAM Generation

To achieve adequate storage cell charge capacity, 4M DRAMs employ either trench or stacked capacitor cells. Almost all 4M DRAMs use CMOS technologies. Metal bypass wordlines are commonly employed. Sense amplifier designs are generally similar to 1M CMOS DRAM designs.

3.6.1 Toshiba

The Toshiba 4M DRAM design, presented in 1986 [63], [64], uses a twin-tub CMOS process. The 17.4 μm^2 trench cells are placed in p-wells on a p-substrate. Cell storage capacitance is 40 fF. Folded bitlines are formed using polycide. Polysilicon wordlines are strapped with metal bypass wordlines. Bitline segment capacitance is 600 fF. The memory is divided into sixteen 512K blocks. Chip area is 137 mm^2. The DRAM includes an on-chip voltage converter. The chip can be operated either from the external 5 V supply or from an internal 3.5 V supply controlled by the voltage converter. A metal mask option is used to change between supply options.

The 4M DRAM sense amplifier is shown in Figure 3.12. Bitlines are precharged to $1/2\ V_{DD}$ at the end of the cycle. Full-capacitance dummy cells are also precharged to $1/2\ V_{DD}$. Use of dummy cells reduces the sense amplifier susceptibility to variations in the bitline precharge voltage.

The n-channel flip-flops are activated before the p-channel flip-flops. Isolation devices, with gates tied to V_{DD}, separate the bitline segments and the n-channel flip-flops. The isolation devices reduce the effective initial signal node capacitances, speeding signal amplification. The p-channel cross-coupled pair is connected directly to the bitlines, allowing full V_{DD} '1' level restoration without bootstrapping the isolation device gates above V_{DD}.

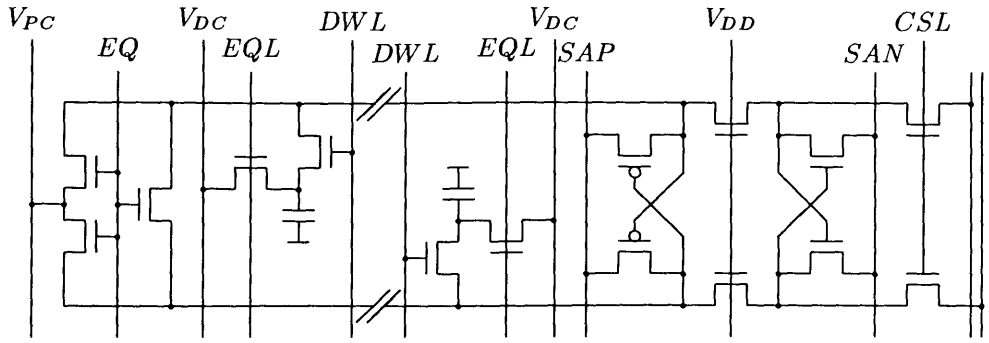

Figure 3.12: Toshiba 4M DRAM Sense Amplifier

Clocking the isolation device gates would allow further reduction of the effective signal node capacitance and would allow quick development of a full V_{CC} signal. However, the necessary clock timing and driver circuitry would likely increase chip area and power dissipation.

3.7 16M DRAM Generation

While 16M DRAMs have not yet been produced in volume, several designs have been published. All employ CMOS technology and either stacked capacitor or trench cells.

Issues of increased importance in 16M and higher density DRAM designs include signal development time, bitline to bitline coupling, and sense amplifier layout. New design approaches have been introduced in response to these issues. Instead of considering specific 16M DRAM sense amplifier designs, new design approaches which seem especially relevant to 64M DRAM design will be examined.

3.7.1 Twisted Bitline Architecture

The reduced bitline pitch of 16M and higher density DRAM cells results in high bitline to bitline capacitance. This capacitance introduces noise during both signal development and signal amplification.

Figure 3.13 shows a folded bitline model including bitline coupling capacitance. C_{BG} is the total bitline segment to ground capacitance. C_{BB} is the total capacitance between neighboring bitlines.

Assuming the states of all odd columns are identical and the states of all even columns are identical, the bitline segment charges after signal development is complete are given by

$$\begin{aligned} Q_{BLO} &= \Delta V_{odd} C_{BB} + V_{BLO} C_{BG} + (V_{BLO} - V_{\overline{BLE}}) C_{BB}, \\ Q_{\overline{BLO}} &= -\Delta V_{odd} C_{BB} + V_{\overline{BLO}} C_{BG} + (V_{\overline{BLO}} - V_{BLE}) C_{BB}, \\ Q_{BLE} &= \Delta V_{even} C_{BB} + V_{BLE} C_{BG} + (V_{BLE} - V_{\overline{BLO}}) C_{BB}, \\ Q_{\overline{BLE}} &= -\Delta V_{even} C_{BB} + V_{\overline{BLE}} C_{BG} + (V_{\overline{BLE}} - V_{BLO}) C_{BB}, \end{aligned} \tag{3.1}$$

where V_{BLE}, $V_{\overline{BLE}}$, V_{BLO}, and $V_{\overline{BLO}}$ are the bitline segment potentials; $\Delta V_{even} \equiv V_{BLE} - V_{\overline{BLE}}$; and $\Delta V_{odd} \equiv V_{BLO} - V_{\overline{BLO}}$.

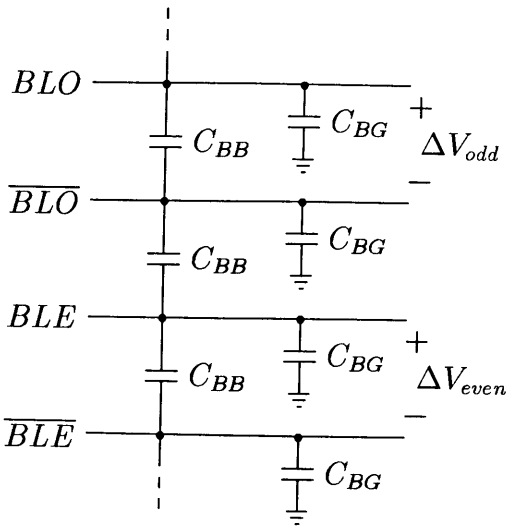

Figure 3.13: Folded Bitline Model

The charge differences between bitline segment pairs must equal the signal charge. Thus, the odd and even signal charges are given by

$$Q_{SO} = Q_{BLO} - Q_{\overline{BLO}} = 2\Delta V_{odd}C_{BB} + \Delta V_{odd}C_{BG} + (\Delta V_{odd} + \Delta V_{even})C_{BB},$$
$$Q_{SE} = Q_{BLE} - Q_{\overline{BLE}} = 2\Delta V_{even}C_{BB} + \Delta V_{even}C_{BG} + (\Delta V_{odd} + \Delta V_{even})C_{BB}. \tag{3.2}$$

Solving these equations for ΔV_{odd} and ΔV_{even} gives

$$\Delta V = \frac{Q_S}{C_{BG} + 4C_{BB}}, \quad \text{if } Q_{SO} = Q_{SE}, \tag{3.3}$$

and

$$\Delta V = \frac{Q_S}{C_{BG} + 2C_{BB}}, \quad \text{if } Q_{SO} = -Q_{SE}, \tag{3.4}$$

where

$$\Delta V \equiv |\Delta V_{odd}| = |\Delta V_{even}| \tag{3.5}$$

and

$$Q_S \equiv |Q_{SO}| = |Q_{SE}|. \tag{3.6}$$

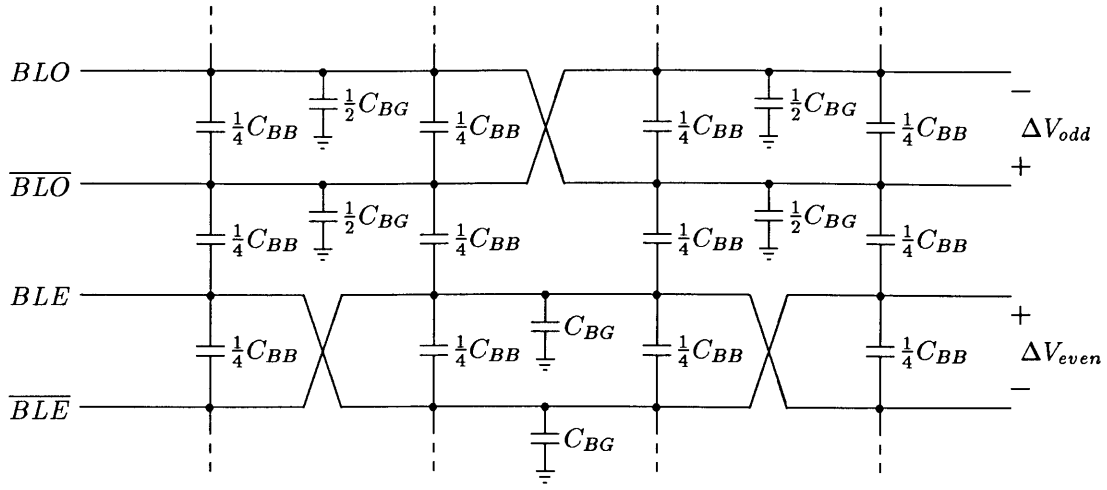

Figure 3.14: Twisted Bitline Model

Thus, if the stored patterns are uniform, bitline coupling capacitance increases the total effective bitline capacitance by $2C_{BB}$ in the best case and $4C_{BB}$ in the worst case.

Noise resulting from bitline coupling during signal amplification is difficult to analyze. It depends not only on the particular bitline potentials [65], but also on details of sense amplifier operation [66], [67]. Analyses indicate that the noise produced during signal amplification may be more than twice as large as the noise produced during signal development [68], [66].

Figure 3.14 shows a twisted bitline model including bitline coupling capacitance. The twisted bitline architecture, introduced by Yoshihara *et al.* [69] and Aoki *et al.* [70], significantly reduces bitline coupling noise. It has been employed in 16M DRAMs [70], [68], [71], [72], [73].

Assuming a uniform pattern, the bitline segment charges after signal development

is complete are given by

$$
\begin{aligned}
Q_{BLO} &= \Delta V_{odd} C_{BB} + V_{BLO} C_{BG} + (V_{BLO} - V_{\overline{BLE}}) C_{BB}/2 + (V_{BLO} - V_{BLE}) C_{BB}/2, \\
Q_{\overline{BLO}} &= -\Delta V_{odd} C_{BB} + V_{\overline{BLO}} C_{BG} + (V_{\overline{BLO}} - V_{BLE}) C_{BB}/2 + (V_{\overline{BLO}} - V_{\overline{BLE}}) C_{BB}/2, \\
Q_{BLE} &= \Delta V_{even} C_{BB} + V_{BLE} C_{BG} + (V_{BLE} - V_{\overline{BLO}}) C_{BB}/2 + (V_{BLE} - V_{BLO}) C_{BB}/2, \\
Q_{\overline{BLE}} &= -\Delta V_{even} C_{BB} + V_{\overline{BLE}} C_{BG} + (V_{\overline{BLE}} - V_{BLO}) C_{BB}/2 + (V_{\overline{BLE}} - V_{\overline{BLO}}) C_{BB}/2.
\end{aligned}
\tag{3.7}
$$

The odd and even signal charges are given by

$$
\begin{aligned}
Q_{SO} &= Q_{BLO} - Q_{\overline{BLO}} = 3\Delta V_{odd} C_{BB} + \Delta V_{odd} C_{BG} \\
Q_{SE} &= Q_{BLE} - Q_{\overline{BLE}} = 3\Delta V_{even} C_{BB} + \Delta V_{even} C_{BG}
\end{aligned}
\tag{3.8}
$$

Solving these equations for ΔV_{odd} and ΔV_{even} gives

$$
\Delta V = \frac{Q_S}{C_{BG} + 3C_{BB}}, \tag{3.9}
$$

where

$$
\Delta V \equiv |\Delta V_{odd}| = |\Delta V_{even}| \tag{3.10}
$$

and

$$
Q_S \equiv |Q_{SO}| = |Q_{SE}|. \tag{3.11}
$$

Thus, if the stored patterns are uniform, bitline coupling capacitance increases the total effective bitline capacitance by $3C_{BB}$, independent of the stored pattern. The twisted bitline architecture reduces the worst case total effective bitline capacitance from $C_{BG} + 4C_{BB}$ to $C_{BG} + 3C_{BB}$, compared to the conventional folded bitline arrangement.

The impact of twisted bitlines on coupling noise during signal amplification is much more significant. In the twisted bitline architecture, inter-pair coupling noise during signal amplification is canceled. The two bitline segments of each bitline pair couple equally with neighboring bitline segments.

The twisted bitline architecture requires twice the number of dummy cells and dummy wordlines as the folded bitline architecture. This not only increases chip area, but also increases the complexity of the dummy wordline decoder circuitry. Extra area is also required for the "twists."

The additional area required by the twisted bitline architecture depends on the technology employed. In the Hitachi 16M DRAM [70], [68], first level metal is used to twist the silicide bitlines. First level metal is also used to bypass the polysilicon wordlines. The twists increase total chip area 7 percent. In the Oki [73] and Mitsubishi [71], [72] DRAMs, special local interconnect levels are used to twist the bitlines, allowing dummy cells to be placed under twists. In the Oki DRAM, employing twisted bitlines increases chip area 2.6 percent. In the Mitsubishi DRAM, overhead is reportedly limited to 0.1 percent.

3.7.2 V_T-Derived Bitline Precharge Potentials

Almost all 1M and 4M CMOS DRAMs employ a $1/2\ V_{DD}$ bitline precharge potential. However, in 16M and higher density DRAMs, a $1/2\ V_{DD}$ precharge potential may result in long signal development time. Two factors contribute to the reduction in relative signal development speed: delayed initiation of charge transfer due to wordline rise time and low transfer device overdrive.

In 16M and higher density DRAMs, wordline rise time can be quite large. In n-channel arrays, '1' cell charge transfer does not begin until the activated wordline reaches $1/2\,V_{DD} + V_T$. In p-channel arrays, '0' cell charge transfer does not begin until the activated wordline reaches $1/2\ V_{DD} - V_T$. The delay between wordline selection and the initiation of charge transfer increases access time.

The reduced internal voltages used in 16M and higher density DRAMs result in lower transfer device overdrive. Charge transfer speed is limited by transfer device

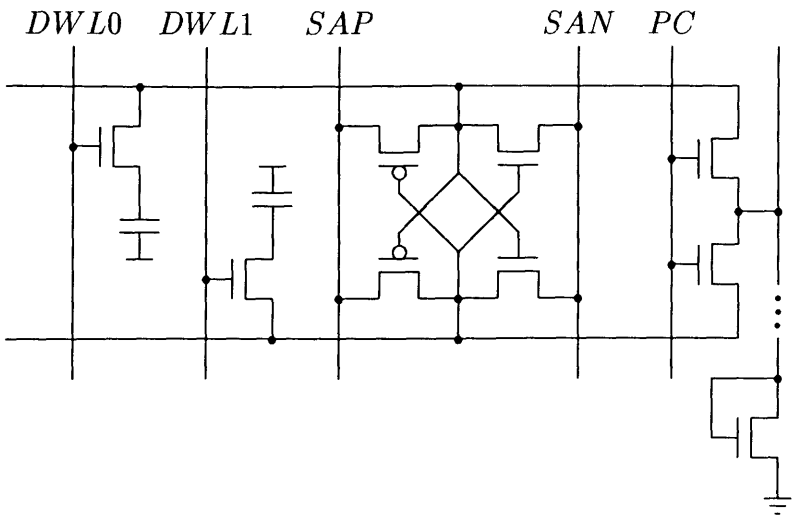

Figure 3.15: NTT 16M DRAM Sense Amplifier

current. Low transfer device overdrive produces low currents, slowing signal development.

The NTT 16M DRAM presented by Mano *et al.* in 1987 [74] employs *n*-channel arrays. The NTT sense amplifier circuit, shown in Figure 3.15, precharges bitline segments to V_T. Mano *et al.* refer to the approach as "pseudo-grounded bitline initialization." Compared to 1/2 V_{DD} bitline precharge approaches, the NTT approach achieves earlier initiation of '1' cell charge transfer and greater transfer device overdrive, reportedly decreasing access time by 10 ns.

NTT chose the V_T bitline precharge potential over precharging bitline segments to ground. While precharging the bitline segments to ground would further reduce signal development time, it would also increase the susceptibility of the array to wordline noise. In *n*-channel arrays, as the bitline precharge potential is reduced, the difference between the bitline precharge potential and the wordline "off" potential decreases. As a result, wordline noise will result in greater subthreshold currents in '1' cell transfer devices.

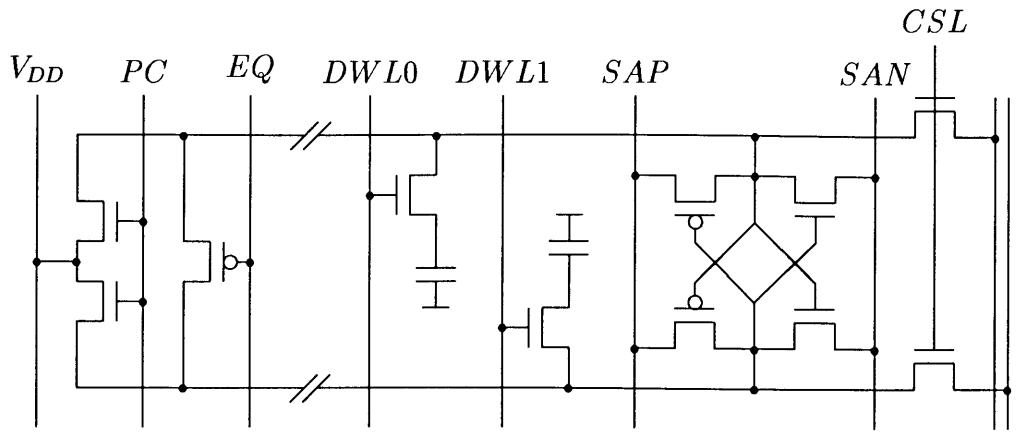

Figure 3.16: 2/3 V_{DD} Sense Amplifier Circuit (from [75])

In 1988 Dhong *et al.* employed the same basic approach as Mano *et al.* in sense amplifiers designed for use with a *p*-channel array [75]. One of the circuits is shown in Figure 3.16. Bitline segments are precharged to $V_{DD} - V_T$. Since $V_{DD} - V_T \approx 2/3\,V_{DD}$, Dhong *et al.* refer to the approach as "2/3 V_{DD}-Sensing."

The important difference between the circuits presented by Mano *et al.* and Dhong *et al.* is the method used to precharge the bitlines. In the Mano *et al.* design, a single diode-connected transistor must discharge all the bitlines to the precharge potential. In the Dhong *et al.* design, the precharge potential in each column is produced independently by transistors operating in a source-follower configuration.

In both circuits, the precise precharge potential will likely vary depending on the length of the precharge interval and the parameters of the precharge transistors. In the Dhong *et al.* design, local variations in precharge transistor characteristics may result in bitline precharge potential variations between different columns. This would cause signal amplification to begin at different times, increasing bitline coupling noise during sensing.

3.7.3 Sense Amplifier Pitch Doubling

With each new DRAM generation, cell dimensions have been reduced relative to feature sizes. As a result, sense amplifier pitch constraints have become increasingly tight. Using folded bitlines, the sense amplifier pitch constraint can be relaxed to four bitline pitches by placing sense amplifiers on both sides of each array. Several 16M DRAMs employ this technique [74], [71], [72], [76], [77].

This approach is likely to increase total sense amplifier area. Twice as many sense amplifier signal and/or supply buses are needed. In addition, particular care must be taken to prevent timing skews between sense amplifiers on opposite sides of each array.

Chapter 4

64M DRAM Technology and Performance Projections

Key technology features and performance specifications must be projected to facilitate 64M DRAM sense amplifier analysis. Estimates will be based primarily on published 16M DRAM parameters and historical trends.

16M DRAM chip areas generally range from 130 mm^2 to 160 mm^2. Typical cell areas range from 4 μm^2 to 5 μm^2. Based on the trends shown in Figures 1.8 and 1.9, 64M DRAM chip and cell areas should be around 200 mm^2 and 2 μm^2, respectively. While Tasch and Parker [78] predict significantly smaller 64M DRAM chip and cell areas, the 200 mm^2 and 2 μm^2 estimates are consistent with trend data published by Maes *et al.* [27], Lu [26], and Noble [25].

Folded bitline cells will likely be employed in most 64M DRAMs. Almost all published 1M and higher density DRAMs use folded bitlines. In addition, most published cells suitable for 64M DRAMs have folded bitlines.

The area of a folded bitline cell is equal to twice the product of the bitline segment and wordline pitches. Thus, to build a 2 μm^2 cell, the product of the pitches must be 1 μm^2. Since minimum wordline and bitline pitches are nearly equal, both pitches will probably be approximately 1 μm.

Minimum 16M DRAM n-channel device lengths range from about 0.5 μm to 0.7 μm. Minimum p-channel device lengths are usually about 0.2 μm greater. Gate insulator thickness generally falls within the 120 Å to 160 Å range. Based on the trend shown in Figure 1.10, 64M DRAM features should be roughly 1.4x smaller than 16M DRAM features. Thus, minimum 64M n-channel and p-channel device lengths will likely be about 0.4 μm and 0.5 μm, respectively. Gate insulator thickness will likely be around 100 Å.

Electric fields within devices must be limited to avoid hot electron effects, drain breakdown, and oxide breakdown [79], [80], [81], [82]. 16M DRAMs typically use a 5 V external supply, but operate most internal circuits with only 3-4 V. This preserves compatibility with standard 5 V components while limiting internal fields. At the 64M integration level, power dissipation considerations dictate a lower external power supply voltage. The JEDEC supply voltage standard for 64M DRAMs is 3.3 V [83]. This voltage will likely be used both for external supplies and internal circuits in most 64M DRAMs.

Subthreshold conduction limits reduction of device threshold voltages [82]. As the gate-source voltage of a device is decreased below the threshold voltage, device current does not cease. Instead, the current exponentially decreases. The gate voltage swing required to reduce the current by one decade is typically on the order of 100 mV. If device thresholds are too low, substantial current will flow through "off" devices, resulting in significant static power dissipation in peripheral circuits and charge leakage through the transfer devices in the array. Thus, 64M DRAM devices will probably not have significantly reduced threshold voltages. Typical nominal device thresholds may be approximately 0.7 V.

As DRAM cell areas are reduced, bitline to bitline coupling capacitance generally increases relative to total bitline capacitance [84], [85]. Figure 4.1 shows bitline

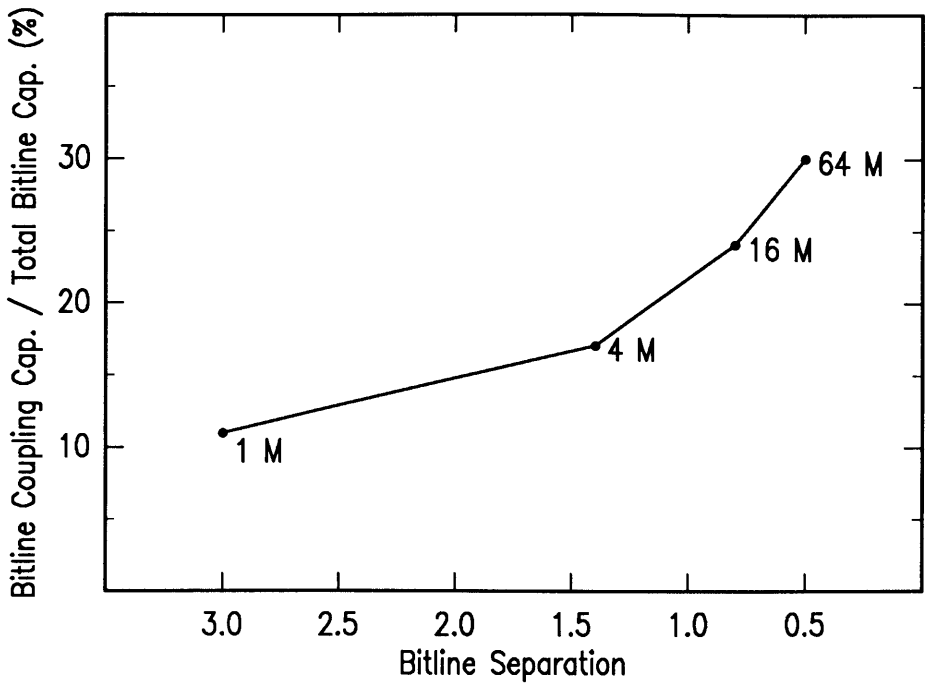

Figure 4.1: Bitline Coupling Capacitance (from [85])

coupling capacitance (defined as twice the bitline-to-bitline capacitance) as a fraction of total bitline capacitance. To build more compact cells, bitline spacing must decrease. Conductor resistance precludes drastic reduction of polycide line thickness. Electromigration considerations limit decreases in metal line thickness. Finally, even if the bitline thickness is significantly reduced, the fringe capacitance component will remain relatively large.

16M DRAM bitline capacitance per bit generally ranges from 1.5 to 2 fF. As shown in Figure 4.1, bitline to bitline coupling capacitance accounts for around 20-25 percent of the total capacitance. 64M bitline to ground capacitance will likely be around 0.8 fF per bit. Based on Figure 4.1, bitline to bitline capacitance should be about 0.2 fF per bit, assuming use of metal bitlines. With polycide bitlines, coupling capacitance can be more easily reduced through decreases in line width and thickness [84]. Using polycide bitlines, bitline to bitline capacitance might be around 0.1 fF

per bit.

DRAM chip power dissipation has increased only slightly with increases in chip capacity. The active power dissipated by 16M DRAMs ranges from 300 mW to 600 mW. This range is about 100 mW higher than the 4M range and 200 mW higher than the 1M range. In 16M DRAMs, bitline charging and discharging is the largest single component of chip power dissipation. Even at a slow 1 μs cycle, bitline current can be almost one-third of the total chip current [86]. Bitline power requirements will be even more significant in 64M DRAMs. Thus, typical 64M power dissipation may be 700 mW or more.

16M DRAM access times generally range from 55 ns to 65 ns. As shown in Figure 1.6, access times are gradually decreasing. 64M access should be around 50 ns. Typical cycle times should be about 100 ns.

As DRAM chip capacity has increased beyond 256K, the number of refresh cycles required per unit time has remained constant. Both the refresh interval and the number of refresh cycles have doubled with each new generation. Almost all 16M DRAMs require 2048 refresh cycles every 32 ms. 64M DRAMs will almost certainly require 4096 refresh cycles every 64 ms.

Projected 64M technology and performance parameters are summarized in Tables 4.1 and 4.2. Design rules were derived from typical lambda-based rules. Dimensions were scaled to accommodate projected 64M cell dimensions. The rules are presented in Table 4.3. While individual rules may differ from actual 64M technology dimensions, the set as a whole provides valuable insight into layout constraints.

Chip Area	220 mm^2
Cell Area	2 μm^2
Bitline Pitch	1 μm
n-channel Device Length	0.4 μm
p-channel Device Length	0.5 μm
Gate Insulator Thickness	100 Å
Power Supply	3.3 V
Device Thresholds	0.7 V
Bitline-to-Ground Capacitance	0.8 fF per bit
Bitline-to-Bitline Capacitance (metal bitlines)	0.2 fF per bit
Bitline-to-Bitline Capacitance (polycide bitlines)	0.1 fF per bit

Table 4.1: Projected 64M DRAM Technology Parameters

Power Dissipation	700+ mW
Access Time	50 ns
Cycle Time	100 ns
Refresh Interval	64 ms
Refresh Cycles	4096

Table 4.2: Projected 64M DRAM Performance Parameters

Gate Poly (GP) Rules:	
GP width over ND (Nch device length)	0.40 μm
GP width over PD (Pch device length)	0.50 μm
GP width not over xD	0.40 μm
GP spacing	0.40 μm
GP overlap past xD	0.40 μm
GP to xD spacing	0.20 μm
1st Level Metal (M1) Rules:	
M1 width	0.50 μm
M1 spacing	0.50 μm
2nd Level Metal (M2) Rules:	
M2 width	0.80 μm
M2 spacing	0.80 μm
N and P Diffusion (ND and PD) Rules:	
xD width	0.50 μm
xD spacing	0.50 μm
xD width over GP (device width)	0.50 μm
xD overlap past GP (S/D length)	0.50 μm
ND to PD spacing	1.60 μm
Contact (CT) Rules:	
CT length and width	0.40 μm
CT spacing	0.40 μm
CT within xD	0.20 μm
CT within GP	0.20 μm
CT within M1	0.05 μm
CT to xD spacing	0.40 μm
CT to GP spacing	0.40 μm
M1 - M2 Via (MV) Rules:	
MV length and width	0.80 μm
MV within M1	0.40 μm
MV within M2	0.40 μm
n-well (NW) Rules:	
NW width	2.00 μm
NW spacing	1.80 μm
ND to NW spacing	1.00 μm
ND within NW	0.60 μm
PD to NW spacing	0.60 μm
PD within NW	1.00 μm

Table 4.3: 64M DRAM Design Rules

Chapter 5

64M DRAM Sense Amplifier Design

This chapter examines critical 64M DRAM sense amplifier design issues. Bitline charging and discharging power dissipation and signal development are considered. Performance impacts of alternative bitline precharge potentials are explored. Sense amplifier layout constraints are analyzed. The use of isolation devices is considered. Finally, the sensitivity of an amplifier circuit suitable for 64M DRAMs is examined.

Computer simulations were performed using an ASTAP-like program. Projected 64M DRAM technology parameters were employed. Assuming 1024 sense amplifiers share the latch nodes, a crude latch node model was developed for sense amplifier simulations. Inductive and resistive effects, though important, are very dependent on process and layout details and therefore were not modeled. Bitline-to-ground capacitance and bitline-to-bitline capacitance values employed were 275 fF, and 50 fF, respectively. These values are appropriate for an array with 256 cells per bitline segment.

As a result of bitline-to-bitline coupling and shared latch nodes, sense amplifier operation is pattern-dependent. Figure 5.1 shows best case and worst case uniform patterns. V_{BL0}, V_{BL1}, and V_{BLR} are the initial '0,' '1,' and reference bitline segment

potentials. The '0' and '1' signals, $(V_{BLR} - V_{BL0})$ and $(V_{BL1} - V_{BLR})$, are equal in magnitude. In the best case pattern, '0' and '1' signals are presented to alternate sense amplifiers. During sensing, the potentials of adjacent bitline segments connected to different sense amplifiers move in the same directions. Thus, Inter-bitline coupling has minimal effect on sensing. In the worst case patterns, identical signals are presented to all sense amplifiers. During sensing, the potentials of adjacent bitline segments connected to different sense amplifiers move in opposite directions. Inter-bitline coupling has maximal effect. Except where otherwise noted, worst case uniform patterns were employed in all sense amplifier simulations.

5.1 Bitline Power Considerations

Sense amplifier power dissipation consists of two components: power intrinsic to bitline charging and discharging and power due to amplifier inefficiencies. Power dissipation per bitline pair due to bitline charging and discharging will be calculated by summing the amount of charge taken from the V_{DD} supply. The analysis will assume stored '0' and '1' potentials are ground and V_{DD}, respectively.

During signal amplification and cell restoration, one bitline segment must be charged to the stored '1' potential, V_{DD}. The charge needed from the supply is

$$Q_{amp} = (V_{DD} - V_{PC})C_{BL}, \tag{5.1}$$

where C_{BL} is the bitline segment capacitance. To precharge the bitlines for the next cycle, the bitline potentials can be first equalized, then charged or discharged to the precharge potential. The charge needed from the supply is

$$Q_{pc} = \begin{cases} 2(V_{PC} - V_{DD}/2)C_{BL}, & \text{if } V_{PC} > V_{DD}/2 \\ 0, & \text{if } V_{PC} \leq V_{DD}/2. \end{cases} \tag{5.2}$$

The total amount of charge needed per cycle is given by

$$Q_{BL} = Q_{amp} + Q_{pc} = (V_{DD}/2 + |V_{PC} - V_{DD}/2|)\, C_{BL}. \tag{5.3}$$

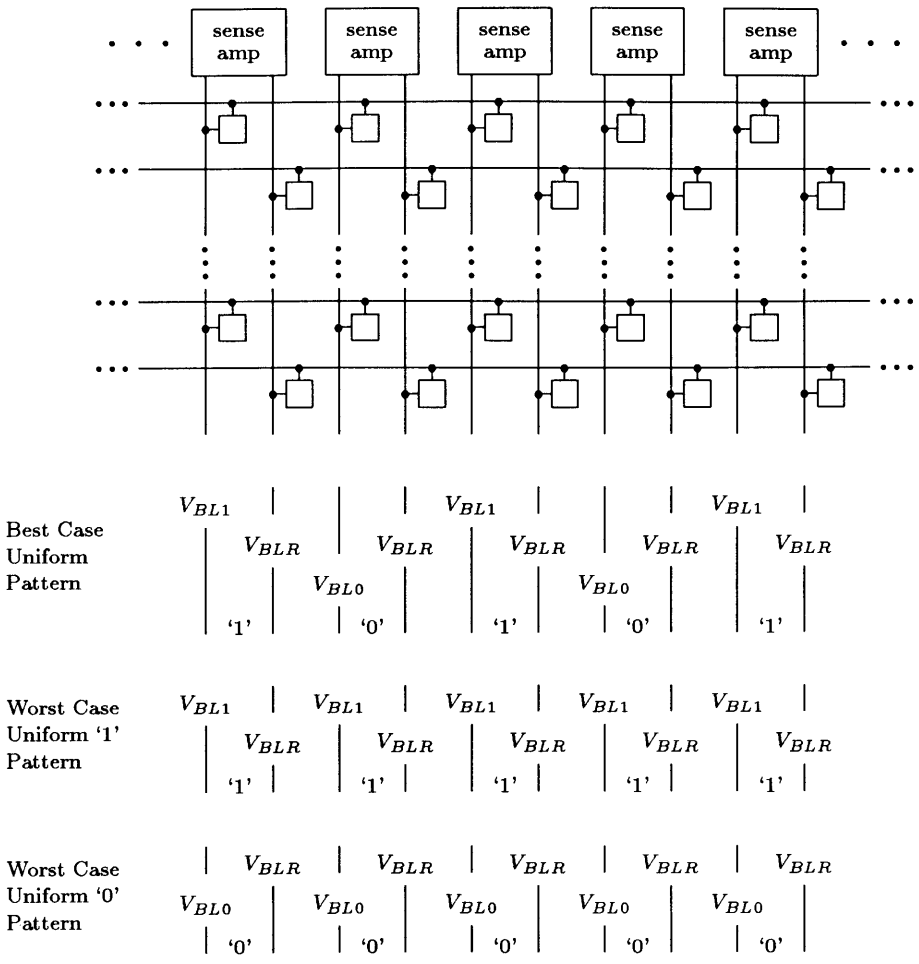

Figure 5.1: Uniform Array Patterns

Bitline Precharge Voltage (V)	Cells per Bitline Segment	Active Segment Pairs per Sense Amplifier	Average Bitline Power Dissipation (mW)
V_{DD}	256	1	550
	512	1	1150
	128	2	550
	256	2	1100
1/3 V_{DD} or 2/3 V_{DD}	256	1	360
	512	1	730
	128	2	360
	256	2	730
1/2 V_{DD}	256	1	270
	512	1	550
	128	2	270
	256	2	550

Table 5.1: 64M DRAM Intrinsic Bitline Power Dissipation

Thus, the average power dissipation per bitline pair due to bitline charging and discharging is given by

$$P_{BL,ave} = \frac{V_{DD}Q_{BL}}{t_{cycle}} = \frac{V_{DD}\left(V_{DD}/2 + |V_{PC} - V_{DD}/2|\right)C_{BL}}{t_{cycle}}. \tag{5.4}$$

To achieve a 4096 cycle refresh, 64M/4096 = 16K cells must be restored each refresh cycle. Consequently, 16K sense amplifiers must be active. Using Equation (5.4), average intrinsic bitline charging and discharging power dissipation during a 100ns refresh cycle was calculated for several memory configurations. The results are shown in Table 5.1.

Clearly, 64M DRAM intrinsic bitline charging and discharging power dissipation will be extremely important. In 4M and earlier DRAM generations, intrinsic bitline power dissipation was not nearly as significant. The growing importance of bitline power dissipation is due primarily to the increased number of active sense amplifiers in higher capacity DRAMs.

In general, the typical number of cells per sense amplifier has increased with each new DRAM generation. Most 16M DRAMs have 512 cells per sense amplifier. From Table 5.1 it is obvious that increasing the number of cells per sense amplifier to 1024 would result in much higher power dissipation.

Limiting the number of cells per sense amplifier to 512 will require finer segmentation of 64M DRAMs, increasing chip area and complexity. However, the advantages, reduced bitline power dissipation and lower transfer ratios, seem likely to outweigh the costs.

Table 5.1 illustrates a traditional argument for a $1/2\ V_{DD}$ bitline precharge potential. Intrinsic bitline power dissipation is proportional to $|V_{PC} - V_{DD}/2|$. Thus, in a $1/2\ V_{DD}$ bitline precharge potential scheme, intrinsic bitline power dissipation will be half the intrinsic power dissipation in a V_{DD} bitline precharge scheme. However, intrinsic bitline charging and discharging power dissipation is only one component of total power dissipation. Other power requirements must also be considered.

5.2 Signal Development Considerations

The time required for signal development depends primarily on cell capacitance and transfer device current. As DRAM chip capacity increases, cell capacitance remains relatively stable. Device dimensions and supply voltages are reduced. In saturation, device current is proportional to (W/L), is inversely proportional to gate oxide thickness, and is proportional to the square of the overdrive voltage. Thus, if device width, length, and oxide thickness and the overdrive voltage are all scaled by the same factor, saturation current will decrease as DRAM chip capacity increases. In linear operation, device current is directly proportional to the overdrive voltage. Thus, if the threshold voltage and the supply voltage were scaled with device dimensions, device current in linear operation would remain fairly constant. However, in high density

DRAMs, threshold voltages are not scaled with supply voltages and device dimensions. Instead, threshold voltages remain relatively stable. Thus, signal development time tends to increase with DRAM chip capacity, requiring faster sensing and/or increasing chip access time.

Long wordline rise time delays the beginning of charge transfer. In high density DRAMs, wordline loads tend to be quite large. Delays associated with wordline rise time may be significant, relative to total access time.

In 64M DRAMs, signal development time may account for a substantial portion of total access time. The impact of the bitline precharge potential on signal development time is very significant. For a p-channel array, a higher bitline precharge voltage results in earlier activation of the transfer devices and greater transfer device overdrive. For an n-channel array, a lower bitline precharge voltage speeds signal development.

Signal development was simulated using both n-channel and p-channel transfer devices. The wordline waveforms shown in Figure 5.2 were used. A 50 fF cell capacitance and a 350 fF bitline capacitance were assumed. Transfer device lengths and widths were both 0.4μm.

Figure 5.3 shows the percentage signal development completion versus time for p-channel transfer devices and 3.30 V, 2.20 V, and 1.65 V bitline precharge potentials. Achieving 95 percent '0' signal development requires about 6 ns if bitlines are precharged to 3.30 V, 8 ns if bitlines are precharged to 2.20 V, and 10.5 ns if bitlines are precharged to 1.65 V.

Figure 5.4 shows signal development versus time for n-channel transfer devices and 0.00 V, 1.10 V, and 1.65 V bitline precharge potentials. '1' signal development requires about 4.75 ns if bitlines are precharged to 0.00 V, 6.5 ns if bitlines are precharged to 1.10 V, and 8 ns if bitlines are precharged to 1.65 V.

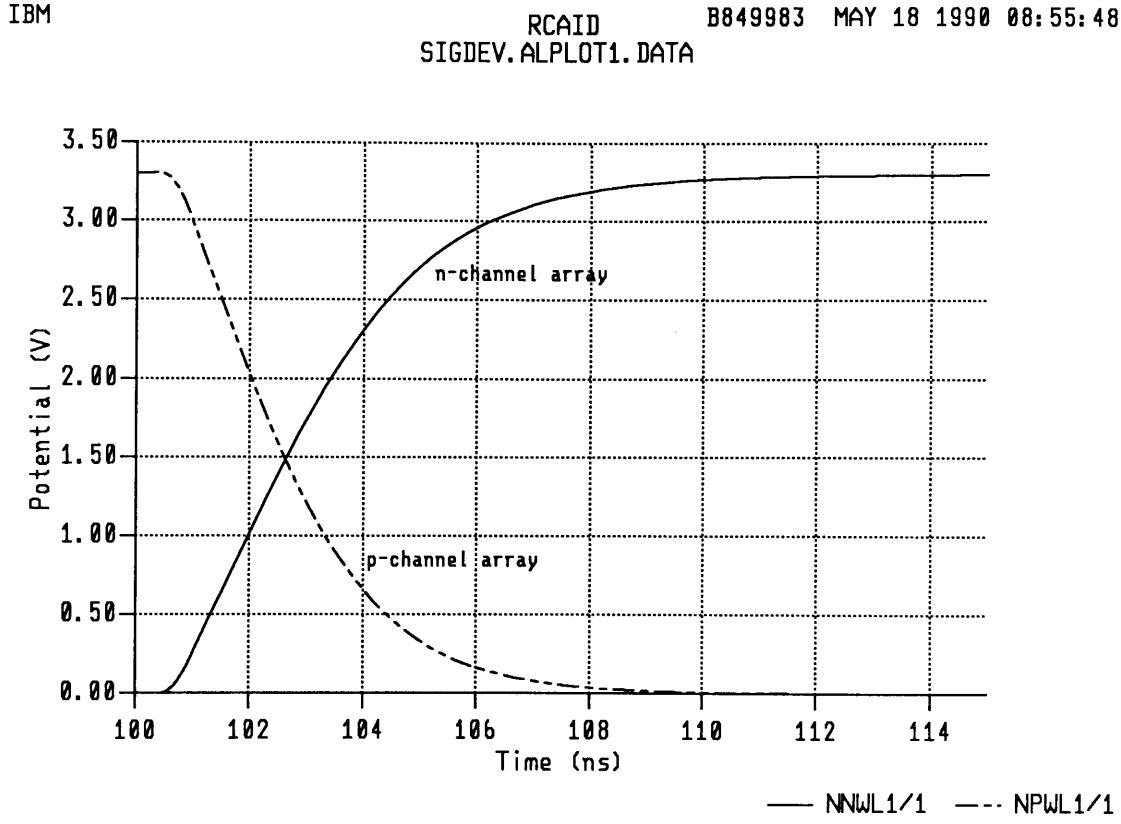

Figure 5.2: Wordline Waveforms for Signal Development Analysis

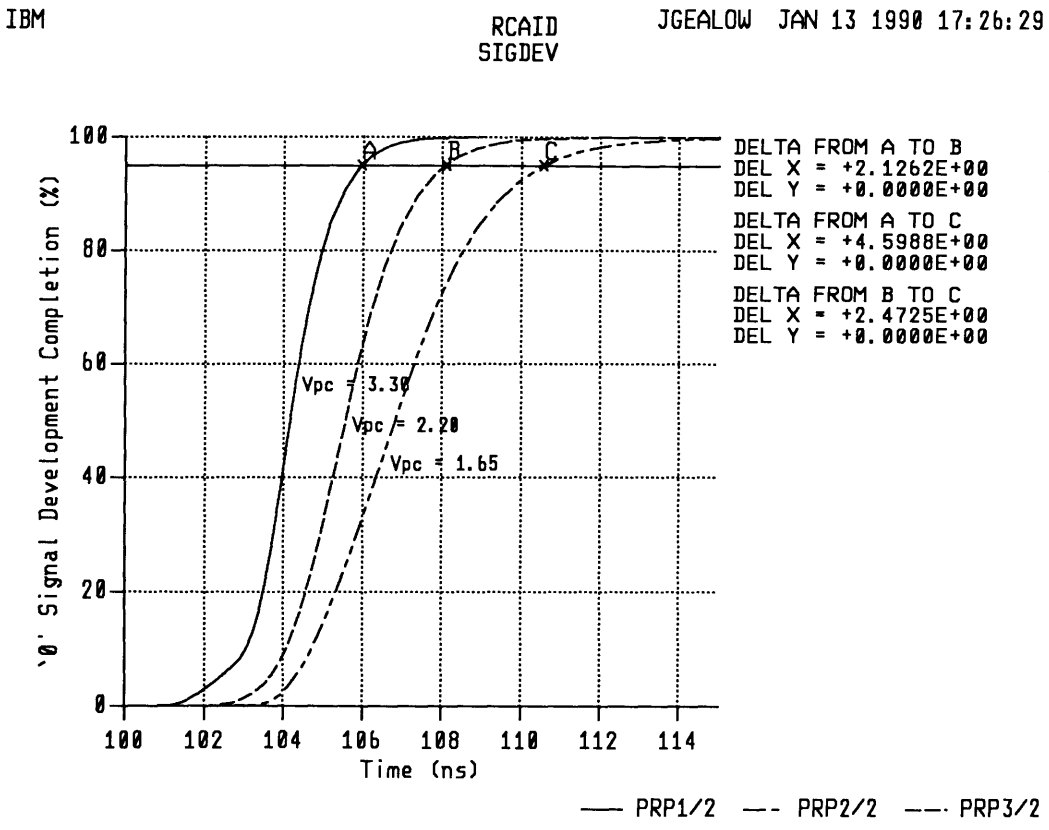

Figure 5.3: p-channel Array Signal Development

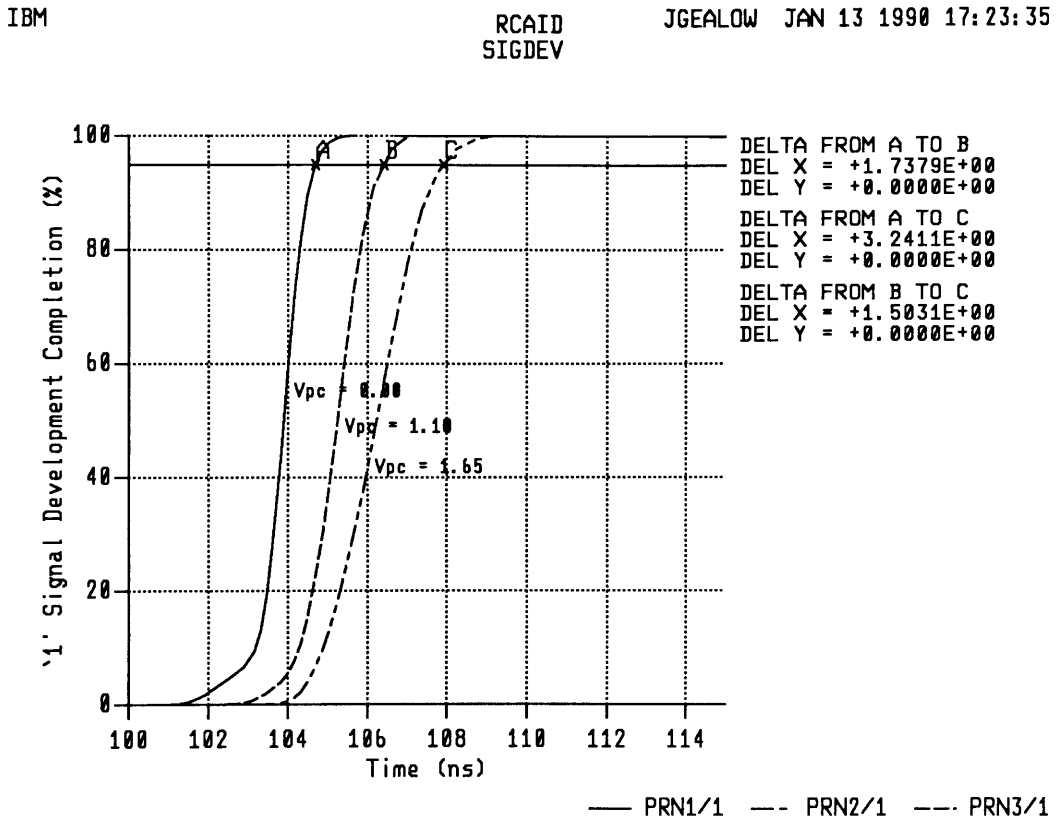

Figure 5.4: n-channel Array Signal Development

Unless signal development and sensing are both completed within about 20 ns, a 50 ns total access time may not be attainable. If signal development takes longer, sensing must be completed faster. If a p-channel array is employed, sensing should require less than 14 ns if bitlines are precharged to 3.30 V, less than 12 ns if bitlines are precharged to 2.20 V, and less than 9.5 ns if bitlines are precharged to 1.65 V. If an n-channel array is employed, sensing should require less than 15.25 ns if bitlines are precharged to 3.30 V, less than 14.5 ns if bitlines are precharged to 2.20 V, and less than 12 ns if bitlines are precharged to 1.65 V.

These results quantify an important advantage of precharging bitline segments to higher potentials in p-channel arrays and lower potentials in n-channel arrays. Signal development time is significantly reduced, relaxing sensing speed requirements.

5.3 Bitline Precharge Potential

Three sense amplifier circuits will be considered. All are designed for use with a p-channel array. Corresponding circuits can be used with n-channel arrays.

The primary difference between the three sense amplifiers is the bitline precharge voltage. The purpose of this section is to identify the precharge potential most suitable for 64M DRAMs. Later, other circuit modifications will be considered.

5.3.1 V_{DD} Sense Amplifier

A sense amplifier designed for use with a full V_{DD} bitline precharge potential is shown in Figure 5.5. The latch node, SAN, is shared by many sense amplifiers. It is driven by large n-channel set devices during sensing. Initial sensing is performed entirely by the n-channel cross-coupled pair. Both p-channel devices remain off until the low bitline segment potential drops below $V_{DD} - V_T$. As long as the high bitline segment potential remains above $V_{DD} - V_T$, no current will flow from V_{DD} to the low potential

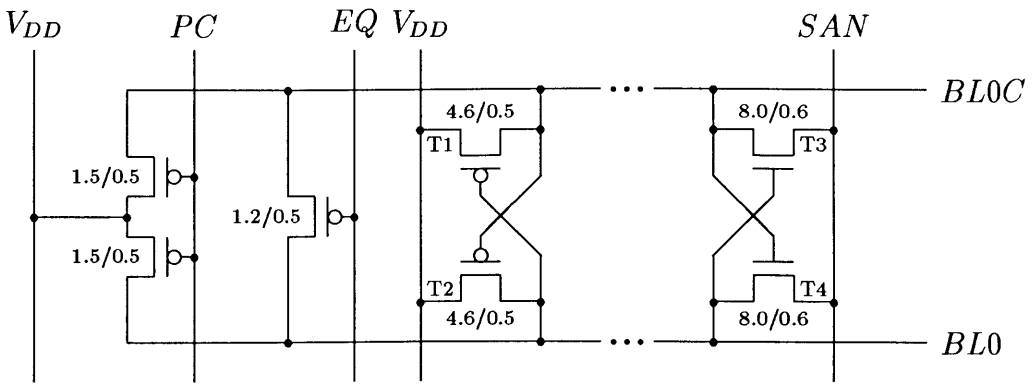

Figure 5.5: V_{DD} Sense Amplifier Circuit

bitline segment.

The n-channel cross-coupled pair devices are relatively wide, reducing offset due to process variations and minimizing the amount of off-side current necessary to achieve adequate speed. The devices are 1.5 times longer than minimum, limiting gain and threshold mismatches due to length variations.

Since the p-channel cross-coupled pair devices are off during initial sensing, they do not appreciably affect amplifier sensitivity. The device lengths are as short as possible, maximizing device gain and minimizing layout area. Since the devices do not carry much current, device widths are relatively narrow, reducing layout area.

An equalization device is employed. The device speeds bitline segment potential equalization, allowing a shorter precharge interval.

V_{DD} sense amplifier waveforms are shown in Figure 5.6. As shown in the figure, signal amplification is completed within 14 ns.

Cross-coupled transistor currents during sensing are shown in Figure 5.7. The n-channel device currents are positive and the p-channel device currents are negative. The n-channel off-side current is low and the p-channel off-side current is negligible.

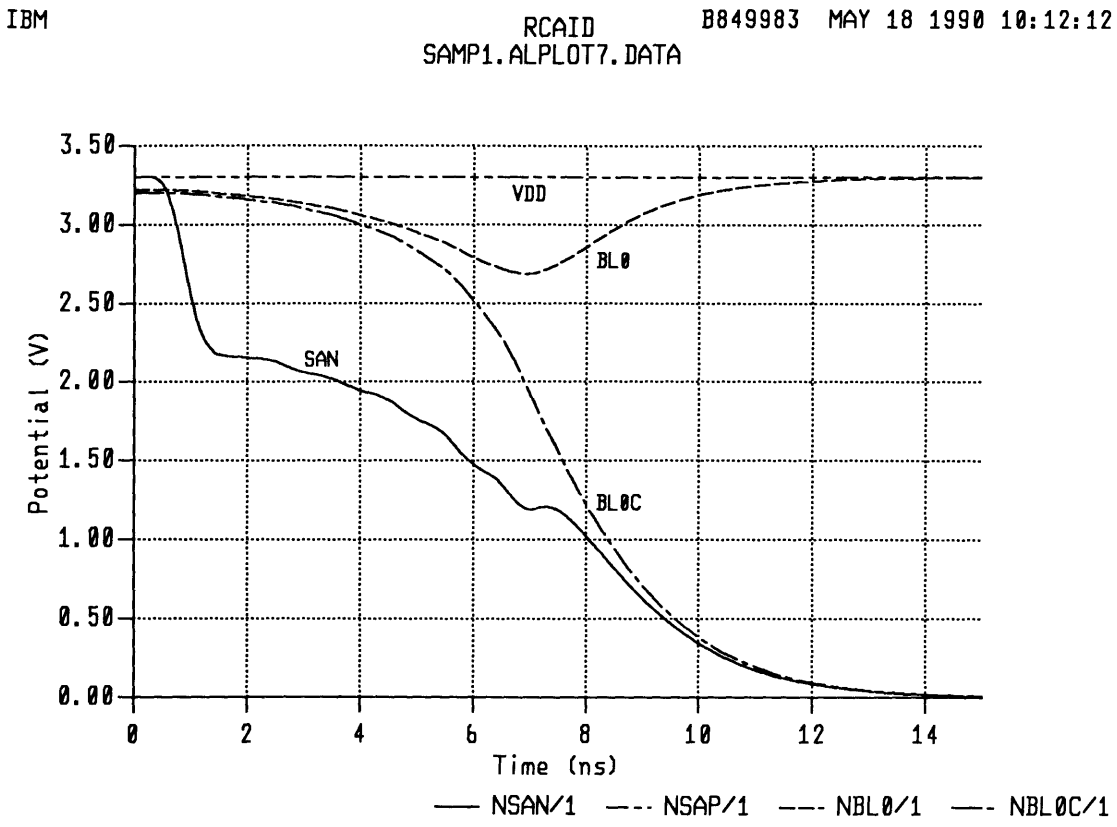

Figure 5.6: V_{DD} Sense Amplifier Waveforms. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

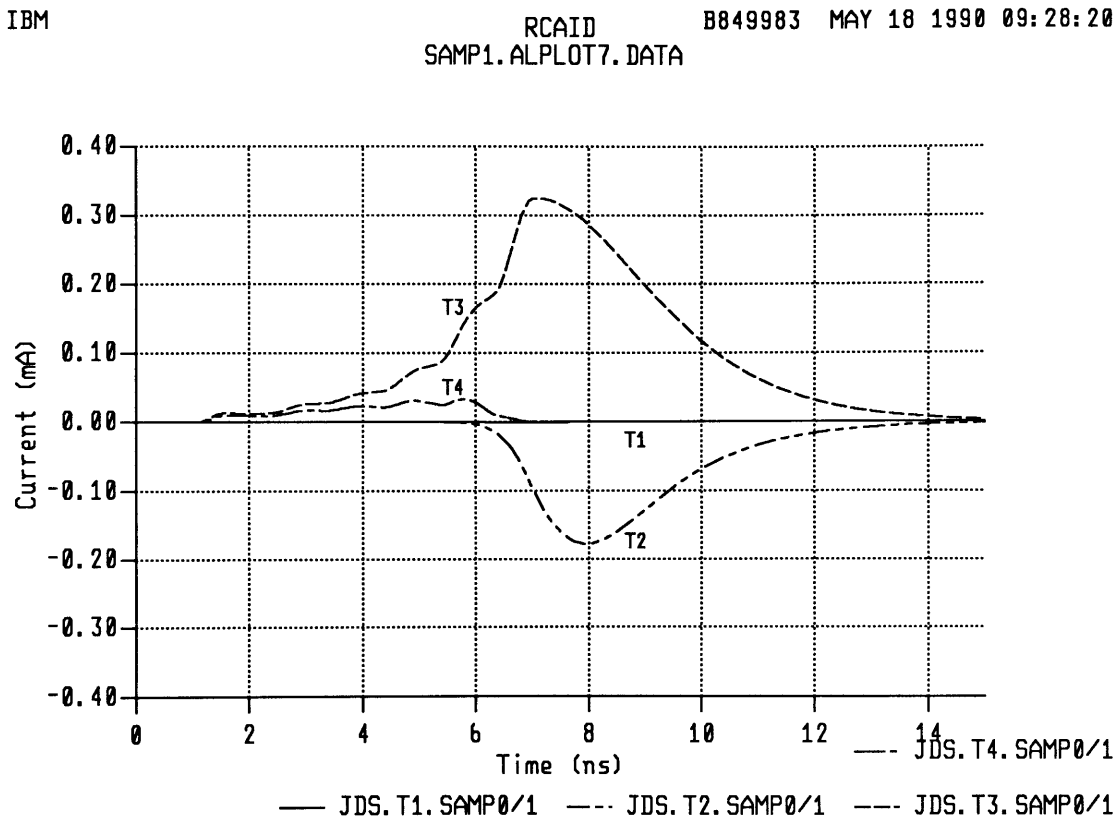

Figure 5.7: V_{DD} Sense Amplifier Device Currents. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

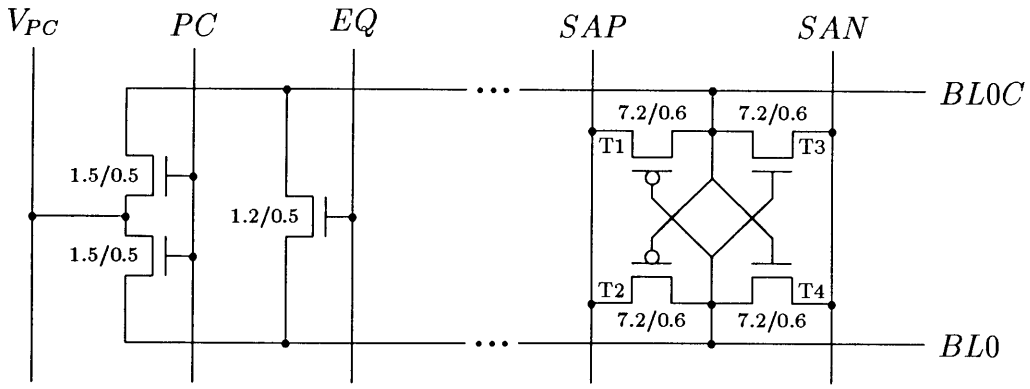

Figure 5.8: 1/2 V_{DD} Sense Amplifier Circuit

5.3.2 1/2 V_{DD} Sense Amplifier

A sense amplifier designed for use with a 1/2 V_{DD} bitline precharge potential is shown in Figure 5.8. Using this circuit structure, three timing approaches are possible: activation of the n-channel cross-coupled pair first, activation of the p-channel cross-coupled pair first, or simultaneous activation of both pairs. The third option was chosen to maximize amplification speed.

Since both cross-coupled pairs are active during initial sensing, both n-channel and p-channel device parameters affect amplifier sensitivity. Device lengths are greater than minimum. Both n-channel and p-channel device widths are relatively large. As a result, the 1/2 V_{DD} sense amplifier requires more area than the V_{DD} sense amplifier.

To precharge and equalize the bitline segments, n-channel devices are employed. Higher n-channel mobility partially compensates for the low device overdrives during precharge.

V_{DD} sense amplifier waveforms are shown in Figure 5.6. The latch nodes are driven rather strongly, allowing completion of signal amplification within about 12 ns.

Cross-coupled transistor currents during sensing are shown in Figure 5.7. As be-

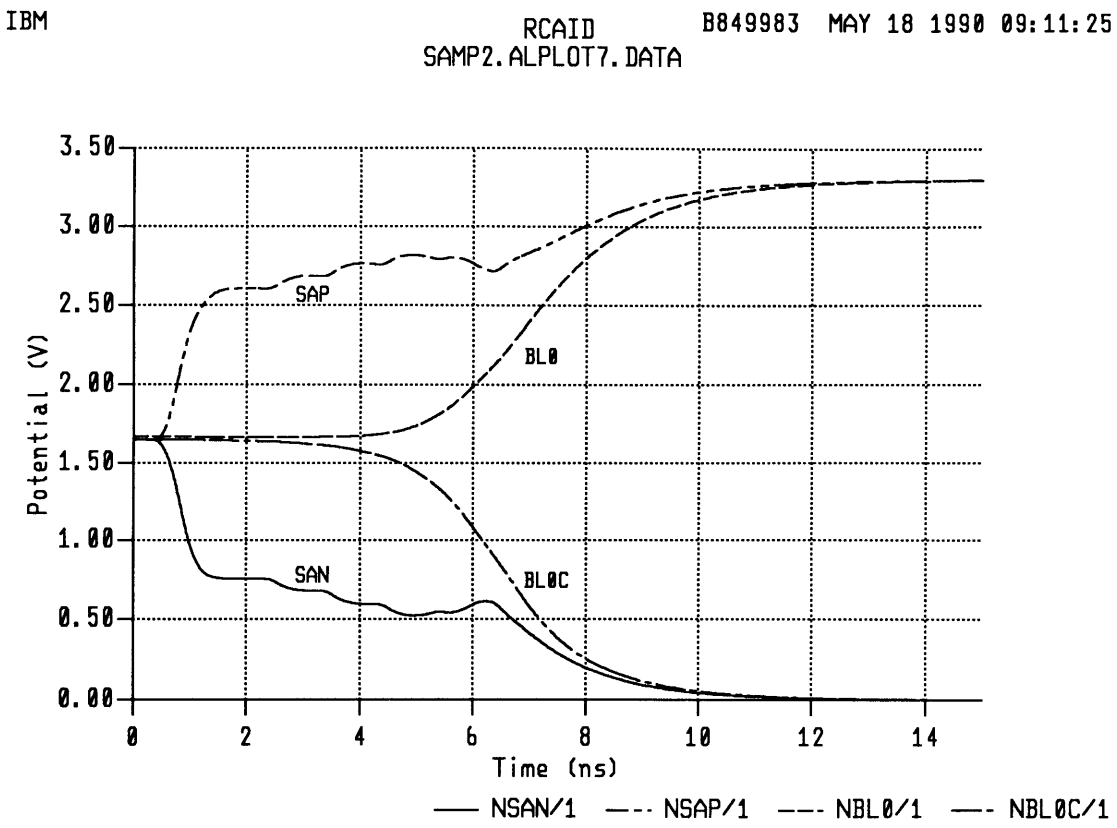

Figure 5.9: $1/2\,V_{DD}$ Sense Amplifier Waveforms. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

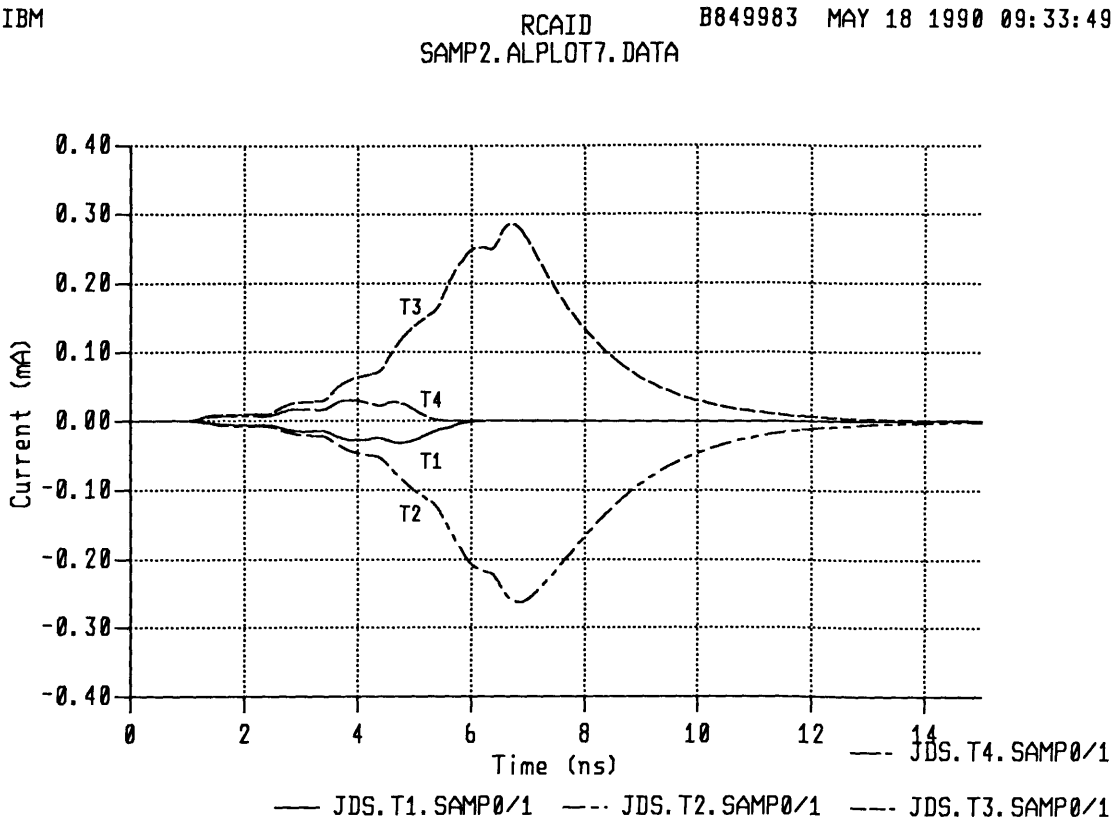

Figure 5.10: 1/2 V_{DD} Sense Amplifier Device Currents. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

fore, n-channel device currents are positive and p-channel device currents are negative. Both n-channel and p-channel off-side currents are evident.

Despite significantly greater off-side current, the 1/2 V_{DD} sense amplifier is not sufficiently faster than the V_{DD} sense amplifier to make up for the difference in signal development times. Thus, use of a 1/2 V_{DD} bitline precharge potential requires either increased access time or even more substantial off-side current.

Another disadvantage of the 1/2 V_{DD} precharge potential is the need for large set

devices to drive two shared latch nodes, SAN and SAP. Once initial amplification is complete, the bitlines should be driven as quickly as possible to the '0' and '1' potentials, maximizing amplifier speed. The rate at which the bitline potentials can be changed is limited by the size of the set devices. To achieve 11 ns signal amplification, it was necessary to employ somewhat larger n-channel SAN set devices than were used in the V_{DD} sense amplifier. More importantly, p-channel SAP set devices, approximately three times larger than the n-channel SAN devices, were needed. These devices require substantial additional layout area.

Bitline segment precharge poses an undesirable tradeoff. Bitlines can be precharged without using a voltage generator by equalizing the bitline potentials. However, if the bitlines are equalized at the end of the cycle, they may float above or below $1/2\ V_{DD}$ before the next cycle, disrupting amplifier operation. If they are equalized at the beginning of the cycle, equalization will likely delay wordline activation. In 4M and 16M DRAMs, precharge voltage generators are often employed. They require additional layout area and power.

5.3.3 $2/3\ V_{DD}$ Sense Amplifier

A sense amplifier designed for use with a $2/3\ V_{DD}$ bitline precharge potential is shown in Figure 5.11. The circuit is based on the n-channel array sense amplifier used in the NTT 16M DRAM [74].

Important aspects of the $2/3\ V_{DD}$ sense amplifier are similar to the $1/2\ V_{DD}$ sense amplifier. Though initial sensing could be performed using only the n-channel cross-coupled pair, both cross-coupled pairs are activated simultaneously to achieve adequate speed. As a result, sensitivity considerations warrant relatively wide and long n-channel and p-channel cross-coupled pair devices.

The precharge and equalization device overdrives during the precharge interval

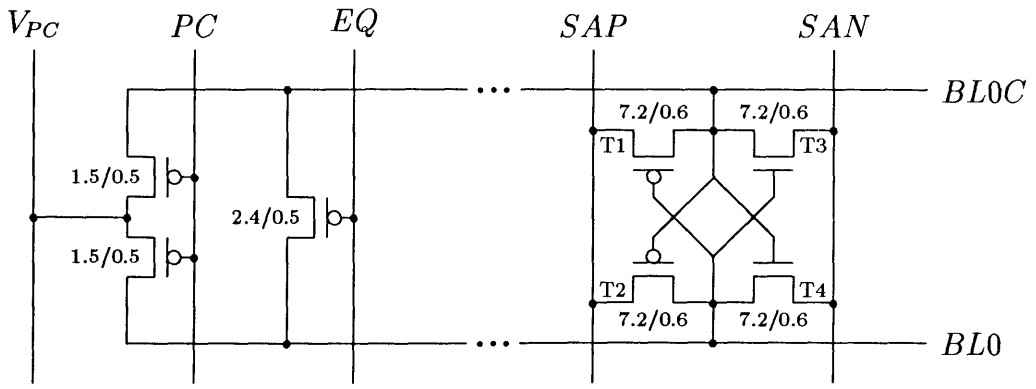

Figure 5.11: 2/3 V_{DD} Sense Amplifier Circuit

are lower than the overdrives in the V_{DD} sense amplifier. The equalization device is twice as wide as the V_{DD} sense amplifier equalization device, partially compensating for the reduced overdrive.

2/3 V_{DD} sense amplifier waveforms are shown in Figure 5.9. The latch nodes are driven sufficiently fast to achieve 12 ns signal amplification. Thus, total access time should be similar to the access time of the V_{DD} bitline precharge configuration.

Cross-coupled transistor currents during sensing are shown in Figure 5.13. Once again, n-channel device currents are positive and p-channel currents are negative. The n-channel off-side current is similar to the V_{DD} and 1/2 V_{DD} sense amplifier n-channel off-side currents. The p-channel off-side current, while smaller than 1/2 V_{DD} sense amplifier p-channel off-side currents, is still significant.

Like the 1/2 V_{DD} sense amplifier, the 2/3 V_{DD} sense amplifier requires both SAN and SAP set devices. Similar set device sizes were employed.

Bitline segment precharge is even more problematic than in the 1/2 V_{DD} approach. The precharge potential, V_{PC}, must be produced using either a diode-connected transistor or a voltage generator. The diode approach poses a tradeoff between precharge potential accuracy, layout area, and precharge interval length. High precharge poten-

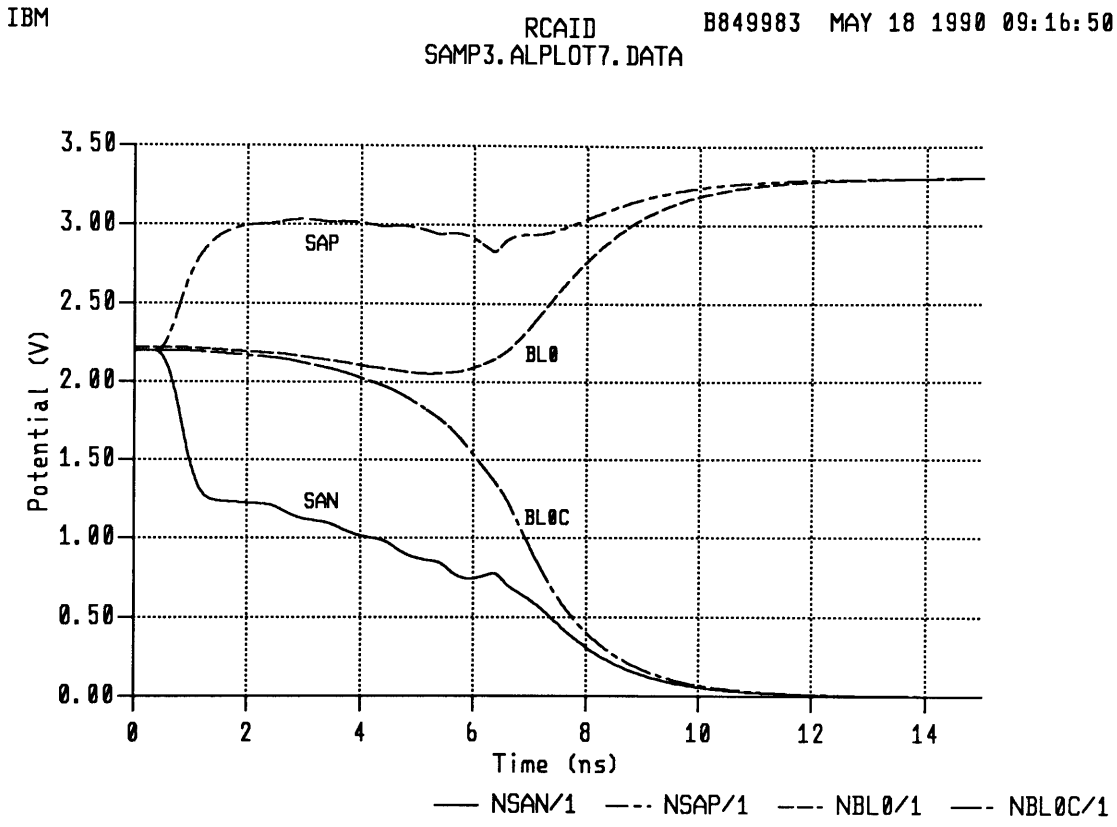

Figure 5.12: 2/3 V_{DD} Sense Amplifier Waveforms. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

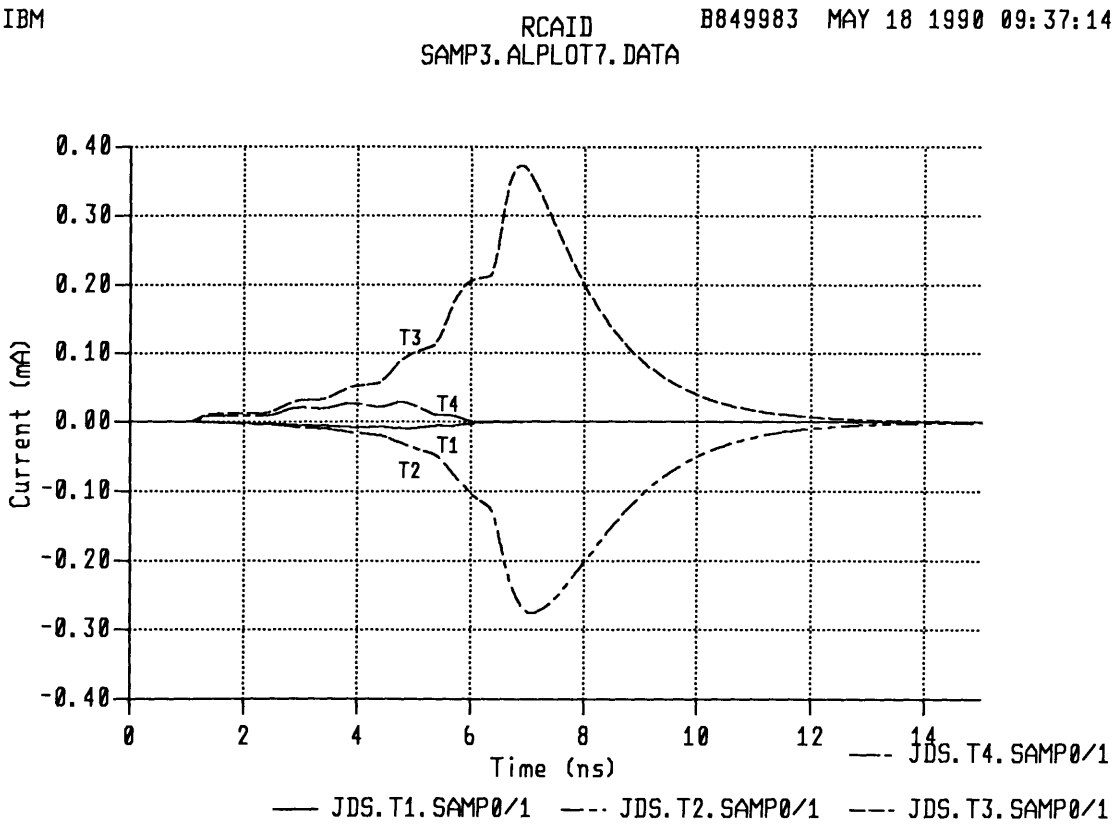

Figure 5.13: 2/3 V_{DD} Sense Amplifier Device Currents. 20mV initial signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

tial accuracy requires a large layout area to increase diode device width and/or a long precharge interval. Using a voltage generator would likely require very high current in order to provide the needed current driving capability.

Dhong *et al.* [75] proposed alternative precharge circuitry. In their circuit, the p-channel precharge devices are replaced by n-channel devices and the V_{PC} node is tied to V_{DD}. The bitlines are precharged through the n-channel devices, producing the necessary threshold drop. A tradeoff exists between n-channel precharge potential accuracy, n-channel precharge device area, and precharge interval length. Mismatches between n-channel precharge devices in different columns may cause precharge potential variations, resulting in reduced amplifier sensitivity due to effective timing skews.

5.3.4 Design Impacts

Use of a V_{DD} bitline precharge potential in 64M p-channel array DRAMs offers several important advantages:

- Faster signal development. Earlier transfer device turn-on and greater transfer device overdrive speed signal development. As a result, sensing speed may be reduced and/or access time may be improved. Slower sensing decreases power dissipation due to off-side current and improves sense amplifier sensitivity.

- Primary amplification is performed entirely by the n-channel cross-coupled pair. The p-channel cross-coupled devices need not be optimized for sensitivity, saving layout area. In addition, the source of the p-channel cross-coupled pair may be tied directly to V_{DD}, avoiding the extra area, power, and complexity required by p-channel cross-coupled pair latch node set circuitry.

- Large precharge and equalization device overdrive and fast device activation. The maximum device overdrive is equal to $V_{DD} - V_T$. Devices begin conducting after the clock potentials drops just $+1$ V_T below V_{DD}. Smaller precharge and equalization devices may be used and/or the precharge interval may be shortened. Smaller devices limit equalization and precharge clock loads, saving clock driver area and power, and reduce sense amplifier area.

- A supply potential is used for the bitline precharge potential. No additional circuitry is required to generate the bitline precharge potential, saving area and power without compromising precharge potential stability.

Traditional advantages of a $1/2\ V_{DD}$ precharge potential in CMOS DRAMs are mostly lost when the approach is applied to 64M DRAM sense amplifiers. Reductions in peak current and dI/dt due to limited bitline swing are offset by increases in current and dI/dt due to the faster amplification required to compensate for slow signal development. Reductions in bitline charging and discharging power are offset by additional power dissipation due to increased off-side current, additional set device clocking, and possible use of a bitline precharge voltage generator. Finally, while dummy cells are not required to provide a reference potential, elimination of dummy cells creates a capacitance mismatch during sensing and increases susceptibility to precharge voltage fluctuations.

A potential advantage of a $1/2\ V_{DD}$ precharge voltage is the equality of the positive and negative bitline potential swings. This equality minimizes variations in plate and bulk potentials induced by bitline potential swings. Plate noise is especially significant when a high impedance plate voltage generator is employed [87]. However, if the plate is tied to a supply potential, the noise may not be very substantial, relative to other noise sources.

A 2/3 V_{DD} precharge potential can be viewed as a compromise between V_{DD} and 1/2 V_{DD} bitline precharge potentials. It provides faster signal development, larger precharge and equalization device overdrives, and quicker precharge device activation than the 1/2 V_{DD} precharge potential. However, it also requires more bitline charging and discharging current and does not achieve perfectly balanced bitline swing.

2/3 V_{DD} sense amplifiers, like 1/2 V_{DD} sense amplifiers require set devices for both the *n*-channel and *p*-channel cross-coupled pair source nodes. Also, to achieve adequate speed, both *n*-channel and *p*-channel devices must participate in sensing. Finally, bitline precharge potential generation is quite problematic.

A full V_{DD} precharge potential seems most appropriate for 64M *p*-channel array DRAM sense amplifiers. The same general arguments support use of ground for the precharge potential in *n*-channel array DRAMs. Signal development is faster, though the absolute differences in signal development time are not quite as large as the *p*-channel array differences. Primary amplification is performed using only one cross-coupled pair. Larger equalization and precharge device overdrive and quicker device turn-on are achieved. With *p*-channel arrays, this advantage is somewhat offset by the substitution of *n*-channel precharge and equalization devices when using a 1/2 V_{DD} precharge potential. With *n*-channel arrays, the advantage is not so diluted. Finally, a supply potential is used for the bitline precharge potential.

Precharging *n*-channel array bitlines to V_{DD} would allow use of *n*-channel sense amplifier devices for primary amplification. However, signal development would be much too slow in 64M DRAMs. When sensing a '0,' the transfer devices would operate in a slow source-follower fashion. In an *n*-channel array, lower bitline precharge potentials result in faster transfer device activation and higher transfer devices overdrive.

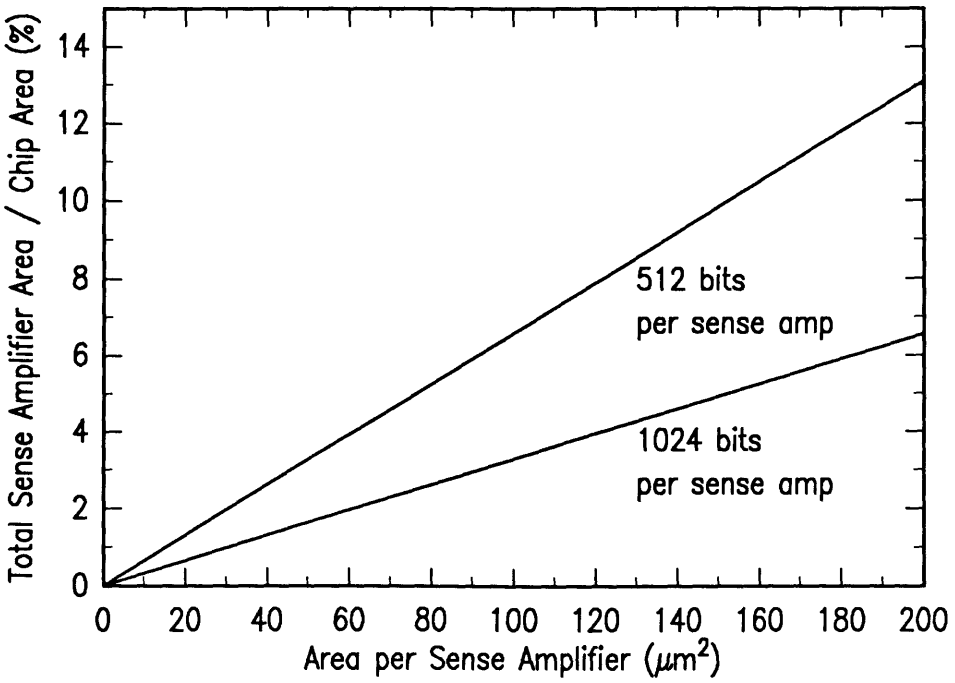

Figure 5.14: Total Sense Amplifier Area versus Area per Sense Amplifier

5.4 Layout Considerations

Sense amplifier area accounts for a substantial fraction of chip area. Using projected 64M DRAM technology parameters, Figure 5.14 illustrates the relationship between area per sense amplifier and the fraction of chip area used by sense amplifiers. Limiting the number of cells per sense amplifier to 512 will necessitate use of relatively small sense amplifiers.

V_{DD}, 1/2 V_{DD}, and 2/3 V_{DD} sense amplifier layouts are detailed in Appendix B. Use of metal bitlines was assumed. None of the layouts require 2nd-level metal. Thus, 2nd-level metal column address lines or column I/O lines may run over the sense amplifiers, parallel to the bitlines. The V_{DD}, 1/2 V_{DD}, and 2/3 V_{DD} sense amplifiers each require about 100 μm^2.

Achieving a 2 μm sense amplifier pitch was difficult, but did not require significant layout area efficiency compromises. It is certainly not necessary to double the sense

amplifier layout pitch by placing complete sense amplifiers on both sides of the arrays. Nor does such an approach seem desirable. Twice as many sense amplifier signal buses and signal drivers would be required. In addition, column decode circuitry would be needed on both sides of the arrays.

In 256M and higher density DRAMs, the bitline pitch may be so small relative to feature sizes that sense amplifiers cannot fit within two bitline pitches. Fortunately, 64M DRAM sense amplifiers can fit within two bitline pitches.

The small sense amplifier pitch does impose some important design limitations. To avoid using 2nd-level metal, bitline precharge devices and column I/O circuitry must be placed on opposite sides of the arrays. Also, unless 2nd-level metal is employed to distribute the bitline precharge potential, precharge device widths are limited by the sense amplifier pitch. This constraint is especially significant when using a $1/2\ V_{DD}$ or $2/3\ V_{DD}$ precharge potential since the precharge device overdrives are relatively small.

5.5 Isolation Devices

Isolation devices do not seem desirable in 64M DRAMs. The traditional purpose of isolation devices is to separate the active cross-coupled pair(s) from the large bitline capacitances during initial sensing. If the bitline capacitance is very large, isolation devices may significantly improve amplifier speed and sensitivity. However, in 64M DRAMs, processing technology features make isolation device usage inappropriate.

As shown in Appendix B, including one isolation device per bitline segment would require over 12 μm^2 of area per sense amplifier. If this area were taken from one of the cross-coupled pairs, device widths would have to be decreased by 3 μm. Thus, potential benefits of isolation devices must be weighed against a large layout area cost.

Isolation device clock loads should be roughly comparable to wordline loads. Thus, in 64M DRAMs, isolation device clock delays will be significant, decreasing DRAM speed.

Employment of isolation devices in 64M DRAMs requires either using an undesirable intermediate bitline precharge potential or bootstrapping the isolation device clock. If a V_{DD} bitline precharge potential and n-channel isolation devices are employed, the isolation device clock potential must be bootstrapped above V_{DD} during signal development. If p-channel isolation devices are employed, the isolation device clock potential must be bootstrapped below ground to restore full '0' potentials. Similarly, if bitlines are precharged to ground, p-channel isolation device clocks must be bootstrapped below ground during signal development and n-channel isolation device clocks must be bootstrapped above V_{DD} during cell restoration.

Decreasing the effective capacitance between cross-coupled pair signal nodes and ground will not always improve performance. In 64M DRAMs with only 256 cells per bitline segment, total bitline capacitance is not particularly large. Isolating cross-coupled pair from the bitline segments will not only decrease total effective signal node capacitance, but will also effect the ratio of the coupling capacitance between the signal nodes and the latch nodes to the capacitance between the signal node and ground.

As processing technology improves, gate capacitances generally increase relative to diffusion capacitances. Decreases in gate insulator thickness increase gate capacitances. Increases in bulk doping increase diffusion capacitances, but the dependence is not nearly as strong as the gate capacitance dependence on insulator thickness. Improved isolation techniques reduce the perimeter components of diffusion capacitances. In 64M DRAMs, sense amplifier diffusion capacitances will likely be small relative to gate capacitances. Thus, if isolation devices are employed, the ratio of

cross-coupled pair gate-source capacitances to the parasitic capacitance between the signal nodes and ground will be quite large. As a result, during primary sensing the change in the off-side signal potential due to gate-source coupling will be substantial.

Unless both the n-channel and p-channel cross-coupled pairs are isolated from the bitlines, a full V_{DD} signal cannot be developed until after the isolation devices are turned on. But if both n-channel and p-channel cross-coupled pairs are isolated, the isolation device clock must be bootstrapped to allow restoration of full V_{DD} and ground stored potentials.

The V_{DD} sense amplifier was simulated assuming complete isolation of the bitlines and the p-channel cross-coupled pair from the n-channel cross-coupled pair. Parasitic diffusion capacitances were derived from the layout. The resulting waveforms are shown in Figure 5.15. The high signal potential drops by roughly a factor of two.

As a result of the large high signal potential reduction, the overdrive on the n-channel cross-coupled pair as the isolation devices are turned on is very small. If n-channel isolation devices are employed, the device separating the low potential signal node and the low potential bitline will turn on before the opposite isolation device. Because cross-coupled pair overdrive is small, the isolation devices must be activated very slowly to keep the low signal node potential below V_T, avoiding significant off-side current.

The benefits of isolation device use in 64M DRAM sense amplifiers are questionable at best. The costs include increased sense amplifier area, extra clock timing and driver circuits, and decreased sensing speed due to isolation device clock delays. Thus, isolation devices should be avoided.

5.6 Sensitivity Analysis

The sensitivity of the V_{DD} sense amplifier was examined. Three aspects of sensitivity were considered: the minimum overdrive voltage required, given a perfectly balanced amplifier; offset due to process variations; and offset due to bitline-to-bitline coupling.

Figure 5.16 shows the final bitline segment potential difference versus the initial signal presented to the sense amplifier. A worst case uniform pattern was assumed. A 3 mV overdrive is sufficient to achieve adequate amplification.

Figure 5.17 shows the average off-side current per sense amplifier assuming a 100 ns cycle and a worst case uniform pattern. If 16K sense amplifiers are active, 10 mV sense amplifier overdrives will limit total average DRAM off-side current to less than 35 mA.

Sense amplifier offset due to transistor gain and bitline capacitance mismatches was analyzed using both best and worst case uniform patterns. All columns had equally unbalanced sense amplifiers and bitlines. Results are presented in Figures 5.18 and 5.19.

As expected, offsets due to gain and capacitance mismatches are roughly proportional to the gain and capacitance mismatch percentages. Interestingly, bitline-to-bitline coupling has a large impact on the resulting offsets.

Increasing cross-coupled pair transistor currents decreases G_m/I, worsening offset due to transistor gain and bitline capacitance mismatches. Because the latch node set devices are shared by many sense amplifiers, currents during amplification are pattern dependent. If the pattern includes only a few '1's and many '0's, the latch node potential will fall quickly until it reaches $V_{BLR} - V_T$. As a result, currents in the amplifiers sensing '1's will be higher than usual. The worst case pattern is shown in Figure 5.20. A small group of '1's are present in the middle of a field of '0's.

Bitline-to-bitline coupling may aid detection of the '1's next to '0's. Thus, the inner '1's are most vulnerable.

In order to minimize this effect, the latch node is initially pulled down by relatively small devices. Given a uniform pattern, off-side current actually increases about 1-2 ns after the cross-coupled pairs begin conducting. Computer simulation showed only a slight difference in offset under a worst case uniform pattern and offset under the worst case non-uniform pattern shown in Figure 5.20.

Bitline-to-bitline coupling during signal amplification introduces an offset. The offset of an individual amplifier depends on the signals presented to surrounding amplifiers. Figure 5.21 illustrates patterns used for coupling induced offset analysis. In the best case patterns, the high bitline segment potentials are equal. Thus, amplification will begin simultaneously in all amplifiers. In the worst case pattern, the low potentials are equal. Amplification will begin in the surrounding sense amplifiers before amplification begins in an amplifier presented with a marginal signal.

Figure 5.22 shows results of computer simulations. Bitline-to-bitline coupling during signal amplification results in very significant sense amplifier offset, especially when a single marginal signal is surrounded by strong signals and when the high bitline potentials differ.

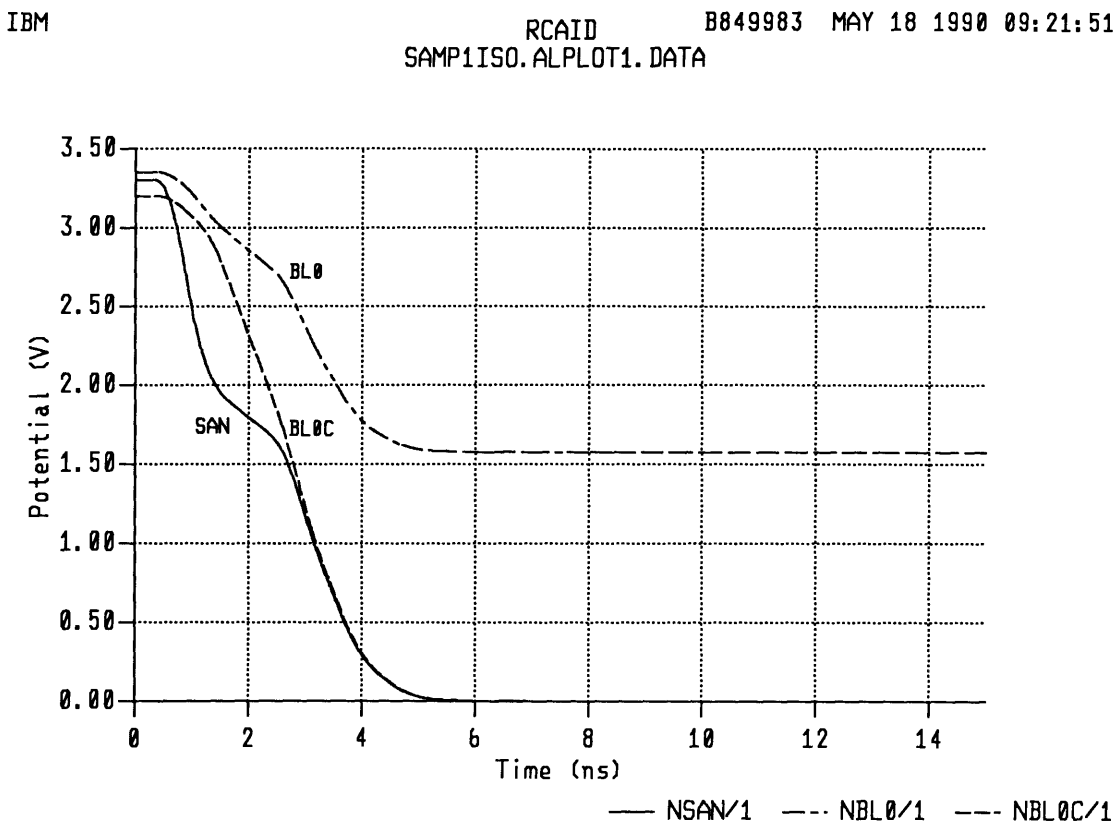

Figure 5.15: Isolated n-channel Cross-Coupled Pair Waveforms

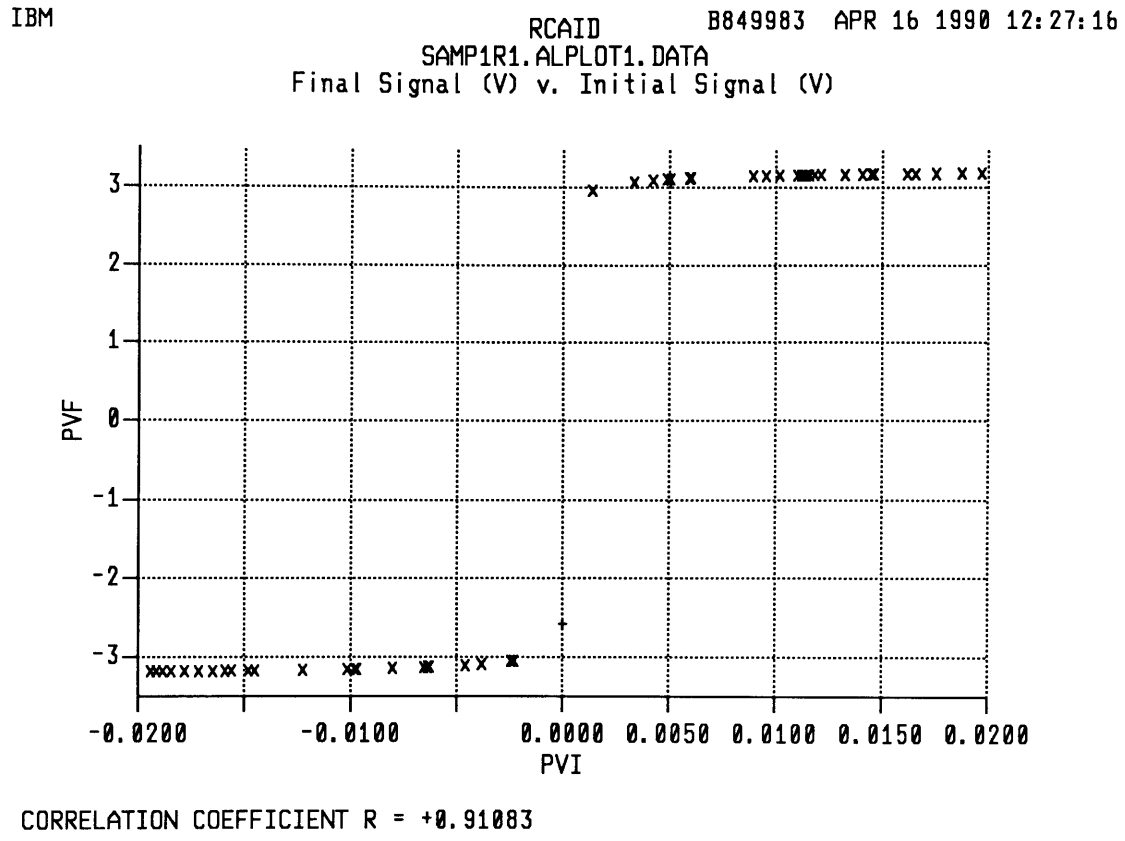

Figure 5.16: V_{DD} Sense Amplifier Signal After Sensing Operation v. Initial Signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

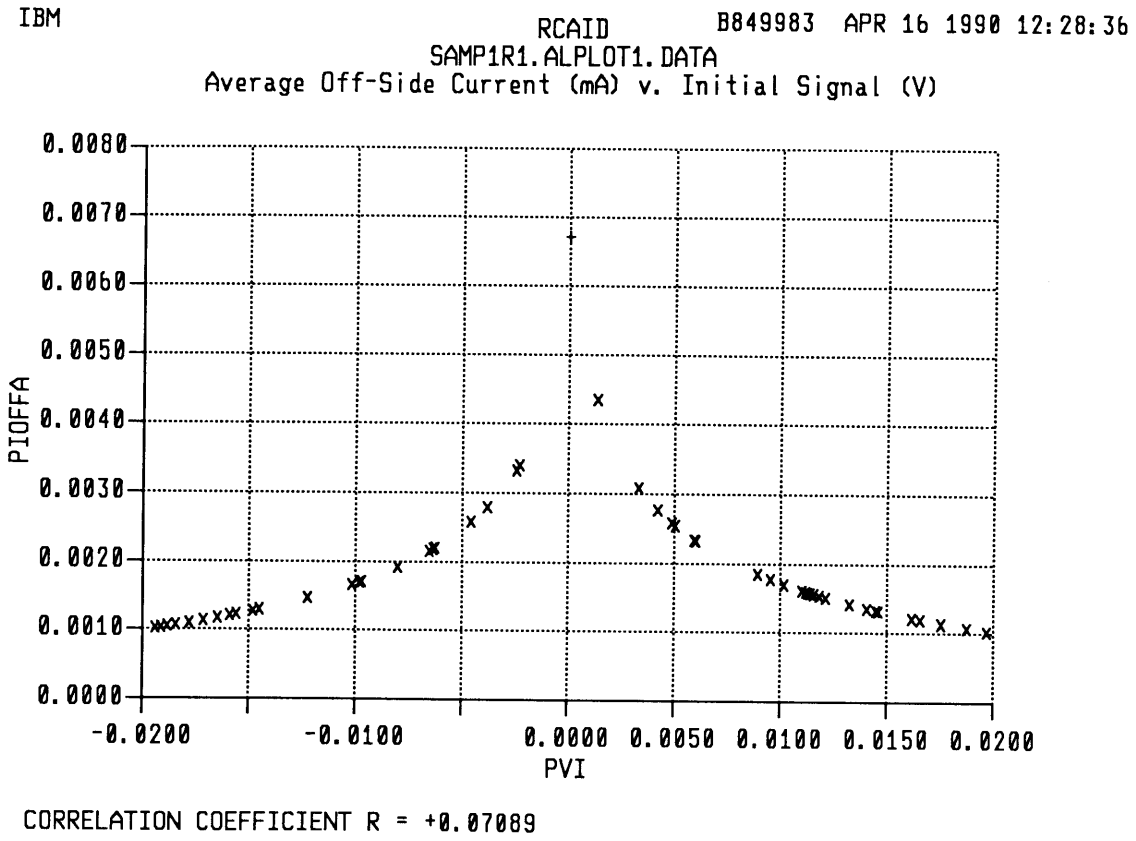

Figure 5.17: V_{DD} Sense Amplifier Average Off-Side Current v. Initial Signal. Perfectly balanced amplifier. $C_{BG} = 275$ fF. $C_{BB} = 50$ fF.

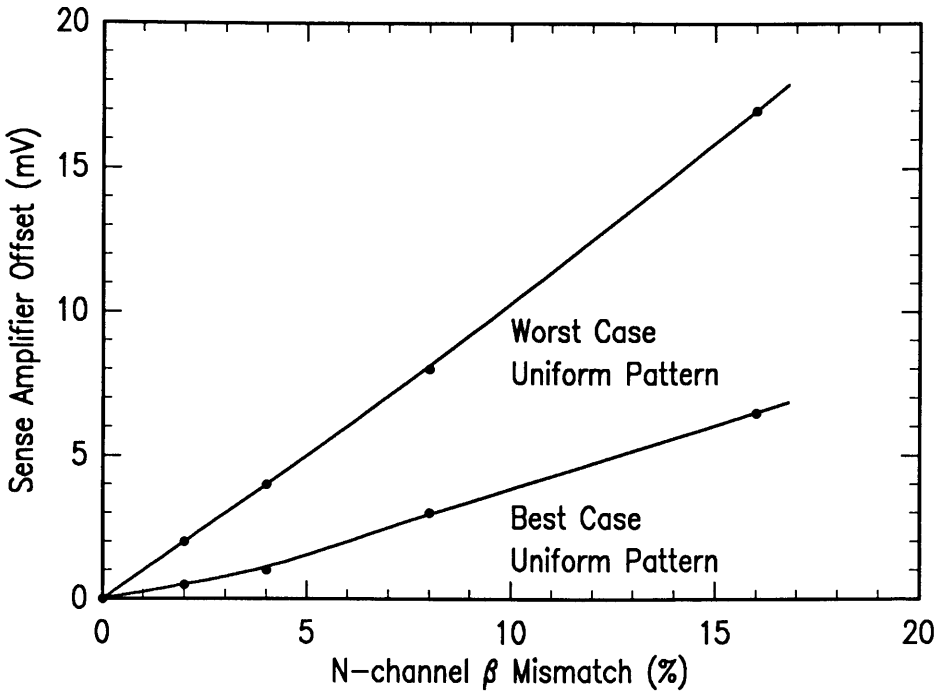

Figure 5.18: V_{DD} Sense Amplifier Offset due to Transistor Gain Mismatch

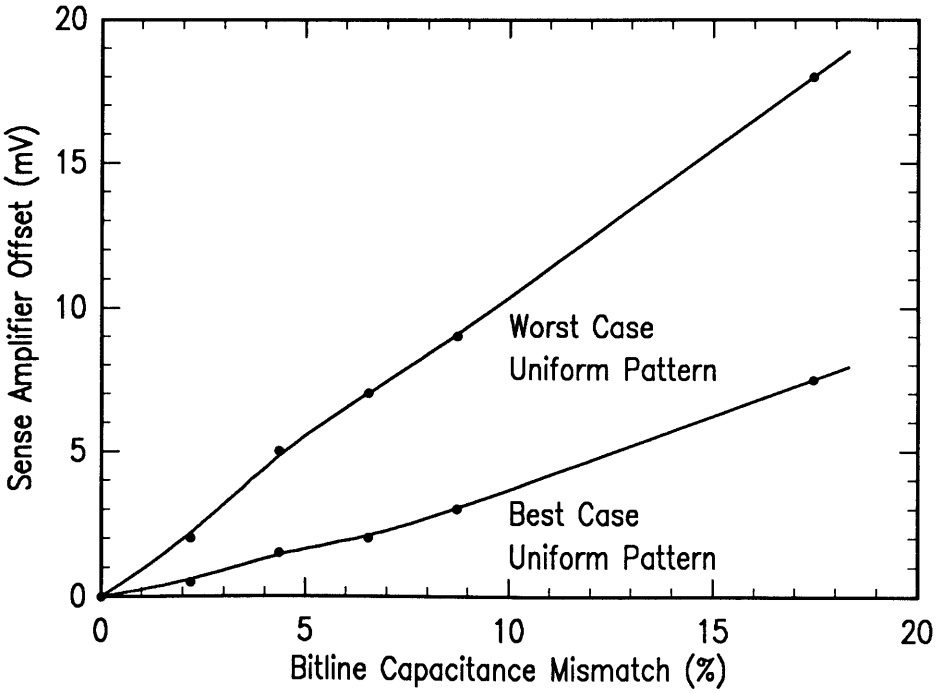

Figure 5.19: V_{DD} Sense Amplifier Offset due to Bitline Capacitance Mismatch

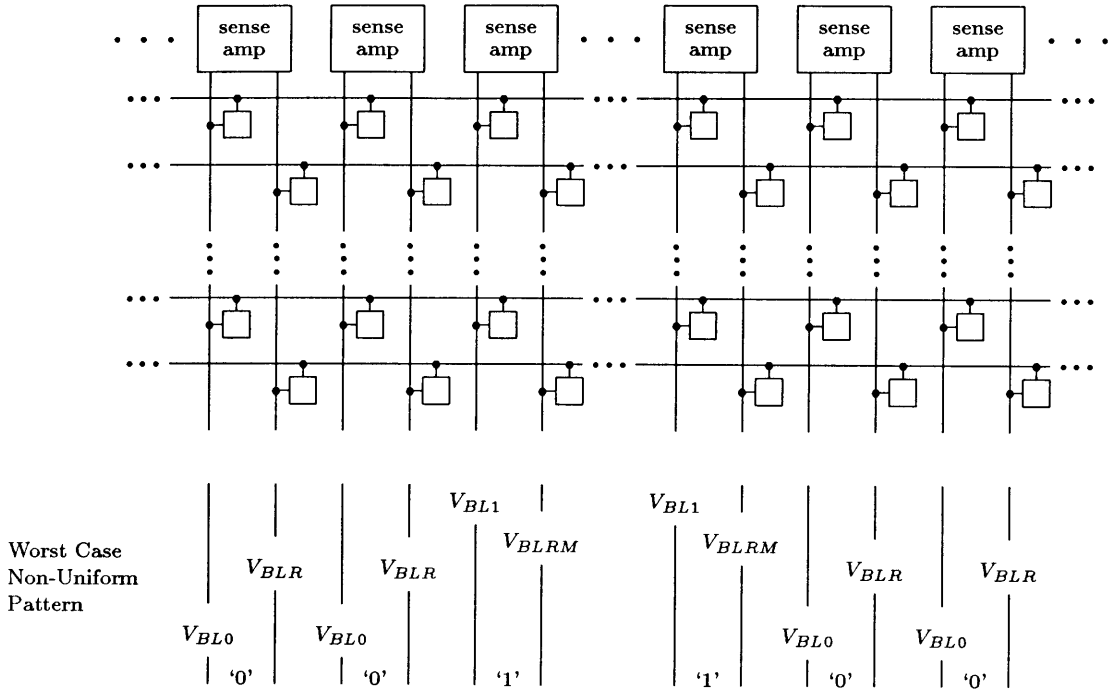

Figure 5.20: Non-Uniform Patterns for Process Variation Induced Offset Characterization

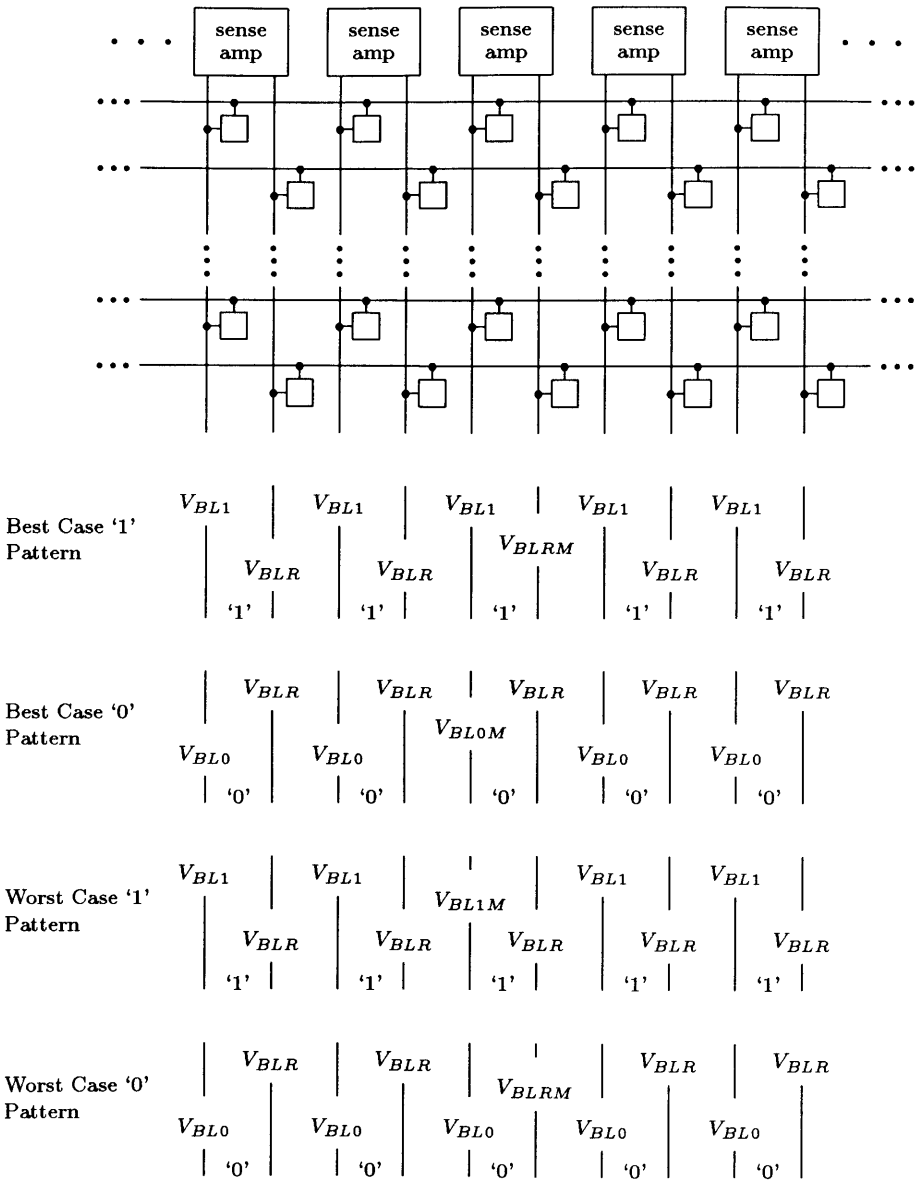

Figure 5.21: Patterns for Bitline Coupling Induced Offset Characterization

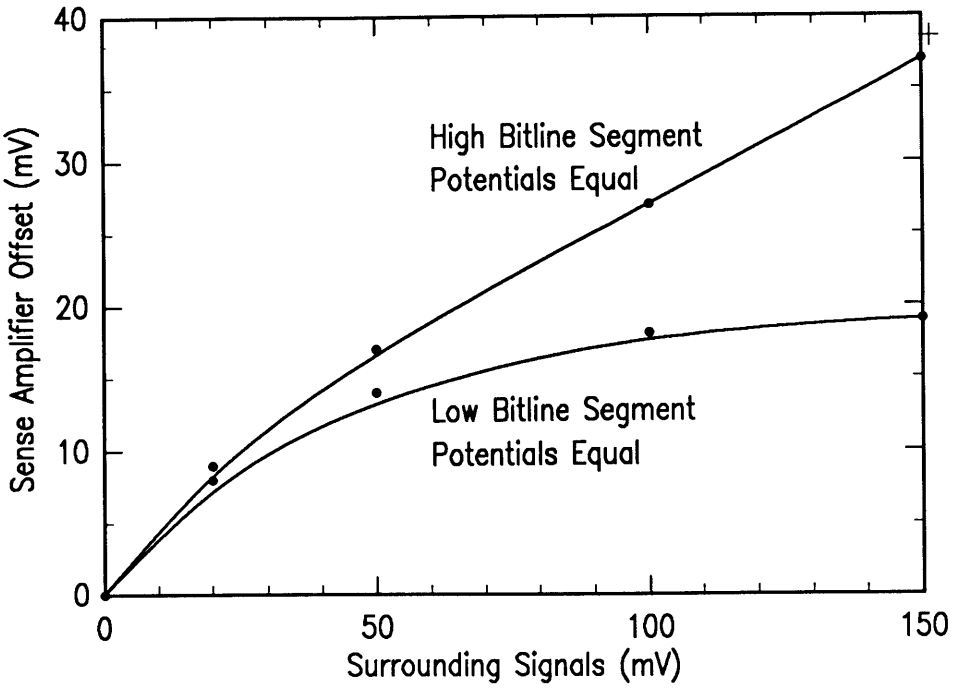

Figure 5.22: V_{DD} Sense Amplifier Offset due to Bitline-to-Bitline Coupling

Chapter 6

Conclusion

6.1 Major Accomplishments

Sense amplifier operation has been studied analytically. Signal node coupling effects were included in an optimal latching pulse derivation. Effects of process variations on sense amplifier sensitivity have been studied.

Sense amplifiers used in each major one-transistor cell DRAM generation have been analyzed. Processing technology evolution has had a major impact on sense amplifier designs. The merits of particular design approaches are critically dependent on the technology employed.

Using technology and performance projections, 64M DRAM sense amplifier design issues have been examined. Several important conclusions have been drawn:

- Intrinsic bitline charging and discharging power dissipation is extremely important. To limit this power, each bitline segment should include only 256 cells.

- In n-channel array DRAMs, bitline segments should be precharged to ground. In p-channel array DRAMs, segments should be precharged to V_{DD}.

- Isolation devices should not be employed.

6.2 Future Work

Effects of bitline-to-bitline coupling on sense amplifier sensitivity are extremely important. Yet available analyses are incomplete. The effects of bitline-to-bitline coupling on offset induced by process variations has not been sufficiently explored. In addition, effects of sense amplifier design parameters and signal patterns may be more completely characterized. Finally, the twisted bitline architecture should be carefully evaluated, paying particular attention to the added layout area and process complexity required.

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Appendix A

DRAM Chip Data

This appendix details important characteristics of published DRAMs employing one-transistor cells. Except where otherwise noted, trends presented in this thesis are based on data in this appendix.

A.1 2K, 4K, and 8K DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
General I [2]	1971	2K	250	64	4	-18,5	300	
Microsys I [32]	1975	4K				12,5		
Microsys I [33]	1975	4K	200	64		12,5		
Mostek [5]	1973	4K	300	64	4	12,5,-12	246	10.2
Philips [3]	1973	4K	400		4	-10	150	25
Philips [4]	1973	4K	300			-10	150	
TI [31]	1973	4K	300	64	2	12,5,-3		
IBM [8]	1973	8K	1730				22.5	2.5
IBM [9]	1973	8K	1730		32	-10	22.5	2.5

Table A.1: 2K, 4K, and 8K DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
General I [2]	PMOS				
Microsys I [32]	NMOS				
Microsys I [33]	NMOS	planer	poly Si	metal	diff
Mostek [5]	NMOS		poly Si	metal	
Philips [3]	PMOS	planer	poly Si	poly Si	Al
Philips [4]	PMOS				
TI [31]	NMOS				
IBM [8]	PMOS	planer	poly Si	metal	diff
IBM [9]	PMOS	planer	poly Si	metal	diff

Table A.2: 2K, 4K, and 8K DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
General I [2]		12.7	2300						64
Microsys I [32]		13.0	1250				100		
Microsys I [33]		13.0	1250			1000	120	1000	32
Mostek [5]		18.5	1480						64
Philips [3]		13.4	864				65	640	
Philips [4]		12.7					55		
TI [31]			1290				100		32
IBM [8]		18.8	1190						
IBM [9]		18.8							64

Table A.3: 2K, 4K, and 8K DRAM Features

A.2 16K DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
Hitachi [88]	1976	16K	200			12,-5	600	
Hitachi [89]	1976	16K	200			12,-5	600	
Hitachi [90]	1980	16K	100	128	2	5	400	50
Intel [34]	1976	16K	250	64			750	
Intel [35]	1976	16K	150	64		12,5,-5	480	12
Intel [36]	1976	16K	150	64	2	12,5,-5	700	12
Intel [91]	1979	16K	80			5	145	15
Mostek [39]	1977	16K				12		
Mostek [37]	1977	16K	150	128	2	12,5,-5	240	9.6
Mostek [92]	1979	16K	150	128	2	5	150	25
NTT [93]	1978	16K	65	128	2	7,-2	140	30
NTT [94]	1978	16K	65	128		7,-2	210	30
Siemens [95]	1978	16K	160	128	2	5,-5	85	
TI [96]	1976	16K	350	128	2		550	8

Table A.4: 16K DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
Hitachi [88]	NMOS				
Hitachi [89]	NMOS	planer	poly Si	Al	diff
Hitachi [90]	NMOS	stacked	poly Si	poly Si	Al
Intel [34]	NMOS	planer	poly Si	metal	diff
Intel [35]	NMOS	planer	poly Si	metal	diff
Intel [36]	NMOS	planer	poly Si	metal	diff
Intel [91]	NMOS	planer	poly Si	metal	diff
Mostek [39]	NMOS	planer	poly Si	metal	diff
Mostek [37]	NMOS				
Mostek [92]	NMOS				
NTT [93]	NMOS				
NTT [94]	NMOS	planer	mobd	mobd	mobd
Siemens [95]	NMOS	planer	poly Si	Al	diff
TI [96]	NMOS	planer	poly Si	poly Si	metal

Table A.5: 16K DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
Hitachi [88]		35	792				130	1690	
Hitachi [89]	5	35	792				140	512	64
Hitachi [90]	3	15.7	184				69.6	83.5	32
Intel [34]		21.9	455				30	500	32
Intel [35]	5	21.9	455						32
Intel [36]			455				30		32
Intel [91]		16.8				400			
Mostek [39]			435						64
Mostek [37]		17.9	435				40	800	64
Mostek [92]		20.2	342						64
NTT [93]	2	12.8	256			400			64
NTT [94]	2	12.8	256	2		400			64
Siemens [95]	3.5	8	175			600	22		64
TI [96]			632						32

Table A.6: 16K DRAM Features

A.3 64K DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
AT&T [40]	1979	64K	170	128	4	8,-5	400	12
AT&T [41]	1979	64K	170	128	4	8,-5	400	12
Fairchild [47]	1980	64K	100	256	4	5	110	18
Fujitsu [97]	1983	64K	70	128	2	5	260	20
Fujitsu [98]	1983	64K	70	128	2	5	260	20
Hitachi [14]	1980	64K	120	128		5	170	8
Hitachi [99]	1980	64K	120	128		5	170	8
Hitachi [15]	1980	64K	120	128		5	170	8
Hitachi [100]	1980	64K	150	128	2	5	200	10
Hitachi [101]	1980	64K	200			5		
Hitachi [102]	1982	64K	120			5	250	18
IBM [42]	1979	64K						
IBM [103]	1980	64K	150			8,5,-2.2		
Inmos [104]	1981	64K	100	256	4	5	300	10
Inmos [105]	1981	64K	100	256	4	5	300	10
Inmos [106]	1982	64K	100			5	350	
Intel [107]	1983	64K	70	256	4	5	140	4
Intel [108]	1983	64K	70	256	4	5	140	4
Intel [109]	1983	64K	80	256	4	5	205	12
Mitsubishi [110]	1981	64K	90	128	2	5	190	
Motorola [111]	1979	64K	150	128	2	5	300	
Natl Semic [11]	1979	64K	120	256	4	5	200	20
Natl Semic [12]	1980	64K	150	256	4	5	200	20
NEC [112]	1978	64K	110	128	2	7,-2	150	15
NEC [113]	1978	64K	140	256	2	5	250	
NEC [114]	1978	64K	150	128	2	7,-2	150	10
NTT [17]	1977	64K	200	128	2	7,-2	150	10
NTT [115]	1978	64K	200	128	2	7,-2	150	10
NTT [116]	1978	64K	200	128	2	7,-2	150	10
NTT [117]	1979	64K	75	256	4	5		
NTT [118]	1980	64K	95	256		5	150	
Siemens [13]	1979	64K	150			8,-2.5	150	
TI [45]	1978	64K	100	256	4	5	200	
TI [46]	1980	64K	150			5	200	
TI [119]	1984	64K	130	256	4	5	225	40
Toshiba [120]	1979	64K	100	256		12,-5	288	11
Toshiba [121]	1979	64K	100	256		12,-5	288	11
Toshiba [122]	1980	64K	120	128	2	5	250	20

Table A.7: 64K DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
AT&T [40]	NMOS	planer			poly Si
AT&T [41]	NMOS	planer	poly Si	metal	poly Si
Fairchild [47]	NMOS	planer	poly Si	poly Si	metal
Fujitsu [97]	NMOS				
Fujitsu [98]	NMOS			Al	diff
Hitachi [14]	NMOS	planer	poly Si	poly Si	Al
Hitachi [99]	NMOS	planer	poly Si	poly Si	Al
Hitachi [15]	NMOS	planer	poly Si	poly Si	Al
Hitachi [100]	NMOS				Al
Hitachi [101]				poly Si	Al
Hitachi [102]	NMOS				
IBM [42]	SAMOS	planer	poly Si	metal	diff
IBM [103]	NMOS	planer	poly Si	poly Si	metal
Inmos [104]	NMOS			poly Si	metal
Inmos [105]	NMOS				
Inmos [106]	NMOS	planer	poly Si	poly Si	metal
Intel [107]	nwCMOSp	planer	poly Si	poly Si	Al
Intel [108]	nwCMOSp	planer	poly Si	poly Si	Al
Intel [109]	NMOS	planer	poly Si	Al	diff
Mitsubishi [110]	NMOS	planer	poly Si	Al	poly Si
Motorola [111]	NMOS				
Natl Semic [11]	NMOS	planer	poly Si	poly Si	metal
Natl Semic [12]	NMOS	planer	poly Si	poly Si	metal
NEC [112]	NMOS	planer		poly Si	Al
NEC [113]	NMOS			poly Si	metal
NEC [114]	NMOS			poly Si	Al
NTT [17]	NMOS				
NTT [115]	NMOS	planer	poly Si	poly Si	mobd
NTT [116]	NMOS				
NTT [117]	NMOS	planer	poly Si	mobd	Al
NTT [118]	NMOS	planer	poly Si	mobd	Al
Siemens [13]	VMOS	vmos		metal	diff
TI [45]	NMOS	planer	poly Si	metal	diff
TI [46]	NMOS				
TI [119]	NMOS				
Toshiba [120]	NMOS	planer	poly Si	Al	diff
Toshiba [121]	NMOS	planer	poly Si	Al	diff
Toshiba [122]	NMOS				

Table A.8: 64K DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
AT&T [40]		40.2	238						64
AT&T [41]		40.2	238						64
Fairchild [47]	3	23.5	170	2		400	50	600	64
Fujitsu [97]	2.5	19.6	97						
Fujitsu [98]	2.5	19.6	97						
Hitachi [14]		25.8	144				38	515	64
Hitachi [99]	3	25.8	144	3		500	38	515	64
Hitachi [15]	3	25.8	144				38	515	64
Hitachi [100]	3	29.3	182						
Hitachi [101]									
Hitachi [102]	3						90		
IBM [42]									
IBM [103]	2.4	25.9	194	2.4		450			64
Inmos [104]		22.3	131						64
Inmos [105]		22.3	131						64
Inmos [106]		22	131				50		64
Intel [107]		19.7	138	1.2		250	145		
Intel [108]	1.5	19.7	137	1.2	1.1	250	145	1015	64
Intel [109]		15.3	77				58	580	128
Mitsubishi [110]	3	31.3	200	2					64
Motorola [111]	3	24.3							64
Natl Semic [11]		24	195	3.5		700			64
Natl Semic [12]		25.3	195	3.5		700	54	594	64
NEC [112]	2	33.3	270	2		400			64
NEC [113]	2	32.7	307	2		400			128
NEC [114]	2	33.3	270	2		400			64
NTT [17]		35.4	210	2		500			64
NTT [115]	2	35.4	210	2		500			64
NTT [116]	2	35.4	210	2		500			64
NTT [117]	1	9	64	1.0		300			128
NTT [118]	1	9	64	1		300			128
Siemens [13]		25.2	215				100		64
TI [45]	2.5	21.3	170	2.5		400	50	600	128
TI [46]	2.5	22.6		3					128
TI [119]	3.5	27.8	158	2.7		300			128
Toshiba [120]	4	25.5	200			750	40	600	128
Toshiba [121]	4	25.5	200			750	40	600	128
Toshiba [122]	3								64

Table A.9: 64K DRAM Features

A.4 256K DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
AT&T [123]	1982	256K	105	256	4.4	5	220	6
AT&T [124]	1982	256K	105	256	4	5	220	6
Fujitsu [125]	1983	256K	80	256	4	5	300	15
Fujitsu [126]	1983	256K	90	256	4	5	300	15
Hitachi [127]	1982	256K	150	256	4	5	250	15
Hitachi [52]	1984	256K	150			5	375	22
Hitachi [53]	1984	256K	150			5	375	22
Hitachi [128]	1984	288K	100				400	10
Hitachi [129]	1984	288K	125	256		5,-3	300	10
Hitachi [130]	1984	256K	125	256		5	250	10
IBM [131]	1982	288K		256		8.5,5,-2.2		
IBM [132]	1983	256K						
IBM [133]	1984	256K	80	256	4	5,-2.2	300	25
IBM [134]	1984	256K	80	256	4	5,-2.2	300	25
Inmos [135]	1985	256K	60	256	4	5	350	10
Intel [54]	1984	256K	100	256	4	5	225	5
Intel [55]	1984	256K	120		32	5	225	10
Intel [56]	1984	256K	100	256	4	5	225	5
Mitsubishi [136]	1983	256K	80	256	4	5	250	10
Mitsubishi [137]	1983	256K	100	256	4	5	250	12
Mitsubishi [138]	1984	256K	66			5		12
Mitsubishi [139]	1984	256K	66			5	200	12
Mitsubishi [140]	1986	256K	47			5	115	1.5
Mitsubishi [141]	1986	256K	47	256	4	5	115	1.5
Mostek [142]	1984	256K	60			5	320	
Mostek [143]	1984	256K	60			5	320	
Motorola [144]	1983	256K	90				225	15
NEC [145]	1980	256K	160	256	4	5	225	25
NEC [146]	1980	256K	160	256		5	225	25
NEC [147]	1983	256K	90	256	4	5	250	10
NEC [148]	1983	256K	90	256	4	5	250	10
NTT [149]	1980	256K	100	256		5	230	15
NTT [150]	1980	256K	100	256		5	230	15
NTT [151]	1983	256K				5/3a	200	3
NTT [152]	1983	256K	160			5/3a	200	3
Siemens [153]	1984	256K	120	256	4	5	350	15
Siemens [154]	1984	256K	100			5	300	10
Toshiba [155]	1983	256K	94	256	4	5	170	15
Toshiba [156]	1983	256K	94	256	4	5	170	15
Toshiba [157]	1984	256K	120	256	4	5	300	25

Table A.10: 256K DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
AT&T [123]	NMOS	planer	poly Si	polycide	Al
AT&T [124]	NMOS	planer	poly Si	polycide	Al
Fujitsu [125]	NMOS	planer	poly Si	Al	poly Si
Fujitsu [126]	NMOS	planer	poly Si	Al	poly Si
Hitachi [127]	NMOS	planer	poly Si	polycide	Al
Hitachi [52]	NMOS	planer	poly Si	polycide	Al
Hitachi [53]	NMOS	planer	poly Si	polycide	Al
Hitachi [128]	nwCMOSn	planer		polycide	metal
Hitachi [129]	nwCMOSn	planer		polycide	Al
Hitachi [130]	nwCMOSn	planer	poly Si	polycide	Al
IBM [131]	SAMOS	planer	poly Si	metal	diff
IBM [132]	NMOS	planer	poly Si	polycide	metal
IBM [133]	SAMOS		poly Si		
IBM [134]	SAMOS	planer	poly Si	Al	diff
Inmos [135]	nwCMOSn				
Intel [54]	nwCMOSp			poly Si	metal
Intel [55]	nwCMOSp	planer	poly Si	poly Si	Al
Intel [56]	nwCMOSp	planer	poly Si	poly Si	Al
Mitsubishi [136]	NMOS	planer	poly Si	polycide	Al
Mitsubishi [137]	NMOS			polycide	
Mitsubishi [138]	NMOS	planer	poly Si	Al	poly Si
Mitsubishi [139]	NMOS	planer	poly Si	Al	poly Si
Mitsubishi [140]	nwCMOSn				
Mitsubishi [141]	nwCMOSn	planer	poly Si	polycide	metal
Mostek [142]	NMOS				
Mostek [143]	NMOS			poly Si / metal	metal
Motorola [144]	NMOS	planer		silicide	metal
NEC [145]	NMOS	planer	poly Si		poly Si
NEC [146]	NMOS	planer	poly Si	metal	poly Si
NEC [147]	NMOS	planer	poly Si	poly Si / Al	Al
NEC [148]	NMOS	planer	poly Si	poly Si / Al	Al
NTT [149]	NMOS	planer	poly Si	mobd	Al
NTT [150]	NMOS	planer	poly Si	mobd	Al
NTT [151]	nwCMOSn	trench	poly Si	mobd	Al
NTT [152]	nwCMOSn	trench	poly Si	mobd	Al
Siemens [153]	NMOS				silicide
Siemens [154]	NMOS	planer	poly Si	metal	polycide
Toshiba [155]	NMOS	planer	poly Si	silicide	metal
Toshiba [156]	NMOS			silicide	
Toshiba [157]	NMOS	planer	poly Si	silicide	Al

Table A.11: 256K DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
AT&T [123]	2.3	54.3	117	1.7		500			
AT&T [124]	2.3	54.3	117	1.7		500	60	840	128
Fujitsu [125]	2.5	34.1	68				35	525	128
Fujitsu [126]		34.1	70	2.4			36.5	500	128
Hitachi [127]	2	46.8	98			350	50		
Hitachi [52]	2	44.1	95				52		
Hitachi [53]	2	44.1	95				52		
Hitachi [128]	2	55.0	92.5				60		128
Hitachi [129]	2	55.0	92.5						128
Hitachi [130]	2	55.0	92.5				60		
IBM [131]	2	59.1	106						128
IBM [132]	1.2	32.2	58.3	1.5			46	300	64
IBM [133]	2	50	103			320	53		64
IBM [134]	2	50				320	50		64
Inmos [135]	1.6	30.1	63				50	488	128
Intel [54]		40.8	70.4	1		250			64
Intel [55]	1.5		70	1.2	1.2	250	55		
Intel [56]		40.8	70	1.2	1.2	250	55		64
Mitsubishi [136]	2	47.5	98	1.6			42	630	128
Mitsubishi [137]	2	47.5	98	1.6			42		
Mitsubishi [138]		30.2	63.5						128
Mitsubishi [139]	1.6	30.2	63.5				50	750	128
Mitsubishi [140]	1.2	21.3	35.6						
Mitsubishi [141]	1.2	21.3	35.6	1.3	1.8	250	45		
Mostek [142]	2.1	46.8	76.2	1.2		300	40	600	
Mostek [143]		46.8	76.2	1.2			40	600	
Motorola [144]	2	46.2	84						64
NEC [145]	1.5	41.6	71.2	1.5		400	35	700	128
NEC [146]	1.5	41.6	71.2	1.5		400	35	700	128
NEC [147]	1.3	34	66.5	1.3		160	50		
NEC [148]	1.3	34	66.5				50		
NTT [149]	1	34.4	69.2	1.2		300			128
NTT [150]	1	34.4	69.2	1.3		300			128
NTT [151]		30.8	35.3	0.5	0.9	150			
NTT [152]		30.8	35.3	0.5	0.9	150	40		128
Siemens [153]	2.5	45	90	1.8		400	55		
Siemens [154]	2.5	45	90	1.8		400	55		128
Toshiba [155]	2	46	76.8			350	40	400	64
Toshiba [156]	2	46	76.8			350			
Toshiba [157]	2	46.0	76.8			350			

Table A.12: 256K DRAM Features

A.5 1M DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
AT&T [158]	1985	1M	80	512	8.8	5	160	0.5
Fujitsu [159]	1985	1M	90	512	8	5	350	15
Hitachi [160]	1987	1M	35	512	8	5/4i	450	30
Hitachi [161]	1987	1M	32	512	8	5/4i	450	
Hitachi [162]	1984	1M	90	512	8	5	300	10
Hitachi [163]	1984	1M	90	512	8	5	300	10
Hitachi [164]	1985	1M	74	512	8	5	230	7
Hitachi [165]	1986	1M	100	512	8	5	250	10
IBM [166]	1984	1M	150	256		5		
IBM [167]	1985	1M	80	512	4	5	625	50
IBM [168]	1985	1M	80	512	4	5	625	50
IBM [169]	1989	1M	27	1024	8	5	450	20
IBM [170]	1989	1M	27	1024	8	5	500	
Intel [171]	1986	1M	65		8	5		0.25
Matsushita [172]	1986	1M		512	2	5		
Mitsubishi [173]	1985	1M	90	512	8	5	350	15
Mitsubishi [174]	1985	1M	90	512	8	5	350	15
Mitsubishi [175]	1987	1M	62	512	8	5	240	4
Mitsubishi [176]	1990	1M	80					
Mostek [177]	1985	1M		512	8	5		
Mostek [178]	1985	1M	85	512	8	5	225	2.5
NEC [179]	1984	1M	120	256	4	5	290	15
NEC [180]	1984	1M	120	256	4	5	290	
NEC [181]	1985	1M	85			5		
NTT [182]	1984	1M	140			5	250	5
NTT [183]	1984	1M	140	512	8	5	250	5
TI [62]	1986	1M				5		
TI [61]	1986	1M		512	8	5	225	4
Toshiba [184]	1985	1M	70	512	8	5	270	15
Toshiba [185]	1986	1M		512	8	5	270	15
Toshiba [60]	1985	1M	56	512	8	5	300	15
Toshiba [58]	1985	1M	56	512	8	5	150	3.5
Toshiba [59]	1985	1M	56	512	8	5	150	1.0
Toshiba [186]	1986	1M	56			5	175	0.25
Toshiba [187]	1986	1M	56			5	175	0.25
Toshiba [188]	1986	1M	62			5	105	0.15
Toshiba [189]	1986	1M	62				105	2

Table A.13: 1M DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
AT&T [158]	twCMOSn				
Fujitsu [159]	NMOS	stacked	poly Si	polycide	Al
Hitachi [160]	twBiCMOSn	planer		polycide / Al	Al
Hitachi [161]	twBiCMOSn	planer			
Hitachi [162]	NMOS	trench	poly Si	poly Si	Al
Hitachi [163]	NMOS	trench	poly Si	poly Si	Al
Hitachi [164]	nwCMOSn			polycide	metal
Hitachi [165]	nwCMOSn	planer	poly Si	Al	Al
IBM [166]	SAMOS	planer	poly Si	metal	diff
IBM [167]	NMOS				
IBM [168]	NMOS	planer	poly Si	silicide	metal
IBM [169]	nwCMOSp	planer			
IBM [170]	nwCMOSp	planer	poly Si	poly Si / Al	Al
Intel [171]	CMOSp	planer			
Matsushita [172]	NMOS				
Mitsubishi [173]	NMOS	planer	poly Si	polycide	Al
Mitsubishi [174]	NMOS	planer	poly Si	polycide	Al
Mitsubishi [175]	nwCMOSn	planer	poly Si	polycide	metal
Mitsubishi [176]	twCMOS				
Mostek [177]	CMOSn	planer	poly Si	metal	poly Si
Mostek [178]	twCMOSn	planer	poly Si	metal	poly Si
NEC [179]	NMOS				Al
NEC [180]	NMOS			poly Si / Al	Al
NEC [181]	NMOS	trench			
NTT [182]	nwCMOSn	trench	poly Si	Mo-poly	Al
NTT [183]	nwCMOSn	trench	poly Si	Mo-poly	Al
TI [62]	twCMOSn	trench	poly Si	polycide	diff
TI [61]	twCMOSn	trench			
Toshiba [184]	NMOS	planer	poly Si	poly Si / Al	Al
Toshiba [185]	NMOS	planer	poly Si	poly Si / Al	Al
Toshiba [60]	nwCMOSn	planer	poly Si	poly Si / Al	polycide
Toshiba [58]	nwCMOSn		poly Si		polycide
Toshiba [59]	nwCMOSn	planer	poly Si	poly Si / Al	polycide
Toshiba [186]	nwCMOSn				
Toshiba [187]	nwCMOSn	planer	poly Si	poly Si / Al	polycide
Toshiba [188]	twCMOSn	planer	poly Si	poly Si / Al	Al
Toshiba [189]	twCMOSn	planer			

Table A.14: 1M DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
AT&T [158]	1.3	69.6	36.7						
Fujitsu [159]	1.4	54.7	26.5	1.8			55		
Hitachi [160]	1.3	74.5	36.0	1.2	1.2	200	40	300	
Hitachi [161]	1.3	74.5	36.0				40	300	
Hitachi [162]		46.0	21	1.6			60	290	
Hitachi [163]		46.0	21	1.6		200	60	290	
Hitachi [164]		47.3	24.1						
Hitachi [165]	1.3	64.0	36						
IBM [166]	1.25	80.8	42.8						64
IBM [167]	1.5	57.8	36.1				37	385	
IBM [168]		57.8	36.1			250	37	385	128
IBM [169]	1	82.8	39.6	1		235			64
IBM [170]	1	83.6	39.6	1					64
Intel [171]	1	50.8	28.5	1	1	250			
Matsushita [172]	1.2	65.9	35.1						
Mitsubishi [173]	1.2	65.0	35.7				45	495	
Mitsubishi [174]	1.2	65.0	35.7	1.5			45	495	
Mitsubishi [175]	1.0	65.5	29.9	1.2	1.5	250			
Mostek [177]	1.2	68.1	36.0	0.9	0.7	225			
Mostek [178]	1.2	68.1	36	0.9	0.7	225	32		64
NEC [179]	1	75.9	44				50	700	
NEC [180]	1	75.9	44				50	700	128
NEC [181]	1.0	43.2	20.4	1.5		300	60		
NTT [182]	0.8	52.5	20.0	0.5	0.9	150	30	270	
NTT [183]	0.8	52.5	20	0.5	0.9	150	30	270	64
TI [62]	1.0	50.3	21.2			200	50	400	
TI [61]	1.0	50.3	21.2			200			
Toshiba [184]	1.2	63.2	32.0				70	420	
Toshiba [185]	1.2	63.2	32.0	1.2		200	70	420	
Toshiba [60]	1.2	62.5	34.2	1.2	1.6	250	42		128
Toshiba [58]	1.2	62.5	34.2						128
Toshiba [59]	1.2	62.5	34.2	1.2	1.6	250	42		128
Toshiba [186]	1.2	54.2	29.2						
Toshiba [187]	1.2	54.2	29.2	1.2	1.6	250	40		
Toshiba [188]	1.2	82.7	29.4	1.0	1.2	200			64
Toshiba [189]	1.2	82.7	29.4	1.0	1.2	200			64

Table A.15: 1M DRAM Features

A.6 4M DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
Fujitsu [190]	1987	4M	70	1024	16	5	200	4.5
Fujitsu [191]	1990	4M				5	780	
Hitachi [192]	1987	4M	76	1024	16	5	225	0.5
Hitachi [193]	1987	4M	65	1024		5	225	0.5
Hitachi [194]	1987	4M	65	1024		5	225	0.5
IBM [195]	1987	4M	65			3.3	363	6.6
Matsushita [196]	1987	4M						
Matsushita [197]	1987	4M	60	1024		5	250	3
Matsushita [198]	1988	4M	70	256	16	5/3i	400	15
Mitsubishi [199]	1987	4M	90	1024		5	300	2.5
Mitsubishi [200]	1987	4M	90	1024		5	300	
Mitsubishi [201]	1990	4M	38	4096	256	5	350	1.0
NEC [202]	1986	4M	95	1024	16	5/4a	425	15
NEC [203]	1986	4M	95	1024		5/4a	425	15
Oki [204]	1987	4M	60			5	325	5
Siemens [205]	1988	4M	60	1024	16	5	350	5
TI [206]	1986	4M	170			5	500	40
TI [207]	1986	4M	150			5	375	10
Toshiba [63]	1986	4M	80	1024		5/3.5i	300	2.5
Toshiba [64]	1986	4M	80	1024		5/3.5i	300	2.5
Toshiba [208]	1987	4M	60	1024	16	5	250	1.0
Toshiba [209]	1987	4M	60	1024	16	5	250	1.0

Table A.16: 4M DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
Fujitsu [190]	nwCMOSn	stacked	poly Si	poly Si / metal	polycide
Fujitsu [191]	nwCMOS	stacked			
Hitachi [192]	twCMOS	stacked	poly Si	poly Si	Al
Hitachi [193]	twCMOSn	stacked			
Hitachi [194]	twCMOSn				
IBM [195]	nwCMOSp	trench	sub	silicide	
Matsushita [196]	twCMOS	trench			
Matsushita [197]	twCMOSn	trench	poly Si	poly Si / Al	polycide
Matsushita [198]	CMOSn	trench	poly Si	polycide	Al
Mitsubishi [199]	twCMOSn	trench	poly Si	polycide / Al	polycide
Mitsubishi [200]	twCMOSn	trench	poly Si	polycide / Al	polycide
Mitsubishi [201]	twCMOS	stacked			
NEC [202]	NMOS	trench	sub	polycide	Al
NEC [203]	NMOS	trench	sub	polycide	Al
Oki [204]	nwCMOS	trench			
Siemens [205]	CMOS	trench	poly Si		
TI [206]	twCMOSn	trench	sub	poly Si / metal	diff
TI [207]	twCMOSn	trench	sub	poly Si / metal	diff
Toshiba [63]	twCMOSn	trench			
Toshiba [64]	twCMOSn	trench	poly Si	poly Si / Al	polycide
Toshiba [208]	twCMOSn	trench			
Toshiba [209]	twCMOSn	trench	poly Si	poly Si / Al	polycide

Table A.17: 4M DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
Fujitsu [190]	0.7	63.7	7.5						
Hitachi [192]	0.8	111	14.7						
Hitachi [193]	0.8	111	14.7	1.2					
Hitachi [194]	0.8	111	14.7						
IBM [195]	0.8	78	11						
Matsushita [196]	0.8	95.6	10.1				90		128
Matsushita [197]	0.8	67.1	8.0	0.8	1.1	170	40		256
Matsushita [198]	0.8	95.6	10.1				90		128
Mitsubishi [199]	0.8	72.3	10.9				50		
Mitsubishi [200]	0.8	72.3	10.9				50		128
NEC [202]	0.8	99.2	10.6				50	400	
NEC [203]	0.8	99.2	10.6	1.0			50	400	128
Oki [204]	1	149	16.8				40		
Siemens [205]	0.9	91.3	10.6	0.75	0.60	200			128
TI [206]	1	100	8.8	1.0	1.0				
TI [207]	1	100	8.8	1.0	1.0				64
Toshiba [63]	1.0	137	17.4	1.0	1.4		40		
Toshiba [64]	1	137	17.4	1.0	1.4	200	40	600	
Toshiba [208]	0.9	111	13.8						
Toshiba [209]	0.9	111	13.8	1.0	1.2				

Table A.18: 4M DRAM Features

A.7 16M DRAM Chip Data

Company [Ref]	Year	Chip Cap. (bits)	Access Time (ns)	Refresh Cycles	Refresh Time (ms)	Supply Voltage(s)	Active Power (mW)	Standby Power (mW)
Hitachi [70]	1988	16M	60	2048		5/3.3a	420	15
Hitachi [68]	1988	16M	60	2048		5/3.3a	420	15
IBM [210], [211]	1990	16M	50	2048		5or3/?i		
Matsushita [212]	1988	16M	65			5/4i/3a	450	5
Matsushita [213]	1988	16M	65			5/4i/3a	450	5
Mitsubishi [71]	1989	16M	60	2048	32	3.3	297	0.66
Mitsubishi [72]	1989	16M	60	2048	32	3.3	297	0.66
NEC [214]	1989	16M	55	2048	32	5/3.3a	400	10
NTT [74]	1987	16M	80			3.3	500	
Oki [73]	1989	16M	60	2048	32	5/4i	425	2.5
Samsung [215]	1989	16M	65	2048	32	5/4i	400	5
Samsung [216]	1989	16M	65	2048	32	5/4i	400	5
Toshiba [217]	1988	16M	70	2048	32	5/4i	600	
Toshiba [218]	1989	16M	70	2048	32	5/4i	600	
Toshiba [76]	1989	16M	45			5/4i	325	2.5
Toshiba [77]	1989	16M	45			5/4i	325	2.5

Table A.19: 16M DRAM Performance Specifications

Company [Ref]	Tech.	Cell Structure	Plate-Line Material	Word-Line Material	Bit-Line Material
Hitachi [70]	twCMOS	stacked			
Hitachi [68]	twCMOS	stacked		poly Si / Al	silicide
IBM [210], [219]	CMOS	trench	sub	polycide	metal
Matsushita [212]	nwCMOSn	trench	poly Si	poly Si / Al	polycide
Matsushita [213]	nwCMOSn	trench	poly Si	poly Si / Al	polycide
Mitsubishi [71]	twCMOSn	stacked	poly Si	polycide / Al	tungsten
Mitsubishi [72]	twCMOSn	stacked	poly Si	polycide / Al	tungsten
NEC [214]	CMOSn	stacked			
NTT [74]	nwCMOSn	trench		poly Si / Al	silicide
Oki [73]	twCMOSn	trench			polycide
Samsung [215]	twCMOSn	stacked			
Samsung [216]	twCMOSn	stacked	poly Si		
Toshiba [217]	twCMOSn	trench			
Toshiba [218]	twCMOSn	trench	poly Si	poly Si / Al	polycide
Toshiba [76]	twCMOSn	trench			
Toshiba [77]	twCMOSn	trench	poly Si	poly Si / Al	poly Si

Table A.20: 16M DRAM Process Technologies

Company [Ref]	Feat Size (μm)	Chip Area (mm^2)	Cell Area (μm^2)	NFET Len. (μm)	PFET Len. (μm)	Tox (Å)	Cell Cap. (fF)	BLseg Cap (fF)	Cells per BLseg
Hitachi [70]	0.6	142	4.16				33		
Hitachi [68]	0.6	142	4.16	0.6	0.9	150	33	300	
IBM [210]	0.5	141	4.13				100	322	256
Matsushita [212]	0.5	93.8	3.3	0.4	0.7	100	50		256
Matsushita [213]	0.5	93.8	3.3	0.4	0.7	100	63	380	256
Mitsubishi [71]	0.5	135	4.8	0.6	0.8				128
Mitsubishi [72]	0.5	135	4.8	0.6	0.8		35	210	128
NEC [214]	0.55	130	4.05						
NTT [74]	0.7	148	4.88	0.5	0.7	120	70	420	
Oki [73]	0.55	128	4.06	0.8	1.1	160	30	270	128
Samsung [215]	0.6	157	5.59				30		
Samsung [216]	0.6	157	5.59	0.8	1.0	160	30	300	128
Toshiba [217]	0.7	210	6.12	0.5	0.5		30		
Toshiba [218]	0.7	210	6.12	0.5	0.5		37		
Toshiba [76]	0.6	137	4.8	0.7	0.9				
Toshiba [77]	0.6	137	4.8	0.7	0.9	150	30	240	128

Table A.21: 16M DRAM Features

Appendix B

Sense Amplifier Layouts

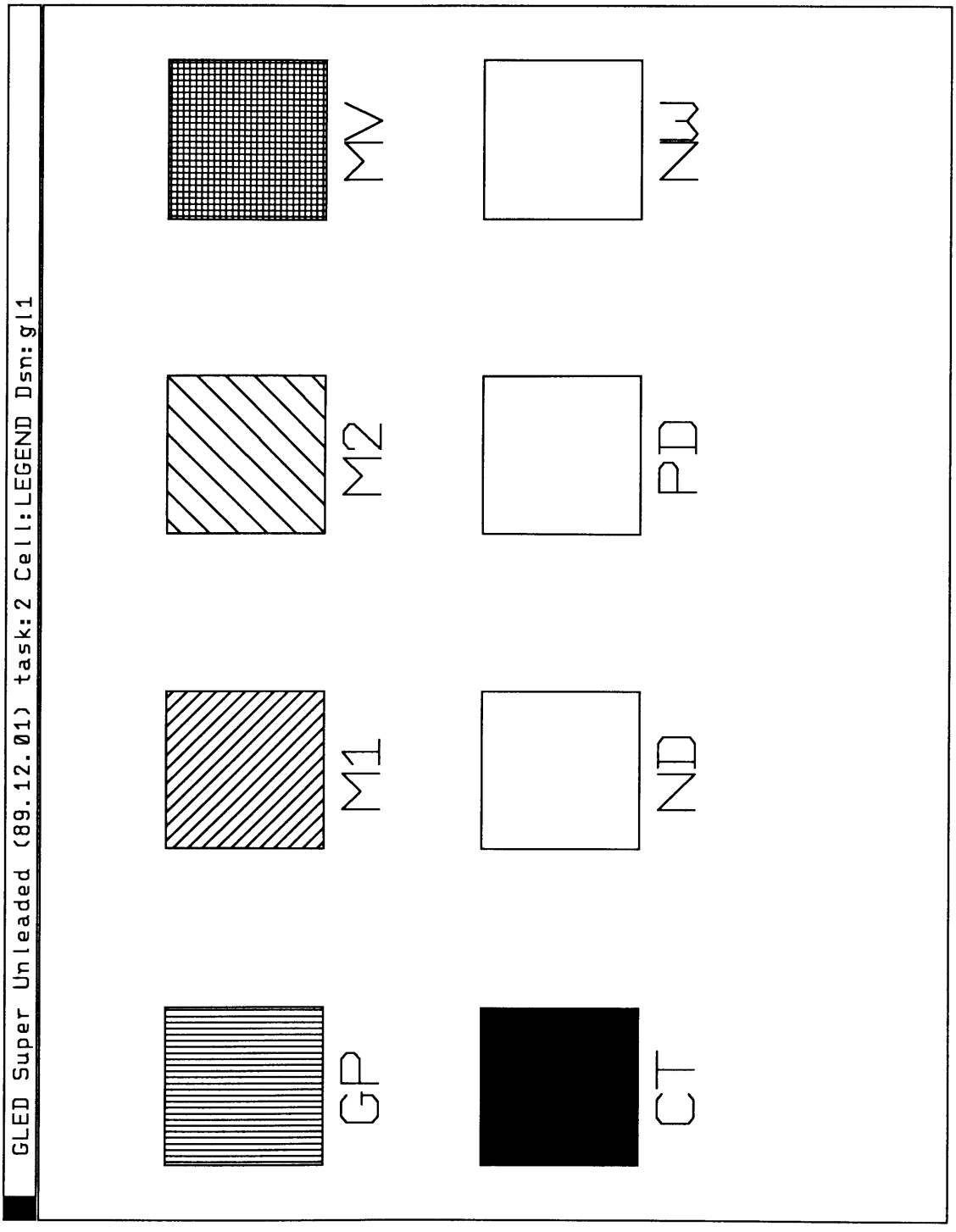

Figure B.1: Layout Legend

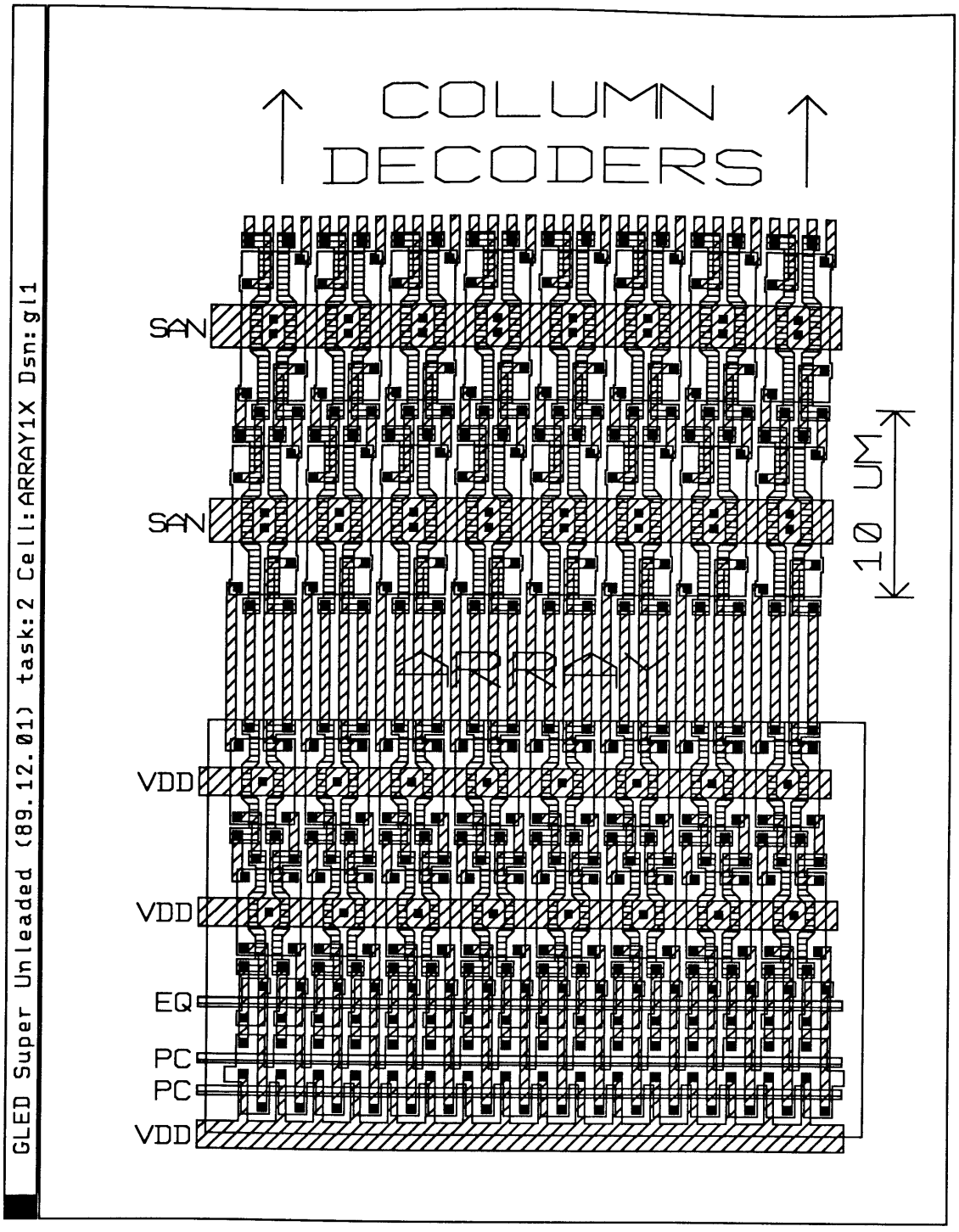

Figure B.2: V_{DD} Sense Amplifier Layout

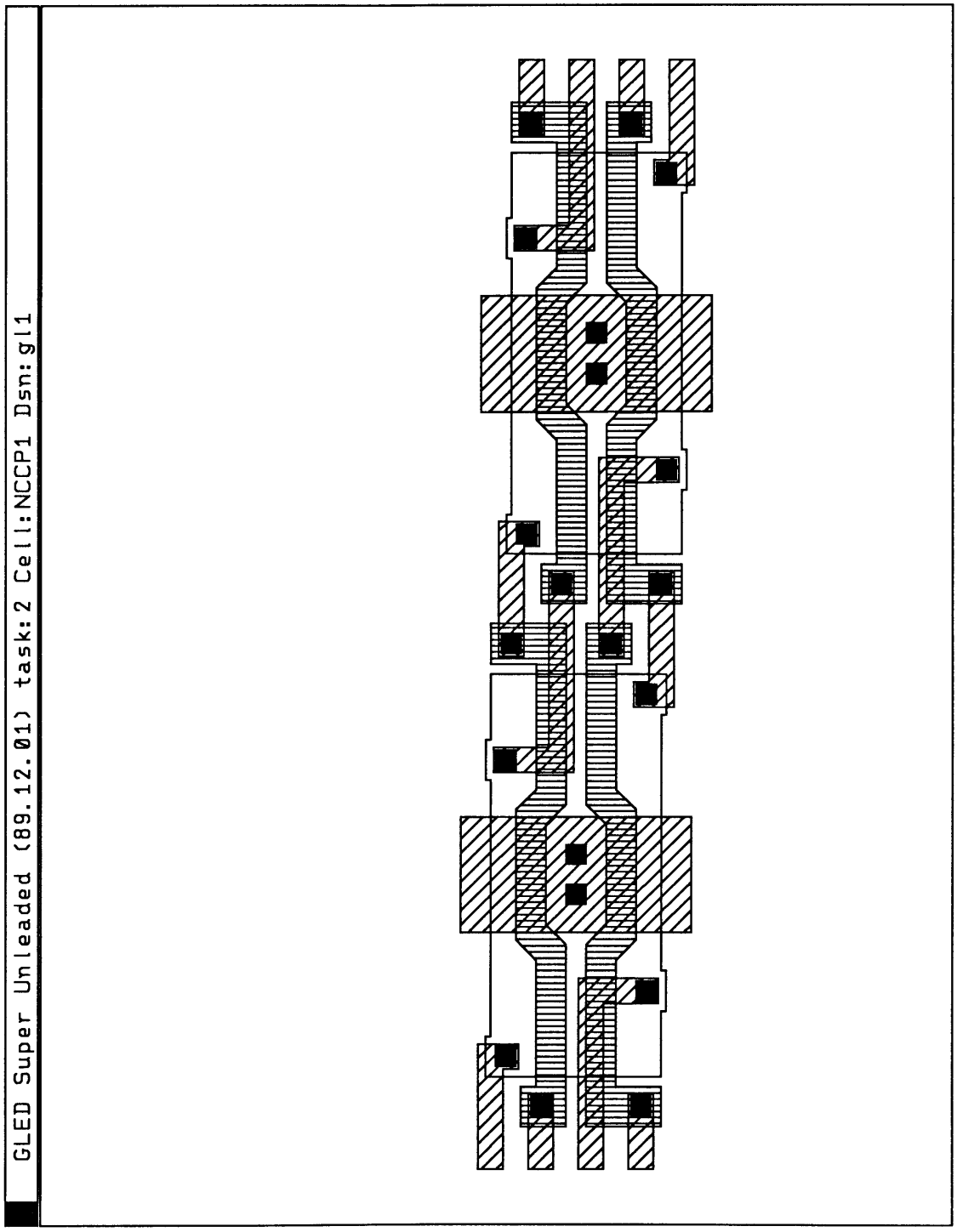

Figure B.3: V_{DD} Sense Amplifier n-channel Cross-Coupled Pair Layout

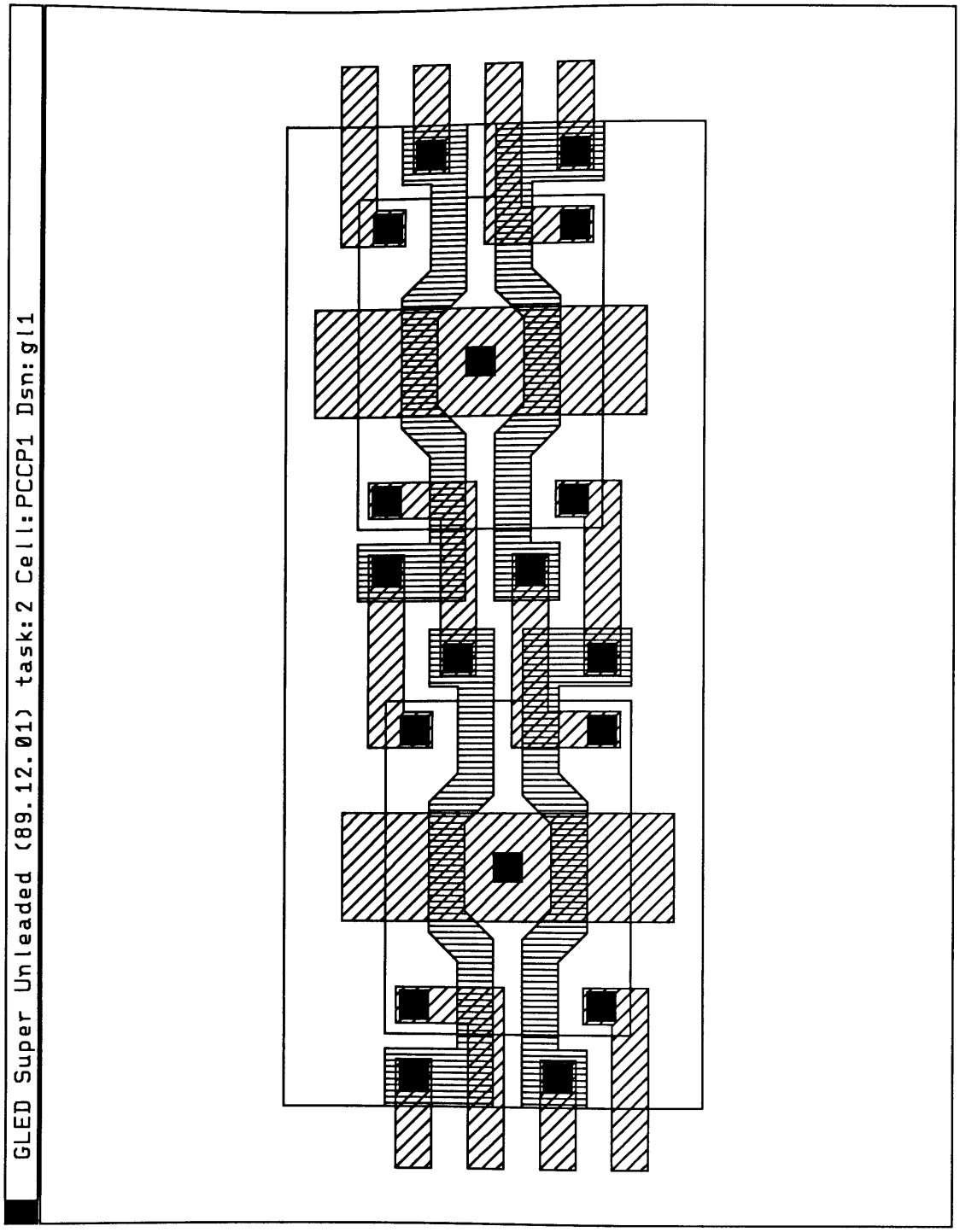

Figure B.4: V_{DD} Sense Amplifier p-channel Cross-Coupled Pair Layout

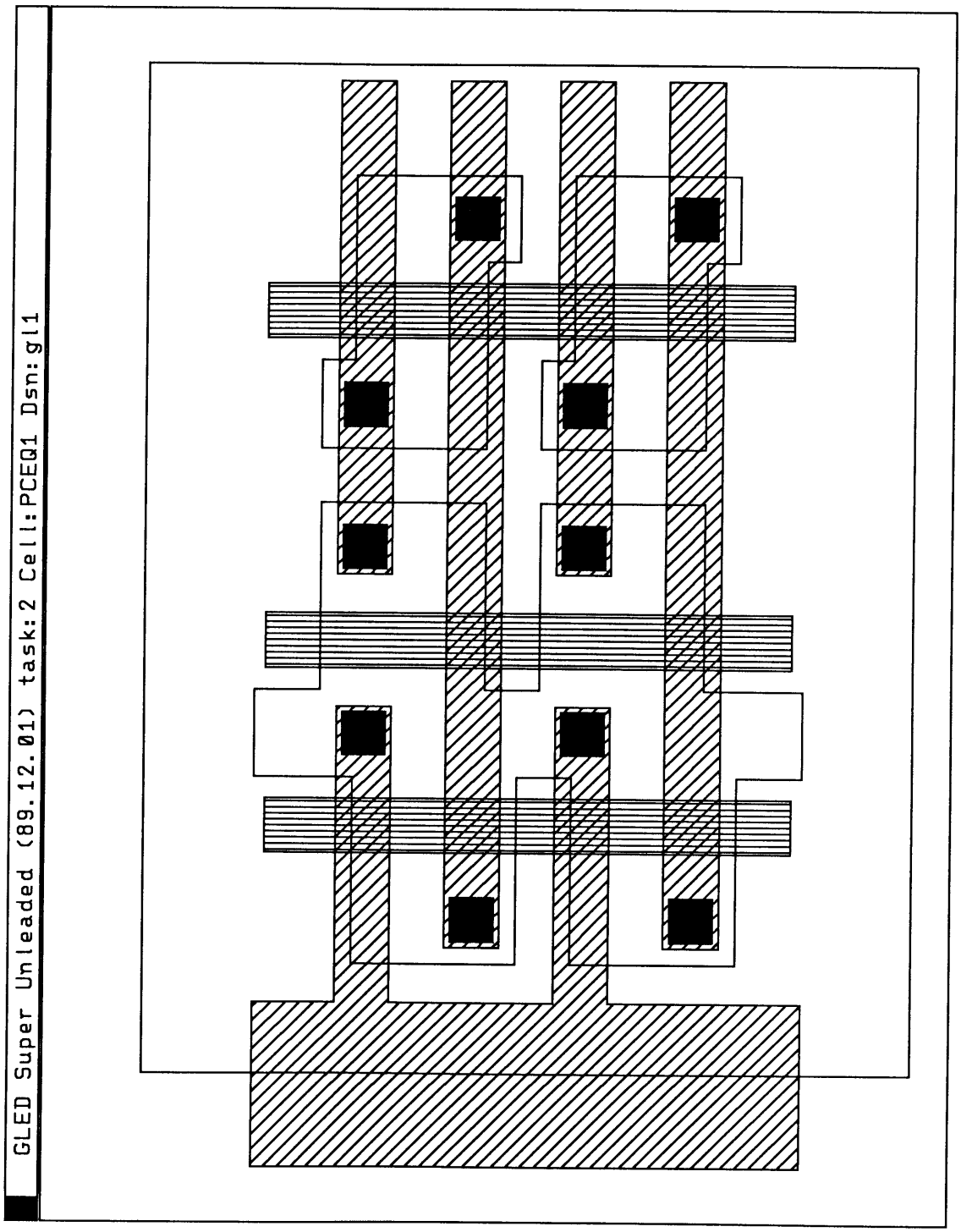

Figure B.5: V_{DD} Sense Amplifier Precharge and Equalization Device Layout

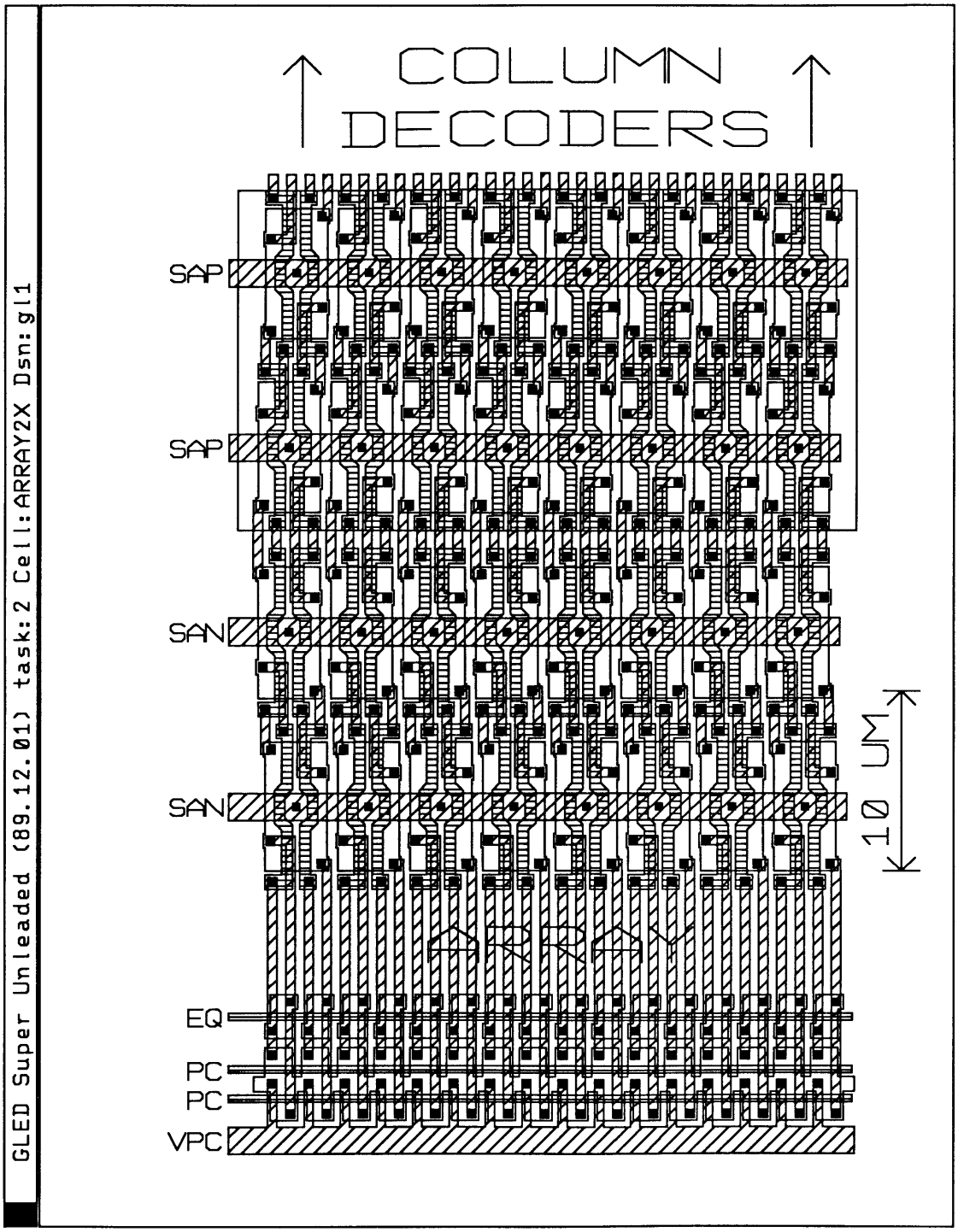

Figure B.6: $1/2\ V_{DD}$ Sense Amplifier Layout

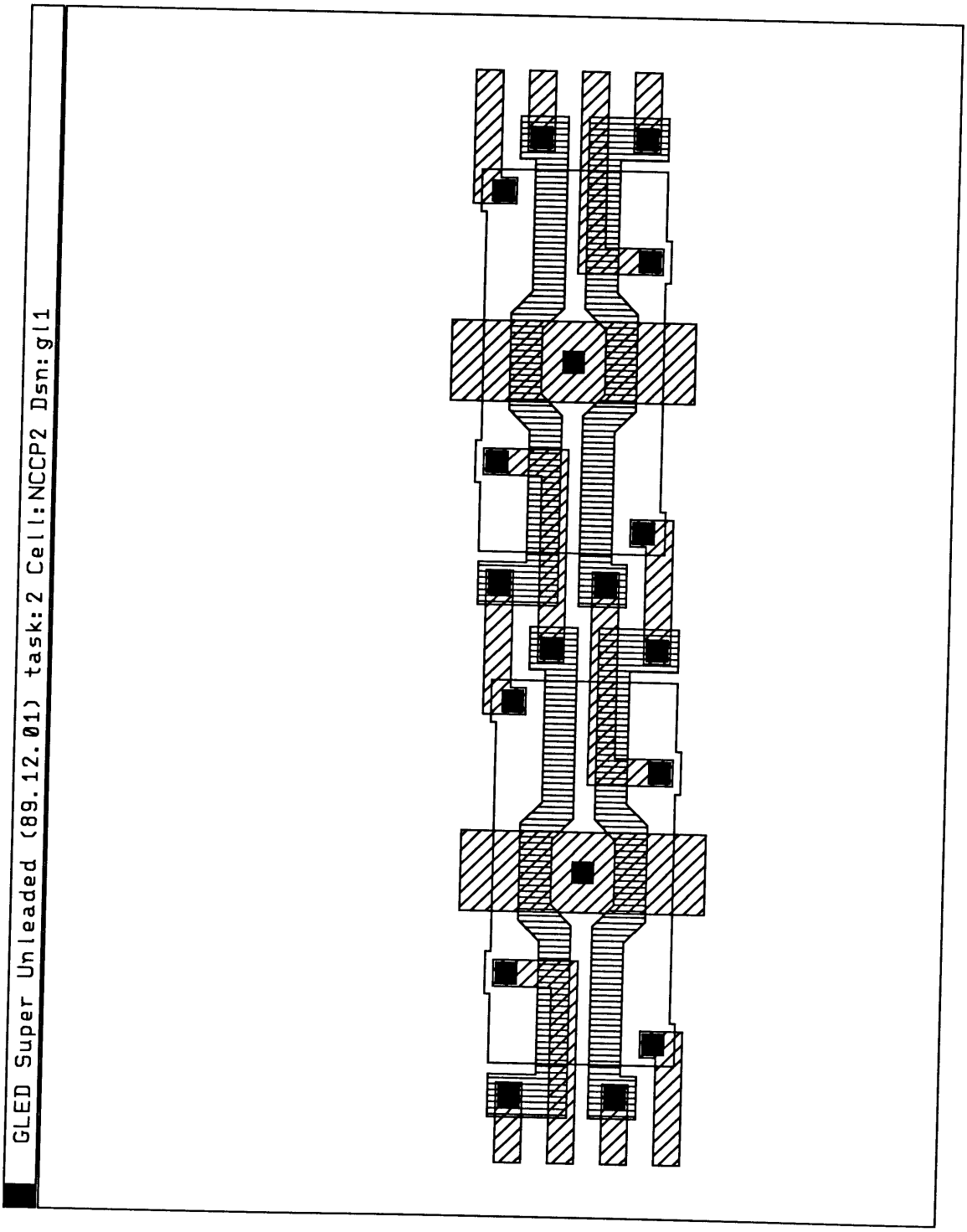

Figure B.7: 1/2 V_{DD} Sense Amplifier n-channel Cross-Coupled Pair Layout

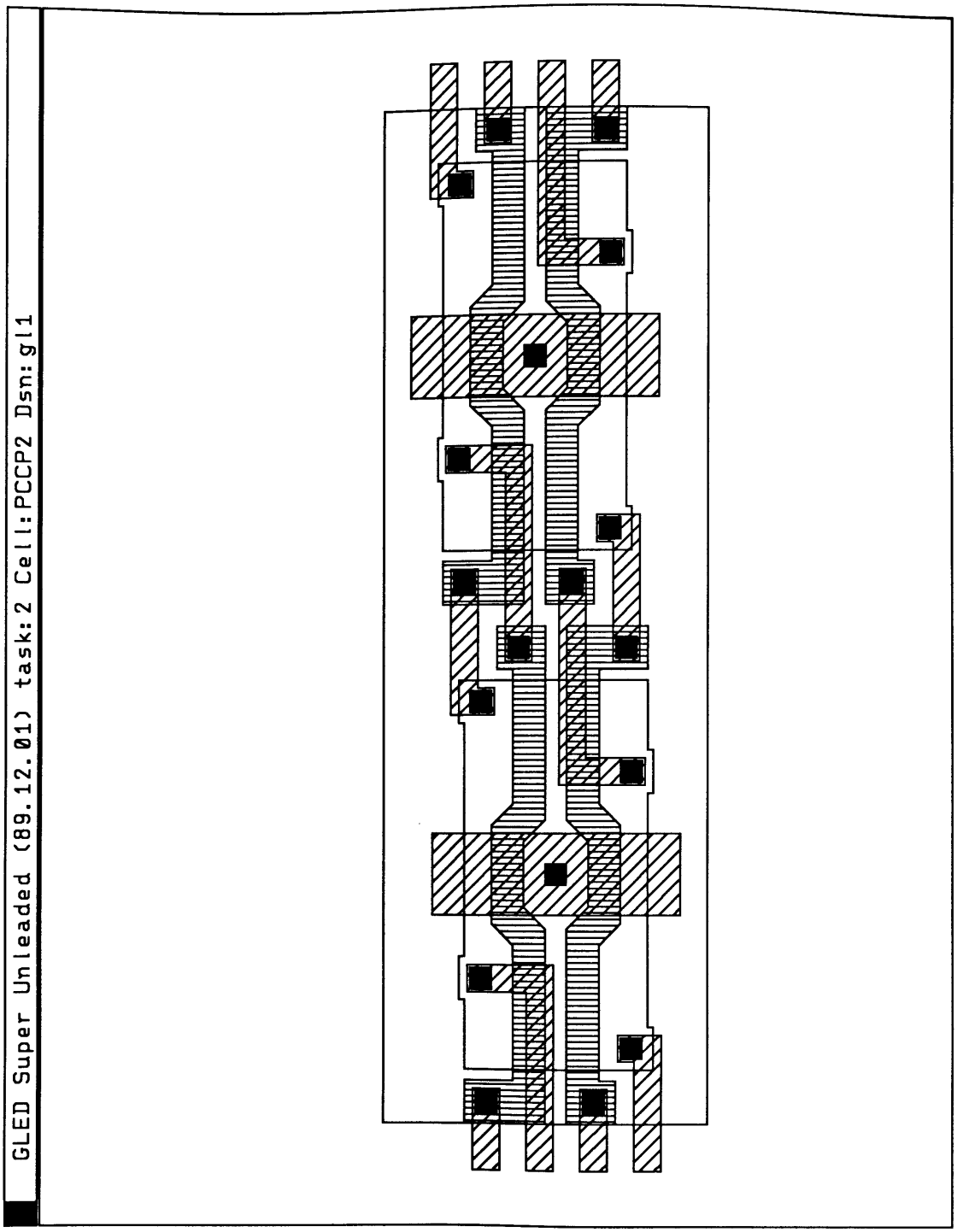

Figure B.8: $1/2\ V_{DD}$ Sense Amplifier p-channel Cross-Coupled Pair Layout

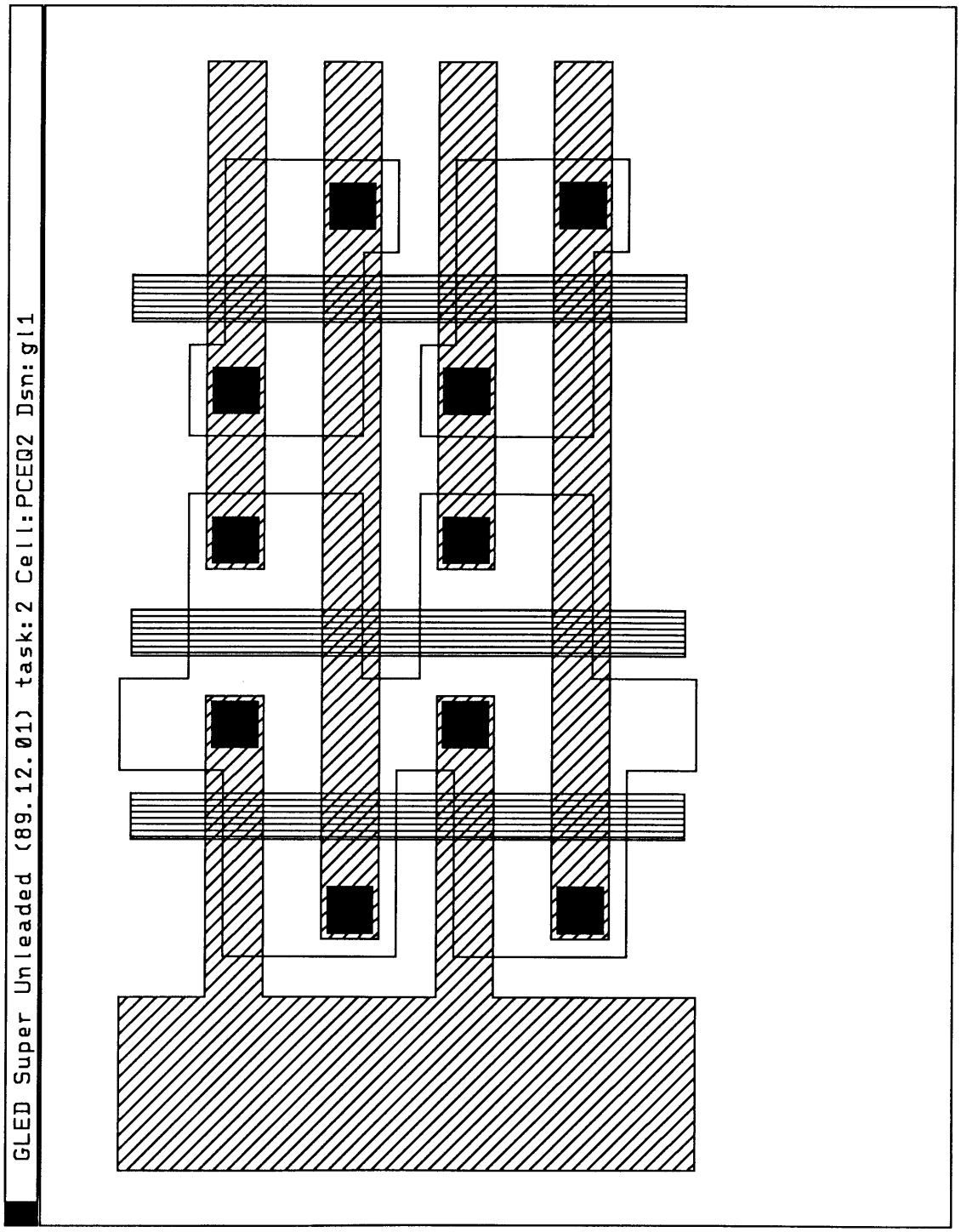

Figure B.9: 1/2 V_{DD} Sense Amplifier Precharge and Equalization Device Layout

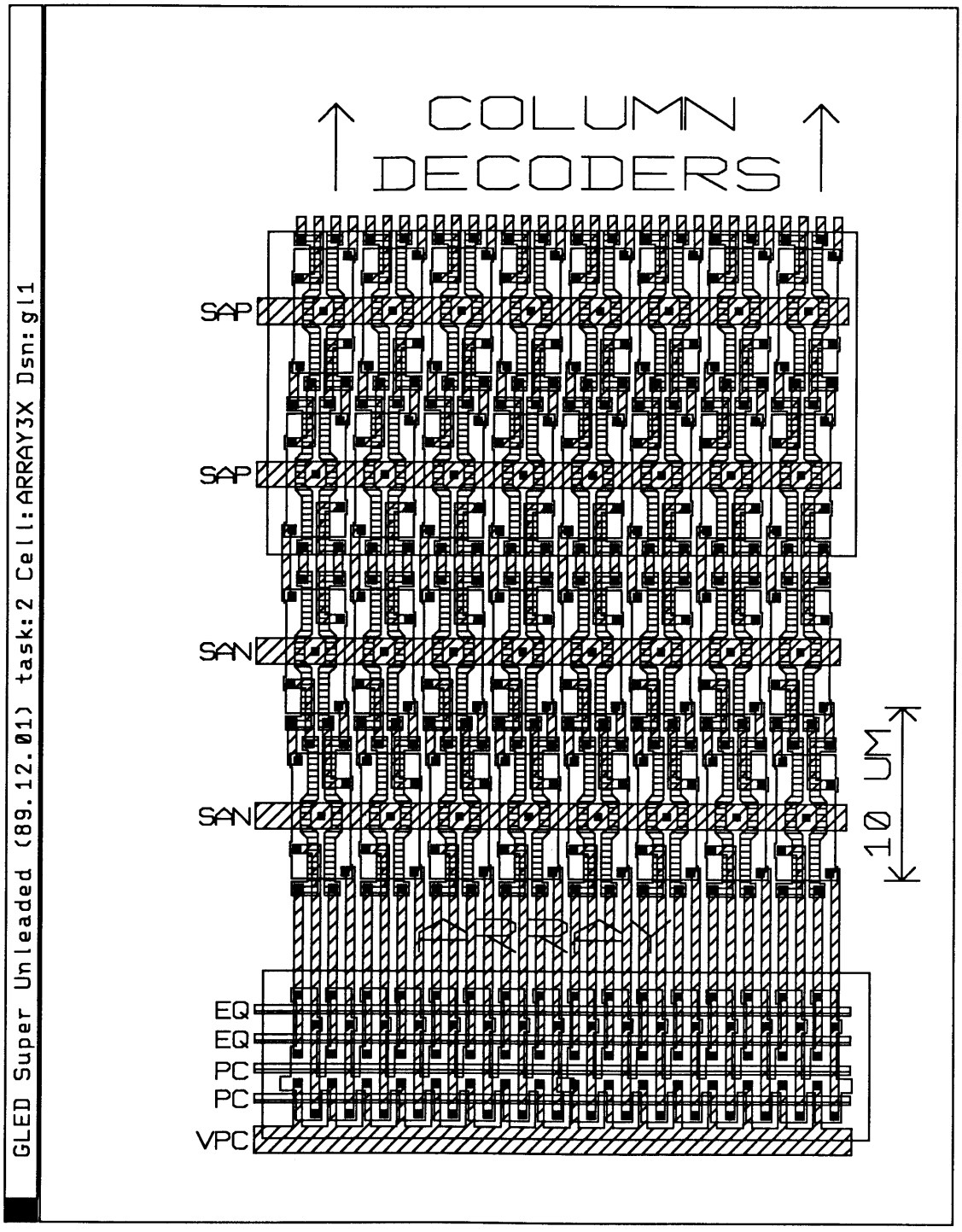

Figure B.10: 2/3 V_{DD} Sense Amplifier Layout

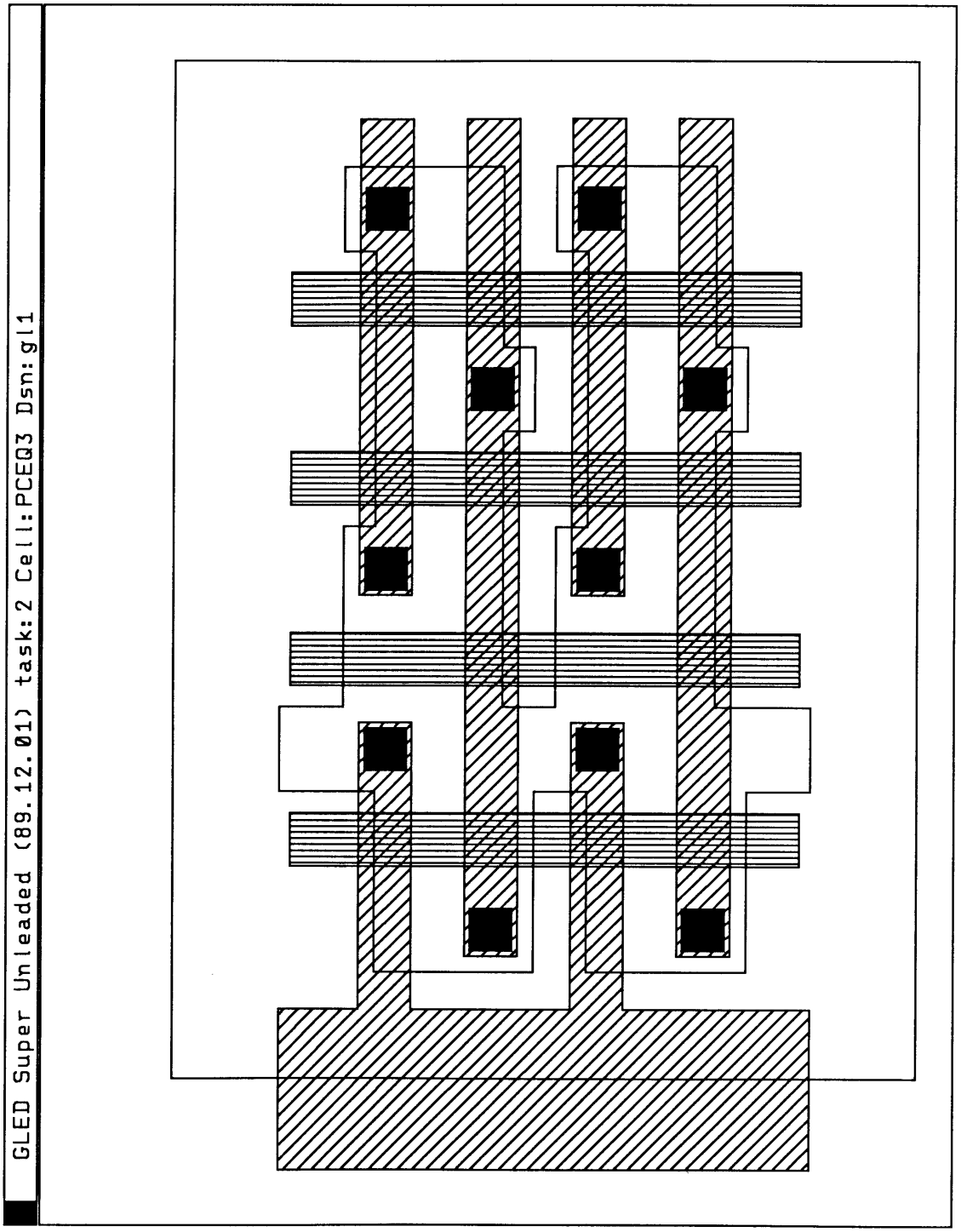

Figure B.11: 2/3 V_{DD} Sense Amplifier Precharge and Equalization Device Layout

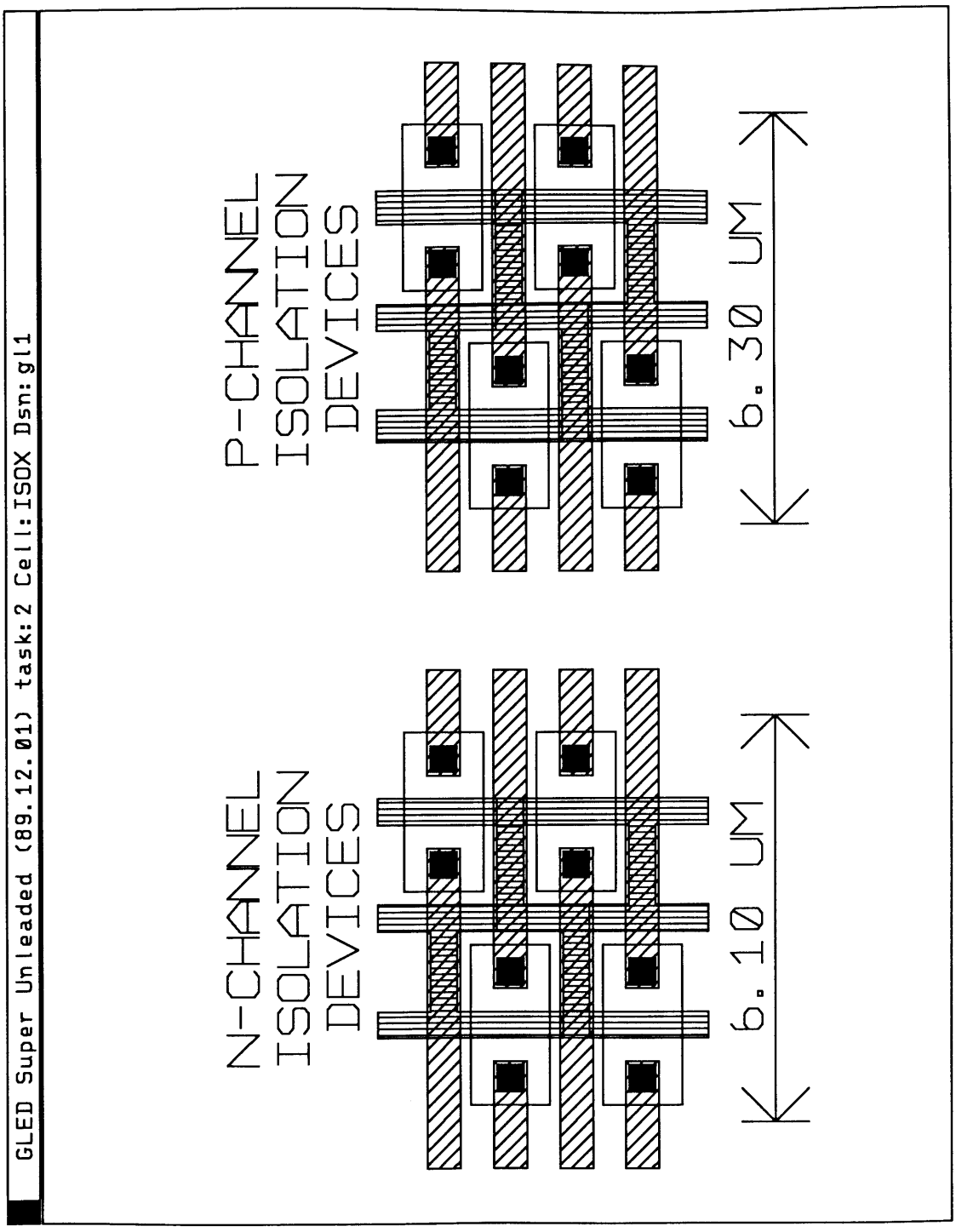

Figure B.12: Isolation Device Layout