Prospects for Wide Bandgap and Ultrawide Bandgap CMOS Devices

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***Abstract*— Power and RF electronics applications have spurred massive investment into a range of wide and ultrawide bandgap semiconductor devices which can switch large currents and voltages rapidly with low losses. However, the end systems using these devices are often limited by the parasitics of integrating and driving these chips from the silicon complementary metal–oxide-semiconductor-based design (CMOS) circuitry necessary for complex control logic. For that reason, implementation of CMOS logic directly in the wide bandgap platform has become a way for each maturing material to compete. This review examines potential CMOS monolithic and hybrid approaches in a variety of wide bandgap materials.**

***Index Terms*— AlN, complementary metal–oxide-semiconductor-based design (CMOS), diamond, GaN, SiC, wide bandgap.**

I. Introduction

THE fields of power and RF electronics, which assume ever-increasing importance in a highly connected and energy-efficient future, meet stringent specifications by demanding smaller, faster, more conductive, and higher-voltage transistors. Silicon, based on its natural abundance, massive economies of scale, and an extensive history of painstaking study and manufacturing maturity, has long been the semiconductor of choice. But while silicon power devices continue to wring every ounce of performance from the material, many applications have begun incorporating wider-bandgap semiconductors. The large voltage-handling capacity of these crystals allows them to exceed the material limits of silicon in the tradeoffs of ON-resistance, breakdown voltage, and capacitances.

But, these advances come at a cost: for the most part, the monolithic integration of control circuitry, common in silicon "smart power ICs" [1], has proven difficult in other materials. The inferiority or absence of complementary (nMOS/pMOS) processes in high-power materials has been a major barrier to their adoption [1], as systems designers must either:

1) Combine external control/driving circuitry in silicon with their wide bandgap power transistors, increasing system complexity, introducing further parasitics and reliability concerns, and often limiting overall performance [2], [3].
2) Or control the power transistors from monolithic circuit topologies limited to noncomplementary devices [4].

The preference for complementary metal–oxide-semiconductor-based design (CMOS) stems from its many advantages as a logic family, such as high input impedance, high fan-out capability, and simple driving, thanks to the gate oxide; low static power consumption and near rail-to-rail swing due to the complementary pair structure [5], [6]; and, finally, high device density and compatibility with memory devices. Even outside digital design, a variety of circuits can be enhanced or simplified by complementary devices, e.g., using active-load architectures [7], or leveraging the flexibility to switch on either high-side or low-side [8].

Axiomatically, circuit designers will find a way to work with what they have. For example, where pMOS is not available, but both enhancement- and depletion-mode nMOS devices are integrated, as in some GaN processes, direct-coupled FET logic (DCFL) has proven a popular substitute [9], [10] for CMOS, see Fig. 1. Nonetheless, a systems-level analysis of these competing logic families with highly imbalanced

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TABLE I
COMPARISON OF SILICON WITH WIDE AND ULTRAWIDE MATERIALS AT ROOM TEMPERATURE

	E_G [eV]	$\mathcal{E}_c$ [MV/cm]	μ_n [cm^2/Vs]	μ_p [cm^2/Vs]	E_{donor} [eV]	E_{acceptor} [eV]	σ_{therm} [W/mK]
Si CMOS	1.1	0.3	500	100	.05	.05	150
4H-SiC CMOS	3.3	2.5-3	25-35 *100-200	7-10 *15.6	.05	.2	400
AlGaN/GaN "GaN HEMT"	3.4	3-3.5	1500-2000	10-30	.03 or polarization	.1-.2 or polarization	200 or foreign substrate
GaN/AlN "AlN-buffer HEMT"	3.6	3-3.5+	700	>20 strain engineering?	.03 or polarization	.1-.2 or polarization	300 or foreign substrate
Diamond	5.5	10	1000-2000	2000-4000	.57	.37	2200
H-Diamond	5.5	?	N/A	50-150	N/A	N/A	2200

For Si, see [17]–[19]. For SiC, see [11], [20]–[23], where *-values indicate room for improvement by other methods [21], [22]. For III-Nitrides, see [20], [24]–[26]. The wider bandgap of GaN when strained to AlN is a k.p effect, and the critical field is expected to increase [27]. The note about strain engineering refers to [28], and polarization can be used to supply a local charge density without chemical dopants [25]. Diamond, see [11], [29], [30]. Most values in this table, regardless of format, represent broad, uncertain, or variable ranges, so the reader should draw only rough comparisons.

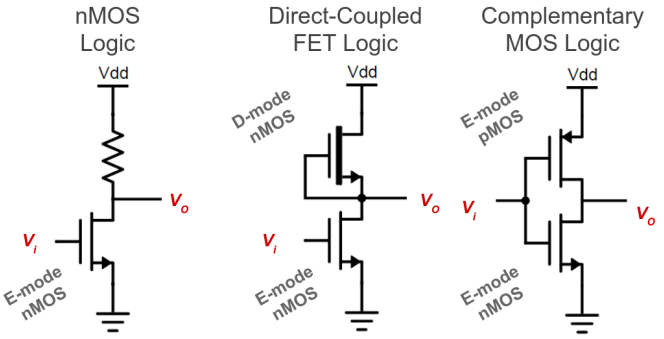

Fig. 1. Basic inverter structure in three relevant MOS logic families (nMOS, DCFL, and CMOS) indicating which transistors are required.

complements is outside the scope of this device-level review. So, although wide bandgap ICs could vary in architecture [11], this work focuses specifically on prospects for CMOS within different wide bandgap material platforms. The review should familiarize the reader with the status of monolithic and heterogeneous CMOS options ranging from wide bandgap SiC and GaN to ultrawide-bandgap diamond.

A. Device Scope

Vertical devices, that is, structures with contacts on both the top and bottom of the epitaxial layers, have dominated the high-power-density discrete market in silicon and silicon carbide [12]. In a vertical device, roughly the full semiconductor volume is available for current flow, as opposed to laterally oriented devices where, generally, current flows only near the epitaxial surface, thus "wasting" much of the volume. Even in GaN, where lateral devices are far more mature than vertical counterparts, these advantages are motivating the development of extremely high-voltage vertical devices [13]–[15].

However, for intimate integration of power devices and controls, when connection parasitics must be reduced for high operating frequencies, lateral devices are preferred (at least within the control circuitry) because of their compatibility with standard integrated circuit layout [1]. On-chip interconnects offer better reliability and performance than the combinations of wirebonds, bumps, traces, solder, etc. which would form a complete system from standalone parts. This allows operation at higher frequencies, enabling the size reduction of the large reactive elements. (Additionally, lateral GaN devices are available on silicon for scalability and economy.) Thus, lateral devices will be the focus of this work (though it should be noted this does not rule out the integration of lateral CMOS control with a vertical power element, e.g., [16]).

B. Material Scope

A quick reference of some relevant parameters at room temperature for the materials touched on here is provided in Table I. All numbers, no matter how specific, should be taken as general ranges, since material quality, measurement technique, device structure, temperature, and operating regime all play a large role in the applicability of these numbers. However, some aspects jump out immediately. SiC MOS is the most n-/p-balanced of the 3-D materials; GaN, with its high-mobility two-dimensional electron gas (2DEG), is the most n-favored, and diamond is the most p-favored, particularly with hydrogenation. The AlN buffer platform may improve the thermal performance of GaN high electron mobility transistors (HEMTs), but both GaN and SiC pale in comparison to diamond, which also tops out the critical field. These factors will come into play in the sections to follow.

II. SILICON CARBIDE

Silicon carbide will be discussed first, as it is the only wide bandgap material system where CMOS is not merely a tantalizing possibility, but already an established platform with complex digital circuit demonstrations and extreme-condition reliability studies. Other candidate materials may benefit by understanding how SiC marketed and matured in this area.

Silicon carbide LED the way as the first wide bandgap semiconductor to reach commercial maturity, and it is projected that, even as other materials catch up, many of the applications demanding the highest voltage-blocking capability will make use of SiC vertical power devices. Development of lateral SiC ICs traces to at least the mid-nineties, including early development at Cree [31] and Purdue [32]. From the start, this field has almost universally emphasized high-temperature operation [33] as the main selling point. Given the low mobilities and operating frequencies [34] characteristic of lateral SiC MOS technology, the main push has been to go where silicon cannot. High temperature silicon with derated lifetimes can operate up to 200 °C, while high temperature silicon-on-insulator (HTSOI), for instance, caps out at ~300 °C

for short-term operation, and <250 °C for longer exposure [33, Table 61.2]. This cedes an enormous operating range (of interest to the automotive, aerospace, and energy industries), accessible only to wider-gap materials. While the wide bandgap allows low-intrinsic leakage up to high temperatures, the high thermal conductivity of SiC [20] gives it an additional leg up in this front over its frequent rival, gallium nitride. In terms of raw operating temperature alone, the most impressive ICs are NASA's JFET circuits, which have demonstrated year-long operation at 500 °C [35], and operation over a 1000 °C wide range [36]. Such performance is critical for the extremes typical in space exploration, with targets such as operation on Venus. Researchers have also studied other oxide-free devices in order to enhance high-temperature reliability [37].

SiC MOS devices, however, have tougher barriers to overcome. The main obstacle has been the low inversion-channel mobility and high interface trap-density at the SiC-oxide interface, as reviewed by Cabello [21]. Among the three popular SiC polytopes (3C, 4H, 6H), 3C-SiC is known to host the highest-quality interface to SiO_2 (showing $D_{it} < 10^{11}/\text{cm}^2/\text{eV}$ and mobilities on the scale of 200 cm^2/Vs with standard dry oxidation [38]), but its lower bandgap and defective bulk epitaxial quality limit commercial adoption. As for the remaining two polytopes, 4H–SiC is preferred for power devices given its higher bulk mobility and slightly higher bandgap [23], even though 6H-SiC shows higher MOS inversion channel mobility under similar processing [39]; accordingly, CMOS has been demonstrated on both these polytopes. At present, the standard for nMOS inversion channel mobility is 25–35 cm^2/Vs, typical of 4H–SiC oxides with nitridation [21]. Techniques such as diffusion of other elements into the oxide have shown promisingly high mobilities in the 100–200 cm^2/Vs range, but concerns remain about reliability for high-temperature operation, which is precisely where SiC needs to perform. Other work has indicated the advantages of alternative crystal orientations for higher mobility on the scale of 100–200 cm^2/Vs [38], and, while these have been adopted for vertical SiC devices, e.g., [40], the implications for a lateral CMOS layout have not been detailed. Buried-channel devices, distancing the carriers from the gate, have also been explored with success [41], [42] in increasing the mobility to 100–200 cm^2/Vs range, though at the expense of significant transconductance reduction and more difficult design constraints to establish normally OFF behavior.

For the time being then, lateral SiC nMOS remains a far cry from the roughly 500 cm^2/Vs available in Si/SiO_2 interfaces and the 1500–2000 cm^2/Vs typical of GaN/AlGaN 2DEGs. A peculiar side-effect of this weakness is that it places SiC nMOS and SiC pMOS on comparable footing, where typical SiC pMOS mobilities of 7–10 cm^2/Vs [5] are only worse than nMOS by a factor of 3–4, not terribly different from long-channel CMOS. This achieves a relatively unique level of "balance" compared to other wide bandgap platforms.

Narrowing our focus specifically to monolithic CMOS, there are first a handful of early exploratory demonstrations [32], [43] which laid the groundwork on topics such as reducing the magnitude of the pMOS threshold voltage. Research continues on optimization to best match n- and p-channel devices given the different doping-dependent mobilities and dopant activation energies involved [34]. To tune appropriately low threshold voltages (e.g., for 5 V logic), precise control over low doping levels is necessary, which means extremely pure epitaxial material or further tuning with counter-dopants [44].

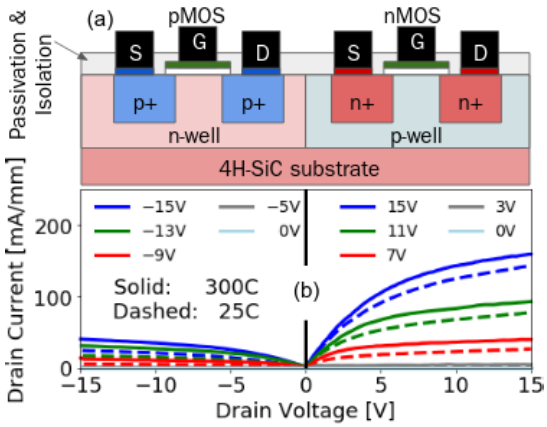

Fig. 2. (a) Technology cross section of Raytheon's HiTSiC process as in [45]. Note that details may vary, e.g., Weng *et al.* [45] and Murphree *et al.* [46] describe body contacts and the substrate differently. (b) *I–V* characteristics of a 1.2-μm pMOS and nMOS at 25 °C and 300 °C (data [46] renormalized to device width).

The state of the art is set by Raytheon U.K. with their 1.2-μm HiTSiC process, which, at some generations, employs two separately doped n- and p-wells on n+ 4H-SiC epi, see Fig. 2, to target operation at 15 V levels in 300 °C-and-up environments [45]. Devices with 2-μm gate lengths for analog operation have been published showing nMOS (pMOS) ON-currents in the 60 mA/mm (20 mA/mm) scale over a range from 100 °C to 400 °C. Devices with 1.2-μm gate lengths for digital operation show nMOS (pMOS) ON-currents on the scale of 150 mA/mm (40 mA/mm) at 300 °C [46], see Fig. 2(b). Threshold voltages are set large at room temperature (e.g., n: 4.65 V, p: −6.04 V in [47]) to allow margin for significant decrease at high temperature. Much of that shift occurs from 25 °C to 100 °C; once above 100 °C, both nMOS and pMOS stay within 1.5 V of their eventual 400 °C values of ±2 V [47]. Modeling the large temperature dependence of the thresholds should account for not only the intrinsic MOSFET physics [19], but also the temperature-dependent interface trap distributions [48]. Using this technology, researchers have demonstrated numerous circuit designs, including timers [47], multiplexers [47], hybrid power module controllers [45], and other complex digital circuits [49], [50] operating at 300 °C and above, including the first digital analog converter (DAC) operational at 400 °C [51]. While less information is available in the public literature about other players, Raytheon is not the only corporation to invest in SiC CMOS. Hitachi, for instance, has emphasized developing a radiation-hard technology for nuclear plant applications—especially in the wake of the Fukushima disaster—and has demonstrated the irradiation performance of an op-amp [52], [53] and a trans-impedance amplifier [54]. While the mobilities (n: 5 cm^2/Vs, p: 3 cm^2/Vs [54]) are substandard, the radiation survivability is a strong selling point.

Many challenges remain to be solved, the first being the poor oxide interface discussed above. Other difficulties stem from the fact that the main p-dopant, aluminum, is a relatively deep acceptor, so source/drain regions are highly resistive at room temperature. On this point, Albrecht *et al.* [44] explained that the source–drain resistances are critical enough to alter the designed n/p width ratios. (This problem lessens at high temperature due to increasing aluminum acceptor activation, but the trend that p-source/drain resistances are an order worse than n-source/drain resistances holds at room [45] and high-temperature [47]). The dopants also introduce further process challenges: the anneal after ion implantation requires temperatures of roughly ∼1700 °C. With that thermal budget, the contacts must be implanted and annealed *prior* to gate formation, which eliminates the simplicity of traditional (gate-first) self-aligned gates. On that front, other researchers have suggested epitaxial contact doping combined with recesses, which eases the thermal budget significantly [5]; further work is required to establish whether these devices can reach similar performance. Meanwhile, other design challenges, such as movement of threshold voltage with temperature, may have to be compensated in circuit design. Nonetheless, the low intrinsic carrier concentration, high thermal-conductivity, and high breakdown of SiC have found a home in the world of extreme-environment, point-of-operation control. As the first wide bandgap system to achieve nontrivial CMOS circuits, and to demonstrate operation in application-relevant stressful environments, SiC is a fine role model for other budding wide bandgap CMOS contenders.

III. Gallium Nitride

Unlike SiC, there is no production GaN CMOS at present. Therefore, it makes sense to first discuss each complement separately, starting with the n-channel. GaN HEMTs, having demonstrated their mettle in the RF market, are steadily breaking into the power market with numerous companies offering production devices [55]. HEMTs are based on the AlGaN/GaN heterostructure, which, due to a polarization difference and band offset, is able to confine a 2DEG channel at the high-quality epitaxial interface, rather than a semiconductor-oxide interface. This distinguishes the device in two ways from a classic MOSFET.

1) Typical gate stacks feature metal directly on the epi surface, with the wider-gap AlGaN serving as a barrier (although depletion-mode insulated-gate GaN "MOSFETs/MOSHFETs" are also commercialized [56]).
2) The baseline device is depletion-mode given the large positive polarization charge present. Nonetheless, various techniques such as gate recesses [57], [58], fluorine implantation [59], [60], castellation/tri-gates [61]–[63], and most popularly p-(Al)GaN gates [15], [64] have demonstrated enhancement mode operation [65], with the latter commercialized [15], [66]. Enhancement-mode devices targeting power applications offer output currents in the hundreds of mA/mm range with breakdowns in the hundreds of volts [58], [60], [64], [67]. Despite the variation between different approaches for most of these research-level devices, they distinctly outperform the lateral SiC nMOS devices above, and given the amount of review work in this area [15], [55], [65], the potential for this n-channel technology needs no further elucidation.

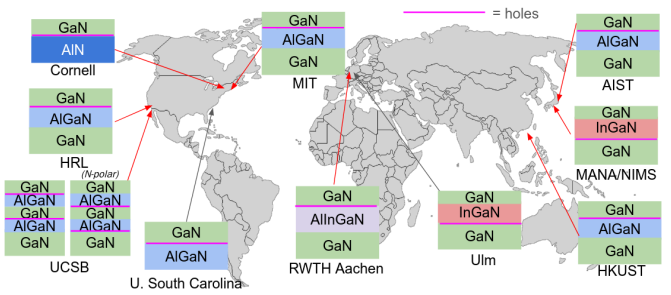

Fig. 3. III-nitride heterostructures which induce a 2DHG. Purely p-GaN approaches (e.g., [71]) are not included.

On the p-channel side, the choice of heterostructure materials is itself still wide open. The difficulties include 1) deep-energy acceptors (magnesium at a level of 100–200 meV [68]); 2) difficult ohmic contacts due to the deep valence bands [69]; and 3) low-mobility/high-mass holes [70]. Researchers have partially circumvented that first challenge, doping, by using the material polarization instead to induce a hole gas: just as a metal-polar AlGaN-on-GaN interface provides a positive fixed sheet charge, a flipped GaN-on-AlGaN (still metal-polar) interface provides a negative fixed sheet charge. Since the sheet charge has the periodicity of the lattice, it attracts holes without scattering them. And since the polarization charge has no Fermi-level dependence, it does not screen the gate fields, thus avoiding the unsavory electrostatics [71] of deep acceptors. Researched heterojunctions that should induce a 2D hole gas (2DHG) include (metal-polar) GaN/AlN, GaN/AlGaN, InGaN/GaN, and (nitrogen-polar) AlGaN/GaN. Fig. 3 indicates the variety studied. Many of these structures, depending on the details of doping and thicknesses, may also host electron gases, and most that do not, with the notable exception of GaN/AlN, seem to (in practice) require some (potentially moderate) amount of doping in order to manifest the hole gas [25].

The second challenge for these structures is ohmic contacts. While many of the works do not report contacts directly, Schottky nature is often evident in the output characteristics. Among the best thus far, contacts on the order of a few $\Omega \cdot$ mm can be achieved by heavily doped InGaN layers atop the high density ($4–5\times10^{13}$/cm^2) hole gases of GaN/AlN [72]. Presently incorporating less than 10% of Indium, this p-contact technique could be pushed further, as explored in the context of LEDs [73]. However, to differentiate structures for contact, access, and/or gate regions is still a thorny process given the difficulty of ion implantation in GaN. Whereas n-type regrowth is highly developed for HEMT ohmic contacts [74], p-type regrowth arguably has the added constraint of needing to preserve or recreate the delicate hole gas, at the risk of *reducing* the local conductivity. And whereas gate recesses are a studied technique in HEMTs, the requirements for the etch are even more stringent in p-channel devices

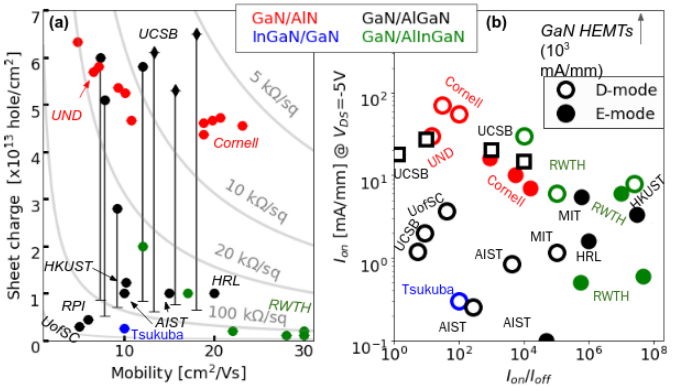

Fig. 4. (a) Mobilities and densities reported for a variety of 2DHG-hosting III-nitride heterojunctions [3], [25], [77]–[90]. For fair inclusion of superlattice structures, vertical lines indicate both the total hole charge (top) and the normalized charge-per-period (bottom). Circles are metal-polar structures, diamonds are nitrogen-polar. (b) ON-current (at fixed 5 V drain) and ON–OFF ratio for of III-nitride p-channel platforms [3], [72], [77]–[81], [83], [85], [86], [88], [89], [91]–[95]. Solid shapes are enhancement-mode, hollow are depletion-mode, and squares represent (width-normalized) tri-gate devices. Devices with ON-currents below. 1 mA/mm are not shown.

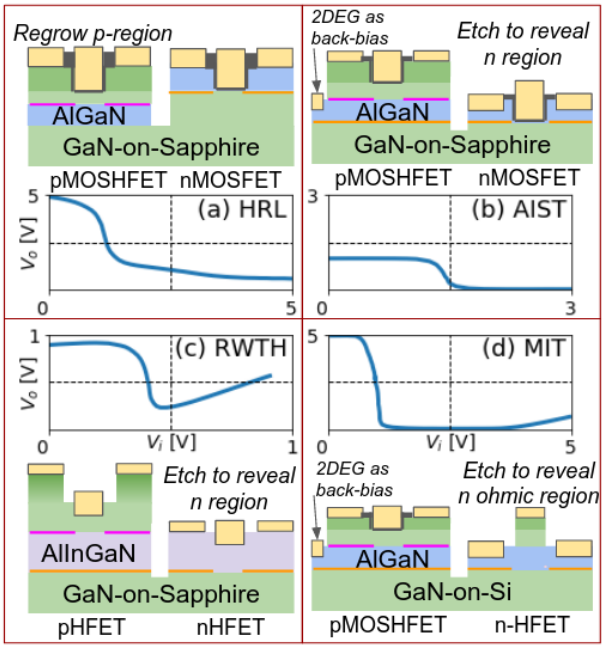

Fig. 5. Inverter dc characteristics from four groups. (a) HRL [3] employed regrowth to separately tune the p-channel epi, while (b) AIST [93] and (c) RWTH [99] used epi with both a 2DEG and a 2DHG then etched the 2DHG away for recessed *E*-mode devices, and (d) MIT [95], [100] designed the epi so the p-layer can serve as an *E*-mode p-GaN gate for the n-channel device.

since plasma etching induces nitrogen-vacancy (*donor*-like) defects [75]. Refinement of etching processes or, depending on the structure, use of combined sublimation [76] and regrowth techniques may prove critical in forming differentiated regions for low-resistance contacts and high-control gates.

The third limitation, mobility, is fundamental to the crystal [70]. Various reports on different heterostructures have yielded different 2DHG densities (dependent on the polarization charge) and mobilities, as shown in Fig. 4(a), with the lattice-matched GaN/AlInGaN structures currently holding the mobility record, and the GaN/AlN interface hosting the most charge (per a single junction), at a reasonable mobility. The mobilities evidenced on the scale of 10–30 cm^2/Vs agree nicely with theoretical predictions of the intrinsic phonon-limited hole mobility around 34 cm^2/Vs computed for a GaN/AlN 2DHG [28] and 50 cm^2/Vs for bulk [70]. The source of the low mobility is the band-edge availability of the heavy hole (HH) band (with its high effective mass, i.e., high density of states (DOS) for both heavy and light holes (LHs) to scatter into). However, it may be possible to improve the situation to some extent by strain engineering, either with biaxial tension [70] to raise the split-off band or in-plane uniaxial strain to break the heavy/light-hole degeneracy [28], [96], [97], with idealized effects estimated to boost mobility to 60–120 cm^2/Vs. There is some exciting albeit limited experimental support for the latter approach [98].

Despite these challenges, significant progress has been made in recent years. P-channel ON-currents have been reported up to the 100 mA/mm range for both the GaN/AlN HFETs (ON-resistance near ~70 Ω·mm) [72] and the GaN/AlGaN fin-HFETs [79]. Modulation ratios up to 10^8 have been evidenced for the lattice matched GaN/AlInGaN devices. A variety of enhancement and depletion mode devices are compared in Fig. 4(b), where it seen that the highest ON-current levels are so far provided by the GaN/AlN approach, and the cleanest device quality from the quarternary approach. Multiple institutes have demonstrated monolithic CMOS inverter operation; four such integrations are described in Fig. 5. A cursory examination of the inverter characteristics reveals there is much further to go. In addition to the obvious matching constraints, integrating two devices with different process requirements can damage one or the other [99], resulting in significant leakage or and/or heightened resistance which prevents rail-to-rail switching. Etch-based tuning of one (or both) separate threshold voltages can be either imprecise or insufficiently enhancement-mode, also preventing the achievement of centered rail-to-rail characteristics. Incorporation and refinement of more precise atomic-layer etching, use of additional threshold tuning mechanisms [93], and continued development of lower resistance p-channel devices will go a long way toward improving these inverters.

Given the interest in ultrawide bandgap electronics specifically, it is worth highlighting the role that AlN could play in a III-nitride CMOS setting. As discussed above, the GaN/AlN interface is a highly promising candidate for a p-channel device wherein the massive polarization difference results in an enormous degenerate hole gas (Fermi level nearly 50 meV into the valence subband at wavevectors of ~1.5 nm^{-1}). This gives high contactability with tight scalable confinement for suppression of short-channel effects, with the AlN buffer also providing a high thermal conductivity path for heat extraction. An n-type complement based on the AlN platform is also under study: the AlN/GaN/AlN heterostructure with a thin GaN channel ("Quantum Well HEMT" or "AlN Buffer HEMT") [101], [102]. The bandgap of AlN provides a large, thin barrier, and since the buffer is also AlN, the barrier is

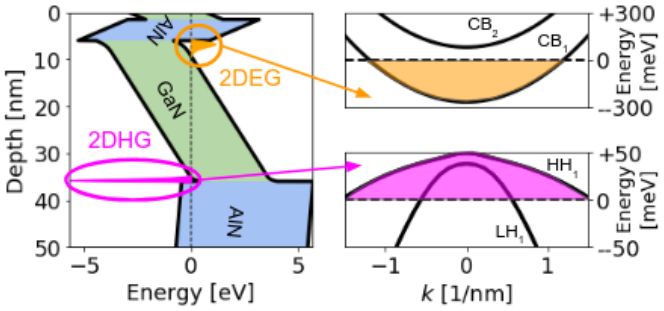

Fig. 6. Band diagram of a QWHEMT (AlN/GaN/AlN + GaN cap), showing the 2DEG and 2DHG separated across a high-field GaN well. Insets show the 2DEG occupying the first subband (CB_1), and the 2DHG occupying the first subbands of the HH and LH bands.

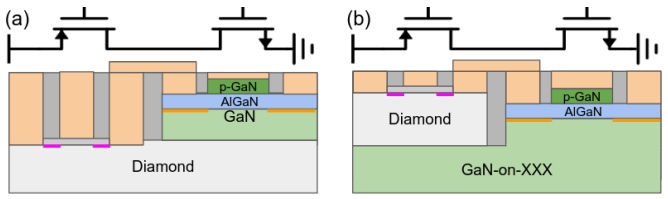

Fig. 7. Diamond p-channel devices and GaN n-channel HEMTs could conceivably be integrated by either (a) bonding GaN onto a diamond template as in [121] or (b) growing diamond on a GaN HEMT template [128].

under far less strain [103]. The backbarrier provides a high-thermal-conductivity, electrically-insulating support, as well as tight confinement from the large polarization fields and, with a thin channel, a boost to the breakdown field [27]. These effects have been combined to demonstrate high-breakdown AlN HEMTs with short gate lengths for high-frequency performance [26]. Despite the present lower mobility of these structures (~700 cm^2/Vs, [104], [105]) versus established GaN HEMTs, the performance has been impressive and development continues. Interestingly, like the GaN/AlGaN/GaN heterostructures above, these AlN/GaN/AlN structures host both a 2DEG and a 2DHG, and both have been demonstrated to be active [106], [107], with the barrier between them formed by a polarization Stark effect rather than a band-offset, as illustrated in Fig. 6. Studies to integrate n- and p-channel devices are underway, and the proximity of high-density electron and hole gases could enable other interesting device concepts, e.g., in lighting, which could coexist in a complementary electronics platform.

As compared to lateral SiC CMOS, GaN CMOS is clearly the more immature, but may have certain advantages. Since the channels can reside at an epitaxial interface rather than a dielectric interface, higher mobilities are possible; GaN HEMTs solidly outperform SiC lateral nMOS, and GaN p-channel devices are comparable to SiC lateral pMOS (but with a great deal more margin for improvement). SiC's thermal conductivity advantage [20] over GaN will preference it toward the higher temperature applications, though this margin could be diminished substantially by employing higher-thermal conductivity AlN as the buffer (i.e., in the GaN/AlN heterostructure). What application range would benefit from Schottky-gated versus MOS-gated GaN structures (since both are a possibility in Fig. 5) remains to be seen as the improved robustness of dielectric-free designs will trade against increased leakage particularly at high temperatures [90]. Overall, it is possible that SiC and GaN CMOS could divide the market (in frequency versus power requirements) as SiC and GaN n-channel devices have already done.

IV. Diamond

Diamond, as an ultrawide bandgap material, further scales the GaN/SiC potential for high-temperature and high-power operation, but makes an unusual entry into this list as its difficulties are somewhat complementary. In diamond, while p-type doping is natural (albeit inefficient with boron at an acceptor level of 0.37 eV) it is n-type doping that has proven difficult [29], [108] with phosphorous a deep donor at 0.57 eV. Though there have been recent advances via methods such as boron-oxygen complexes [109], n-type performance is yet to be fully assessed. Meanwhile, p-type transistors in many forms are a well-demonstrated research-level technology [29].

Two ways of inducing holes should be distinguished.

1) Conventional doping can produce high-mobility carriers (in the thousands of cm^2/Vs) of both signs at low doping levels. However, producing large concentrations requires enormous doping densities, so ohmic contacts are challenging, whether contacting direct epi [110] or providing regrowth [111], and temperature sensitivity with a high-activation-energy dopant is drastic. However, this approach can maintain channels nearer to the large bulk hole mobility of diamond, and breakdown (without field-shaping) has been shown at effective averaged fields of 4 MV/cm [110], already well beyond typical results of GaN/SiC.
2) Alternatively, hydrogenating the diamond surface produces a 2DHG at high density ~ $10^{13}/cm^2$, albeit lower mobility of ~50–150 cm^2/Vs [30], which can be stabilized to roughly 500 °C by dielectric passivation [30], [112] and contacted by TiC annealed metallization [113]. This combination of mobility, temperature range, and high breakdown field promises diamond an eventual niche in high-power switching. Hydrogenated diamond has already demonstrated medium [114] and high-voltage devices with averaged fields exceeding 1–2 MV/cm [112], [115], [116] and lower voltage devices exceeding 3 MV/cm [115]. Toward integration, DCFL logic gates have been demonstrated [117]. Continued design exploration, e.g., fins in both the volumetric [111] and hydrogenation [118] approaches, should keep pushing the envelope.

However, given the dearth of diamond n-channel devices and the present limitations of diamond substrates [119], diamond may wish to join forces with a system like GaN [112], where mature high-performance n-channel devices are yet to mate with high-voltage p-channel devices, as in Fig. 7. Thanks to the high-power output of GaN devices, researchers, and corporations such as TriQuint/Qorvo and Mitsubishi have long tried to bring a high-thermal-conductivity insulator like

diamond into proximity with the GaN transistor, whether by growing GaN on diamond [120], bonding GaN films to diamond [121], [122], growing diamond on the backside of a GaN film [123]–[125], or depositing nanocrystalline diamond on partially processed GaN structures [126]. P-type diamond can also provide electrostatic design advantages to GaN HEMTs [127]. Taking one step closer to CMOS integration, EPFL [128] has recently demonstrated p-channel devices grown on GaN-on-Si templates with 60 mA/mm ON-currents and nine orders of on–off modulation. While the ON-resistance is higher than the best of state-of-art p-type GaN HFETs (mostly due to the low-mobility of the holes 1.3 cm^2/Vs on the rough diamond-on-GaN surface), the 400-V breakdown and high gate control in this first attempt demonstrate a promising potential technology to unite the best of these wide bandgap materials.

V. Brief: 2-D Materials

While most presently studied 2-D materials have low bandgaps compared to GaN/SiC, many transition-metal dichalcogenides (TMDs) at least have larger gaps than silicon, in the range 1.2–2 eV (with correspondingly higher critical fields versus silicon [129]) and high mobilities in the hundreds of cm^2/Vs at room temperature [130]. In many cases, the more symmetric band structures [131] of TMDs could allow for better n-/p-matching, and the flexibility of Van der Waals stacking [132] could allow for a great deal of mix-and-match.

MoS_2 is a popular choice for n-channel FETs due to the background of chalcogen atom vacancies [133], [134] which tend to pin the Fermi-level near the conduction band; conversely, WSe_2 is widely used for p-channel FETs since it has a larger chalcogen vacancy formation energy [135] and a shallower valence band edge amenable to p-type contacts [136]. Black phosphorus (BP) is another popular choice for n- and p-channel FETs offering a wide range of tunable bandgaps from 0.3 to 2.0 eV and large mobility of few hundreds of cm^2/Vs at room temperature [130]. Complementary demonstrations so far have focused on these well-studied 2-D materials, either single-material [137]–[141], or multimaterial pairs [142]–[144].

While the above studies are valuable proofs to establish how 2-D devices can be integrated and what sort of approaches can be useful to mitigate their difficulties [145]–[148], the focus thus far on relatively narrow-gap materials puts most of this field outside the purview of this text. Nonetheless, they lay the groundwork for the further development of wider-gap options such hexagonal boron nitride (hBN). This crystal has an ultrawide bandgap of 6 eV [149], [150] which suggests it may become a powerful candidate for high voltage electronics as challenges in scalable growth [151], doping, and processing are improved upon. Already hBN has served a supporting role as a dielectric environment for sensitive 2-D FETs [152]. Since development in 2-D electronics is sure to continue regardless (spurred more by scaling considerations than power electronics), it is worth keeping an eye on this field for wider-gap discoveries, cointegration demonstrations, or other advances which can be adapted to the 3-D systems mentioned here.

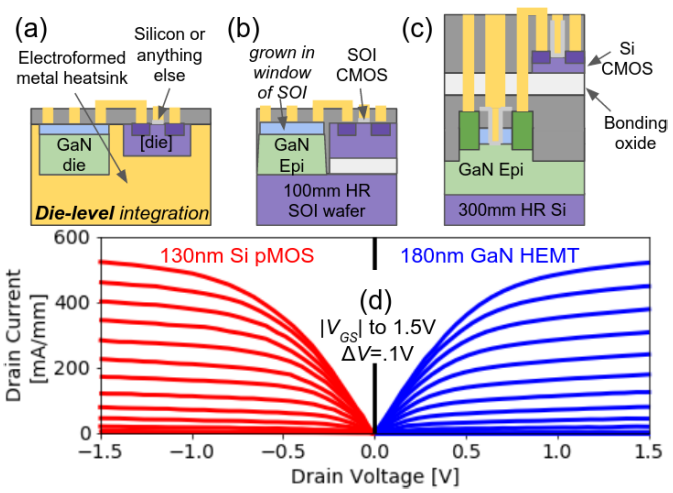

Fig. 8. (a) "MECA" integration from HRL Laboratories [153]. (b) MBE-growth-in-windows integration from Raytheon [157]. (c) Heterogeneous stacking from Intel Corporation [158]. (d) Output characteristics of a complementary pair from Intel's approach, replotted from [158].

VI. Si Heterogeneous Integrations

While a fully wide or ultrawide bandgap CMOS is tantalizing, it may in the near future be more cost-effective to produce tightly integrated CMOS employing one high-performance material and another manufacturable complement. Silicon CMOS is the most advanced, dense, proven semiconductor technology in existence, and, while it may not have the exciting material properties of all these other systems, it could fill in many of their flaws. So before this work completes, it is worth touching on the progress in bringing together wide bandgaps with intimate silicon control. Some researchers have focused on integration at the die level, such as HRL Laboratories' Metal-Embedded Chip Assembly (MECA) scheme [153], which electroforms a heatsink around multiple adjacent dies such that they can be integrated via optically defined interconnects, see Fig. 8(a), with neighboring dies about a 100 μm apart. Nonetheless, in keeping with the theme of this review (prioritizing density of integration) this section will focus on device-level approaches by highlighting examples from Raytheon and Intel Corporation integrating GaN with Silicon. (Other die- or device-level works include epitaxial lift-off [154], mold compounds [155], or bonding hybrid silicon orientations [156].)

Raytheon [157] demonstrated numerous cointegrations of III–V materials, MEMS, and more with silicon by a variety of means. In their GaN method, depicted in Fig. 8(b), the GaN epi is grown in windows on an etched high-resistivity-handler silicon-on-insulator (SOI) wafer. Silicon processing is completed first in a CMOS fab, then the growth to a coplanar height is performed by molecular beam epitaxy (MBE) at a compatible thermal budget, and finally GaN processing and interconnects are performed in a III–V facility. Results are claimed to be similar to GaN-on-SiC devices.

Recently, Intel [158] demonstrated a 3-D heterogeneous stacking in which GaN devices are produced on a 300-mm high-resistivity Si (111) wafer. The GaN-on-Si (111) wafer is then oxide fusion-bonded to a Si (100) wafer with an etch

stop layer that is thinned to 50 nm. Then CMOS processing of the top Si surface continues, all in a CMOS fab, as shown in Fig. 8(c). Altogether, this enables cointegration of high performance *E*-mode GaN MOSHEMTs and Si pMOS with matched characteristics, as shown in Fig. 8(d), and extreme potential density.

The abovementioned approaches provide a valuable compromise which allows each material to accomplish what it is best suited for, and, while they do not achieve every single directive an all-wide bandgap system could (such as extreme environment hardness), they are sure to be part of near-term integrations and long-term hybrid systems, even as the all-wide bandgap approaches mature.

VII. Conclusion

This review has taken a broad snapshot of the state of CMOS-style logic on platforms from wide-gap (GaN, SiC) to ultrawide-gap (hBN, diamond, AlN), and means of merging these with silicon and each other. The maturity of the SiC platform, despite its device limitations, suggests a well-motivated path forward for other systems. GaN, perhaps aided by AlN buffers, is its most likely competitor down the road, with either advances in p-channel fabrication or the augmentation of diamond p-channels as potential enablers. For systems where high-temperature is less critical but frequency matters, the tighter integration of silicon with GaN is a highly promising compromise. Other logic modes are possible, and other hybrid designs are plausible, but this is where the battle lines are drawn in 2020; only the upcoming decade can answer which platforms and alliances will take each corner of application space.

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