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Title:	A new construction adder based on Chinese abacus algorithm.
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Abstract: Abstract: A new construction adder based on Chinese abacus algorithm is presented in this paper. There are two kinds of beads used in this construction. Each column element has three higher beads with a weight of four and three lower beads with a weight of one. The proposed 32-bit adder contains eight column elements. The construction was simulated by the technology of TSMC 0.18μm CMOS process. Layout was also made by the same technology. The maximum delay of the 32-bit abacus adder is 0.91ns and 14% less than that of Carry Look-ahead Adders for 0.18μm technology. The power consumption of the abacus adder is 3.1mW and 28% less than that of Carry Look-ahead Adders for 0.18μm technology. Recent researches are compared with the proposed adder. The construction was also simulated by Predictive Technology Model. The PTM results also presented. The use of Chinese abacus approach offers a competitive technique with respect to other adders. [Copyright &y& Elsevier]

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