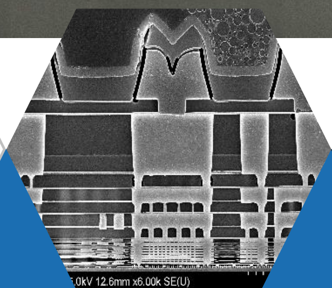

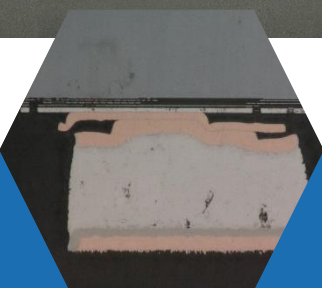

Advanced System-in-Package Technol

in the Apple AirPods Pro

Packaging report by Belinda DUBE
Laboratory Analysis by Youssef EL GMILI
March 2020 – SAMPLE

SAMPLE

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This full reverse costing study has been conducted to provide insight on technology data, manufacturing cost and selling price of the AirPods Pro SiP Audio System. The full system includes two SiP modules and 2 MEMS modules.

System-in-Package (SiP) market attained a huge revenue of $13.4 billion in 2019 and is expected to achieve approximately $18.8 billion is 2025. The market is mainly driven by increased need for advanced architectures in electronic devices mostly in mobile and consumer products. Advanced technology asks for higher levels of die and functionality integration in a single package at lower cost. Since 2015, Apple has integrated several generations of SiP in its Smartwatch. This year, for the first time, the company has chosen the same type of solution for its earbuds. This came in two different SiP, one for the Bluetooth connectivity and one for the audio codec.

Apple's AirPods adopt SiP for the first time in the latest AirPods Pro. The SiP influences device compactness and size reduction of the wireless headsets. The AirPods Pro designed and manufactured by Apple comprises of several SiPs assembled together: Two Inertial Measurement units (IMU), one Bluetooth Module and one Audio Codec Module. The IMUs are standard LGA SiPs from STMicroelectronics.

The Bluetooth Module called H1-Module is packaged using double side Molding technology in order to integrate a memory under the System-on-Chip (SoC). This structure enables wireless connection, drives voice enabled Siri and enforces real time noise cancellation. The Audio Codec integrated up to 8 dies and 80 passives components with a density of 0.96 components per mm².

The module has a special shape that is designed to be mechanically constraint in the earbuds to maximize the lost area in the system. Both SiP are designed in order to has better power management, higher performances with a high cost effectiveness.

The report includes all the packaging details from the substrate to the dies from both SiP modules. The report focuses on the packaging processes of the two SiP modules and the final assembly. High Resolution Images of the Package Cross Section at different positions and angles enables a full package and assembly process analysis. It also includes a full description of the process and the manufacturing cost of the dies and the packaging. Finally, a physical comparison of the two SiP Modules is included.

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The reverse costing analysis is conducted in 3 phases:

Teardown analysis
- Package is analyzed and measured,
- The dies are extracted in order to get overall data: dimensions, main blocks, pad number and pin out, die marking,
- Setup of the manufacturing process.

Costing analysis
- Setup of the manufacturing environment,
- Cost simulation of the process steps.

Selling price analysis
- Supply chain analysis,
- Analysis of the selling price.

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Apple AirPods Pro Earbuds

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Apple AirPods and Audio Module
©Apple

Microphone
External noise d[blurred] .

Microphone
An inward microphone [blurred] inside the ear.

AirPods Pro Right Earbud– View
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AirPods Pro TearDown

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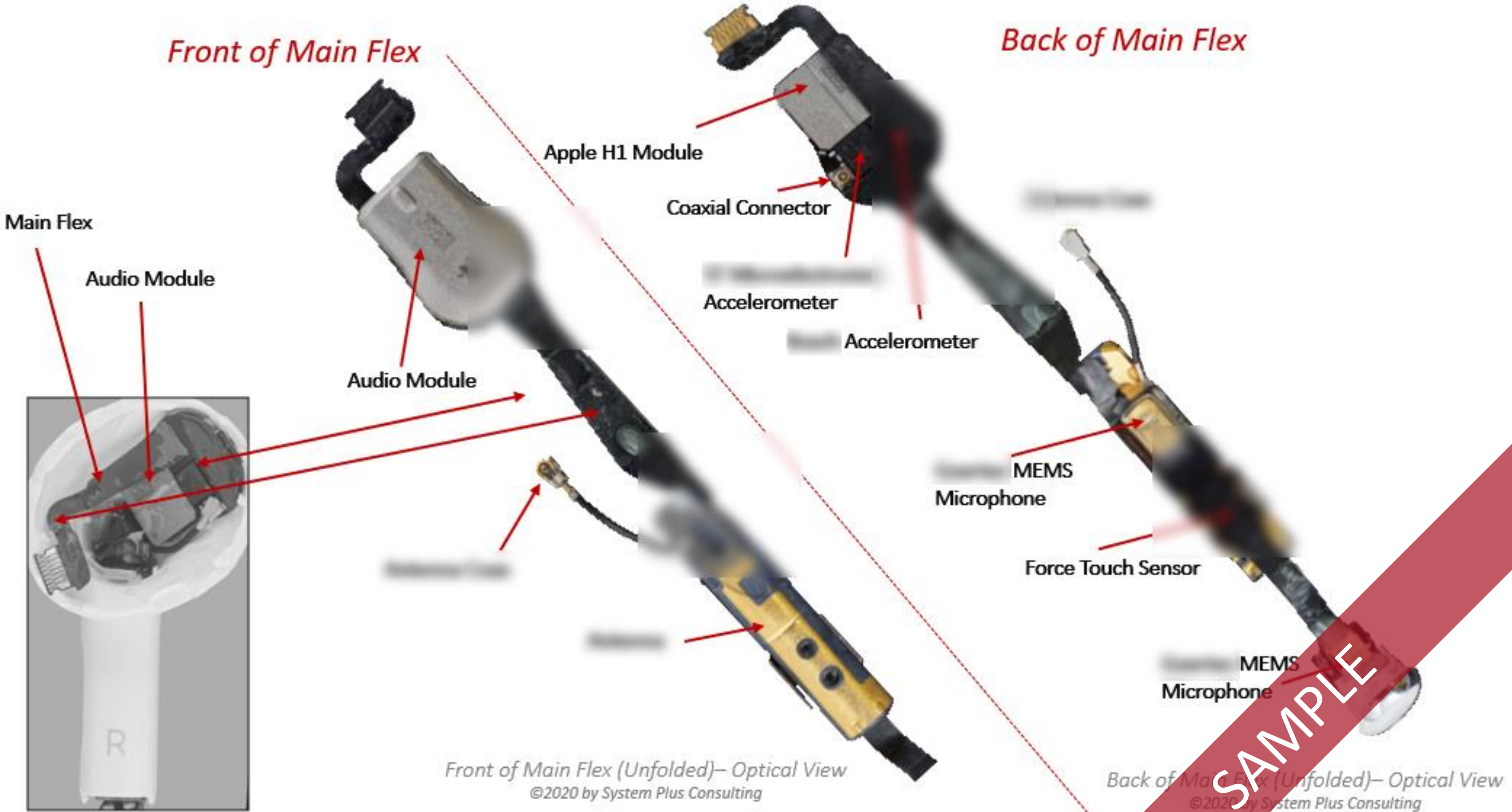

AirPods Pro Earphone TearDown
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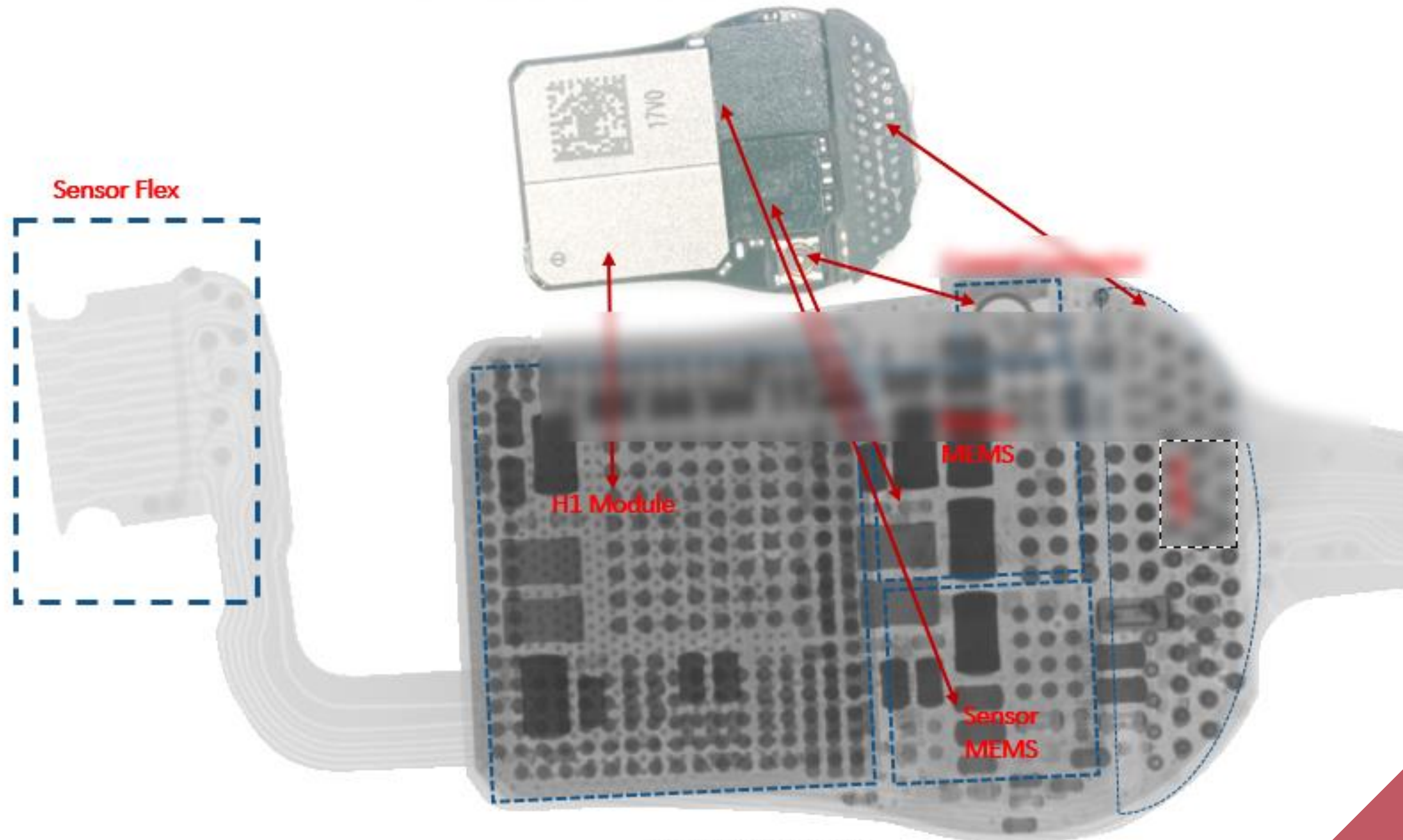
Module X-Ray View

- X-Ray images reveal the integrated in the Module.
- The dies occupy approximately % of the Top Module package surface area.
- The X-Ray image reveals the integrated in the Module.



Module X-Ray View
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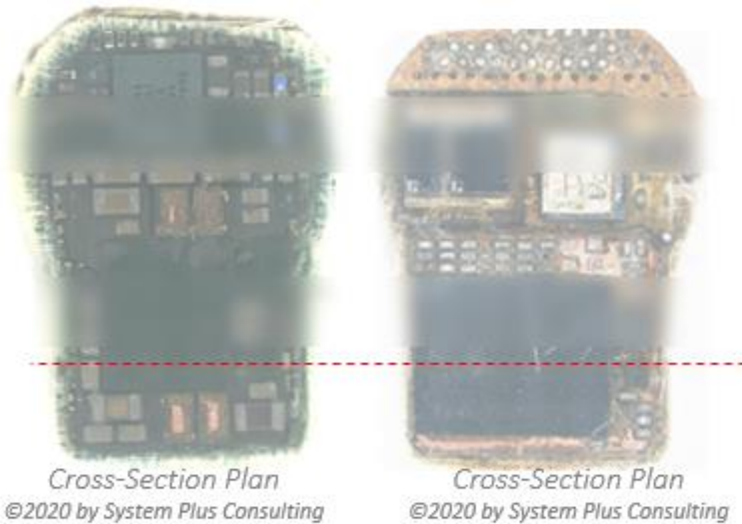
Module Cross-Section



Cross-Section Plan
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Cross-Section Plan
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- Cross-section of the package reveals the die placement on the Top Module PCB and the Bottom Module PCB.
- The Top Module PCB is attached to the Bottom Module/H1 Module PCB using
- Package Conformal shielding structure is also revealed covering the whole Top module and the Bottom H1 Module.
- from the back side of the module are revealed.
- die is placed between the Top Module PCB and Bottom Module PCB.

Solder balls
Package Moudling
MFS: Die 2
MFS:
Die X
BFS:
Die 1
MBS: Capacitor
Top Module
Bottom Module

Module Cross-Section – Optical View
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Top Module Audio Code – Cross-Section

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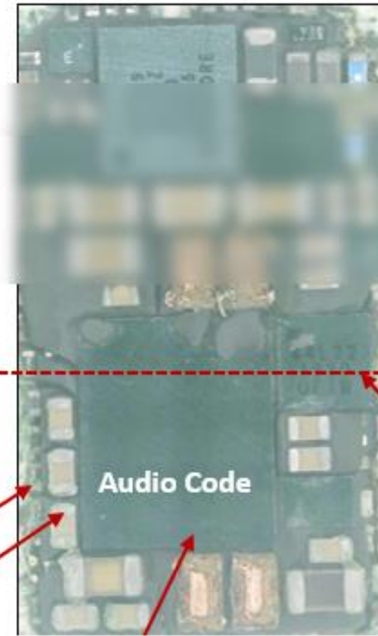

Module Front Side Cross-Sectioning

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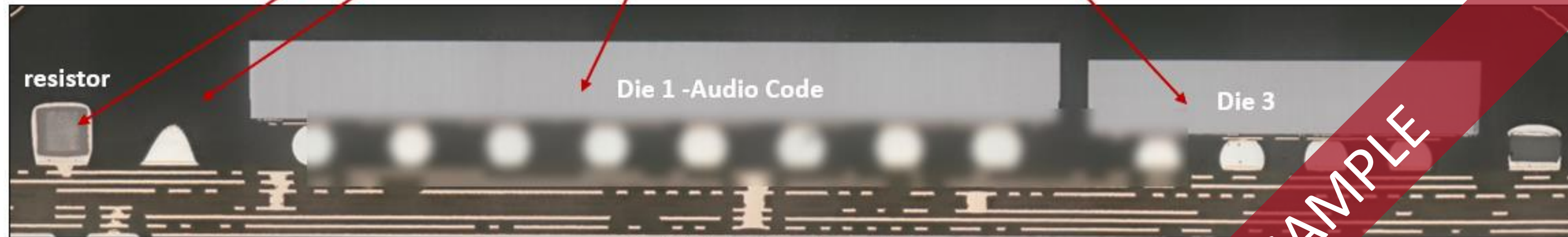

Top Module- Cross-Sectioning

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- The package Cross-Section reveals the and on PCBs.
- Die 1 Audio Code is placed on that allow .

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Top Module Operation Amplifier - Cross-Section

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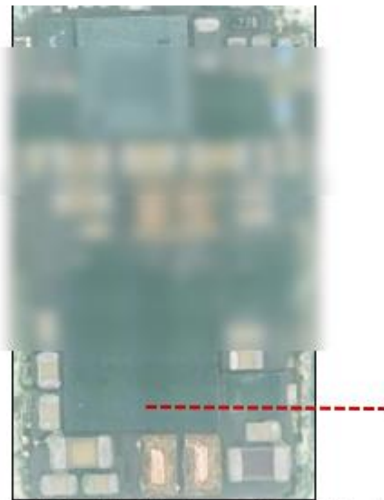

Audio Module Package Cross-Section

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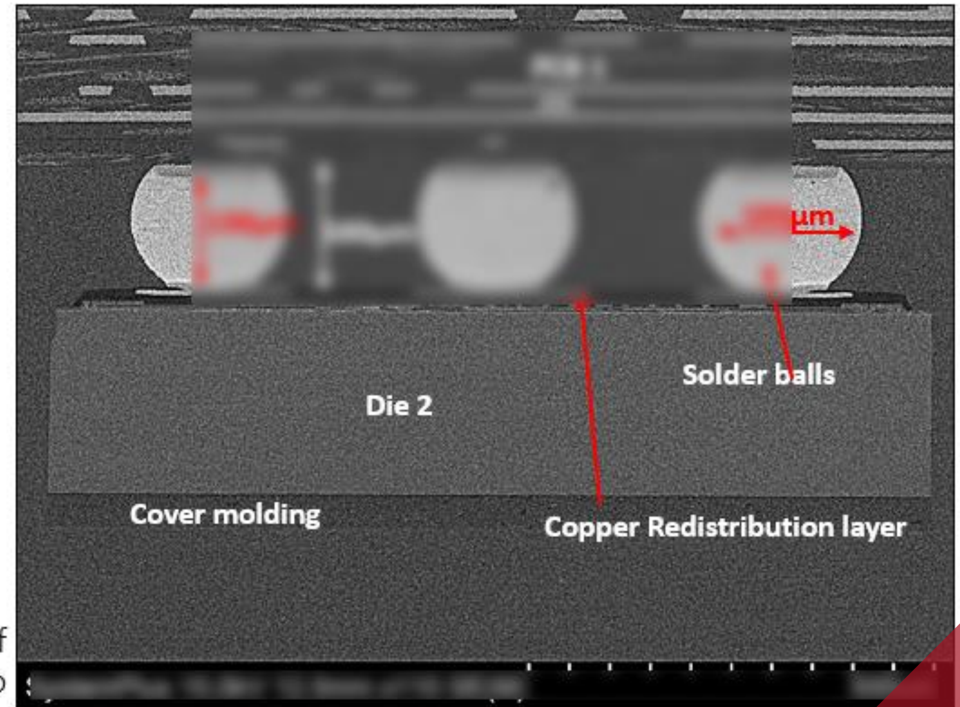

Audio Module Package Cross-Section

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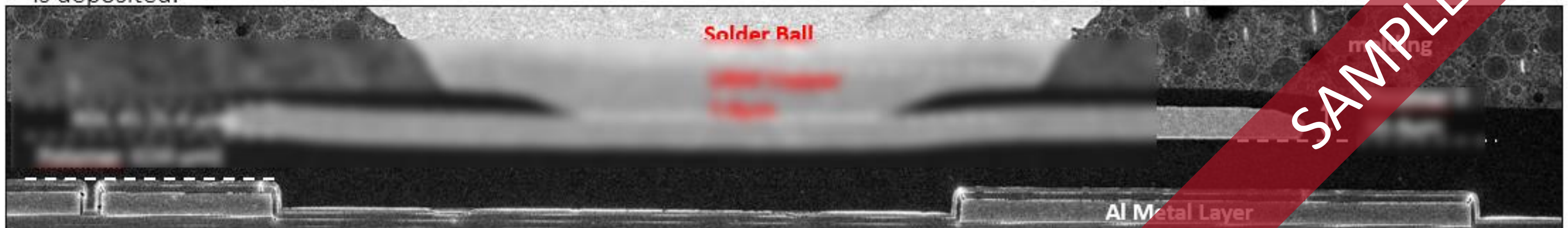
- connect the Operation Amplifier Die 2 to the PCB.
- The layer is deposited and patterned. A thin seed layer of is deposited and polymer layer is deposited and patterned to create opening for the copper redistribution layer.
- The layer is electroplated.
- A and patterned and is deposited.



Audio Module Package Cross-Section – RDL SEM View

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Top Module Circuit Regulator - Die 6 Cross Section

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Top Module - Cross-Sectioning

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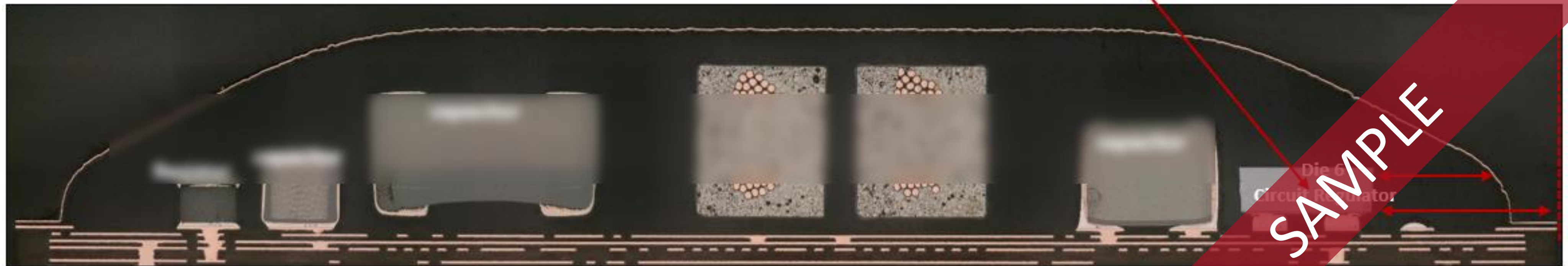

Module Cross-Section 5– Optical View

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- The Cross-Section reveals the passive components and Die 6, the Circuit Regulator PCB .

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Top Module Circuit Regulator - Die 6 Cross-Section

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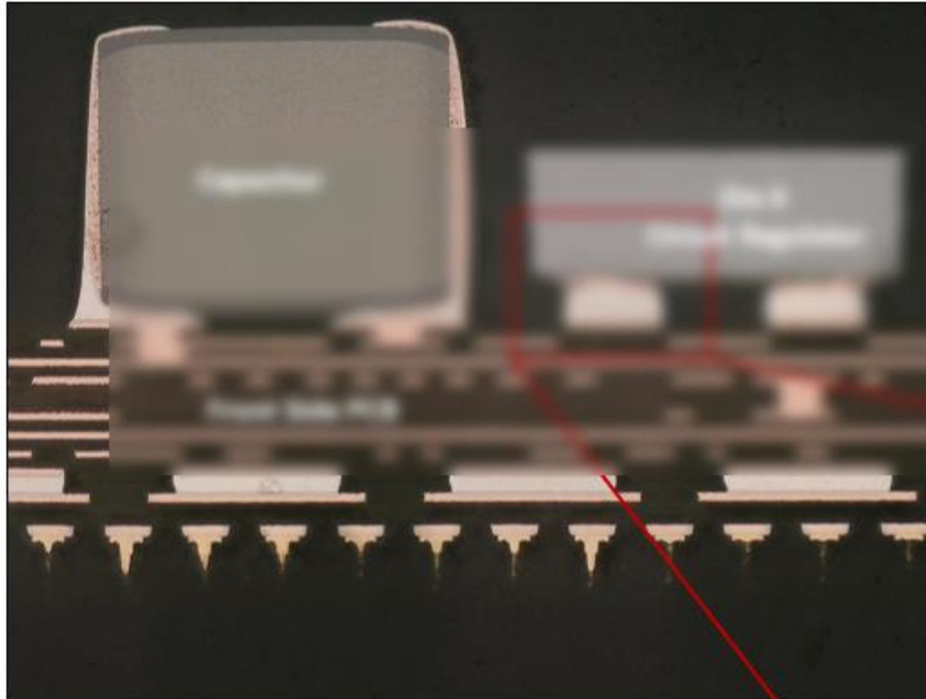

Package Cross-Section
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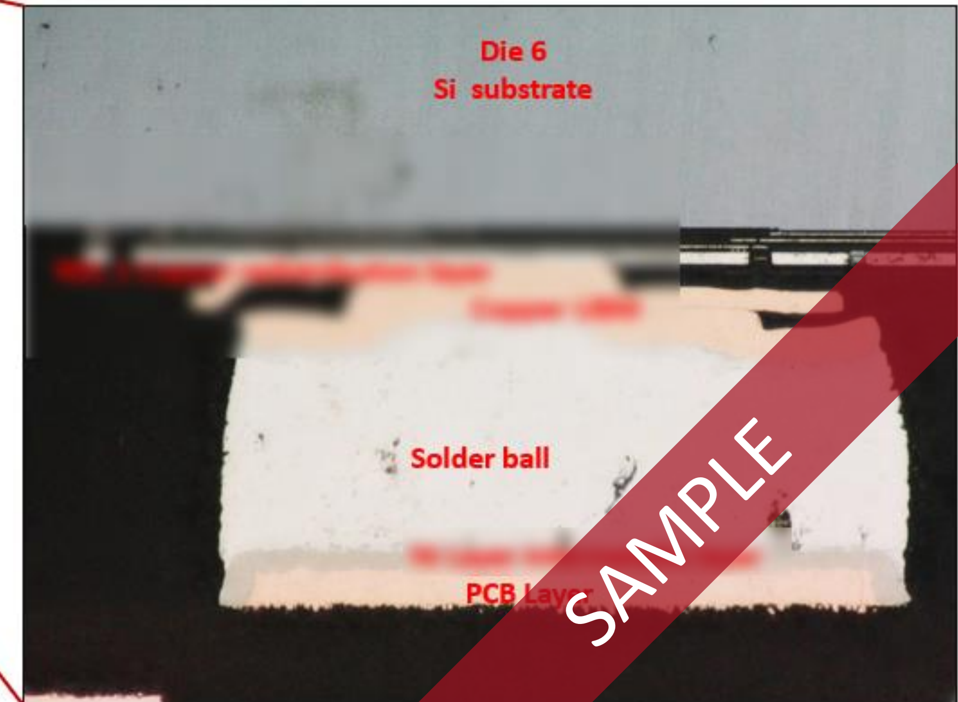
- The circuit regulator die has a [blurred] layer to ensure [blurred] layers.
- [blurred] under the bump is deposited and patterned.
- A [blurred] layer is deposited and patterned. This layer [blurred] between the solder ball and the PCB copper metal.



Package Cross-Section
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Bottom Module Memory Die - Cross-Section

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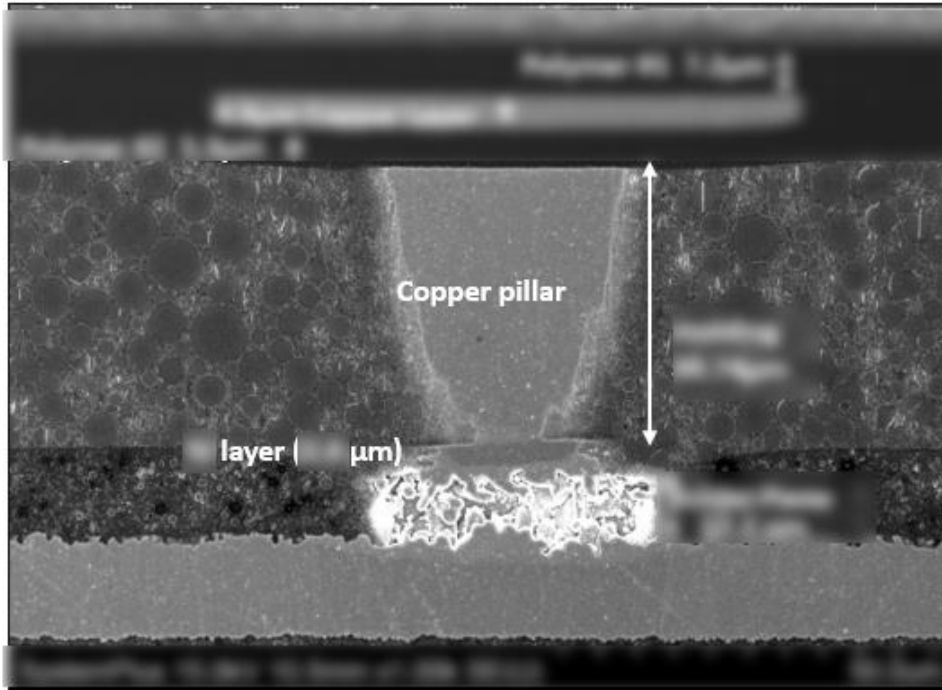

Memory Die Cross-Section
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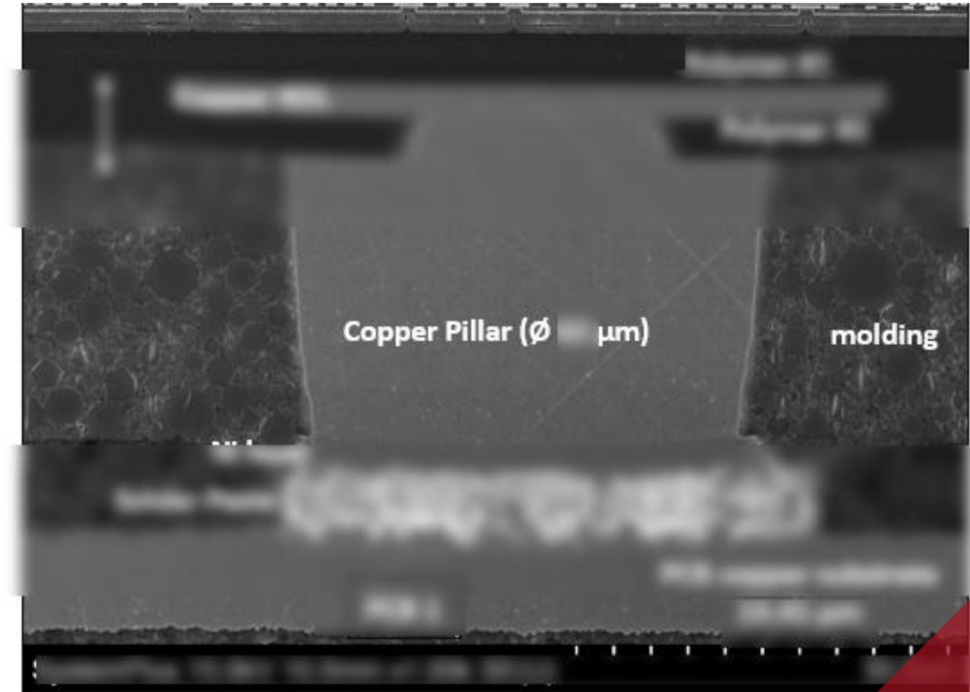

Memory Die Cross-Section
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- is deposited on PCB.
- The attaches the of the die to the PCB.

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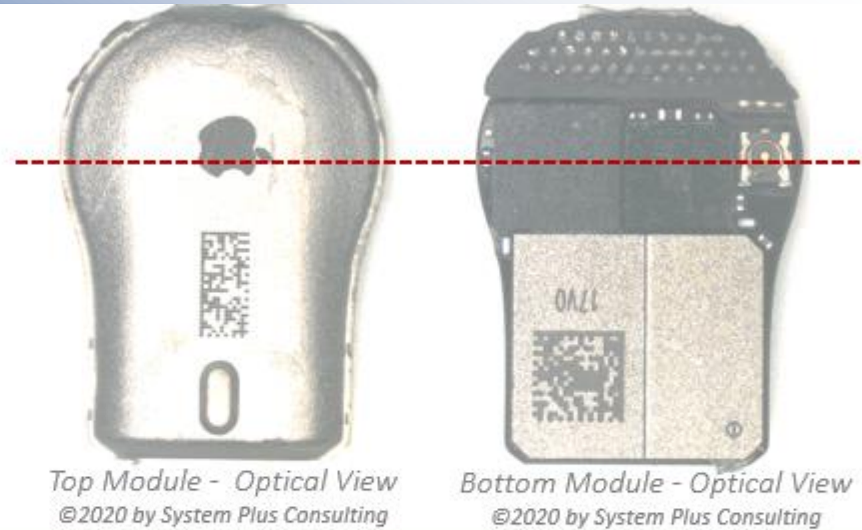
Module Cross-Section - MEMS Modules



Top Module - Optical View
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Bottom Module - Optical View
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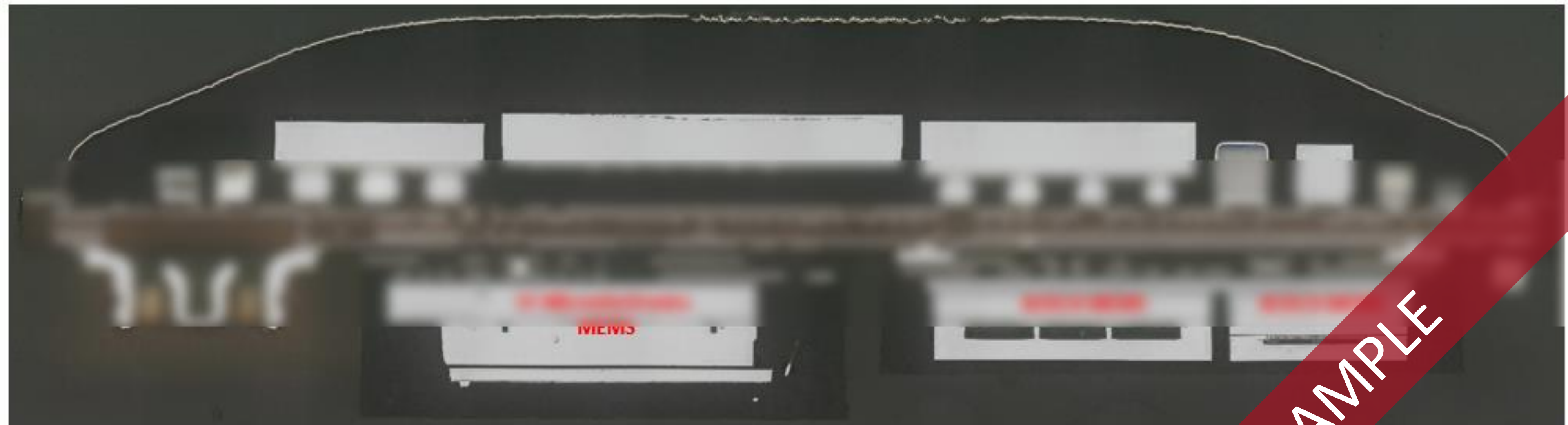

Module Cross-Section – Optical View
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- The Bottom Side has two Sensor Modules integrated on a different PCB.
  - MEMS Module: Accelerometer and Gyroscope
  - Module: Accelerometer

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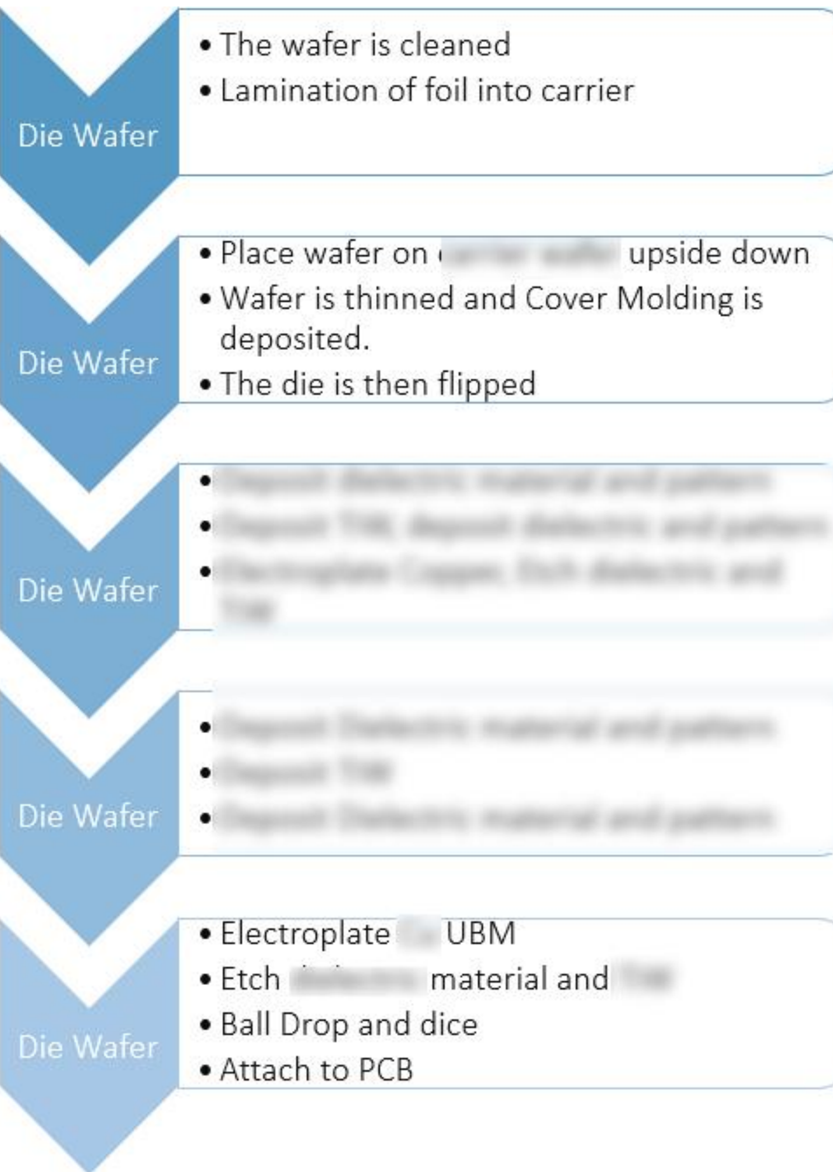
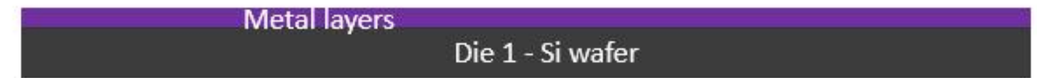
Top Module Die 1 - WLSCP





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H1 Die - Wafer Front-End Cost

Front-End	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Raw wafer Cost 300mm	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Clean Room Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Equipment Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Consumable Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Labor Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
H1 Processor Front-End Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Foundry Gross Profit	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Mask Set Depreciation	[illegible]		[illegible]		[illegible]	
H1 Processor Front-End Price	[illegible]		[illegible]		[illegible]	

H1 Processor Front-End Cost Breakdown (Medium Yield)

The **front-end cost** for the die circuit is estimated between [illegible] **and** [illegible] according to yield.

The largest portion of the manufacturing cost is due to the [illegible]

We estimate a **gross margin of** [illegible] for the die supplier [illegible] and mask set depreciation, which result in a **Wafer price** at [illegible] **in 2020 and** [illegible]

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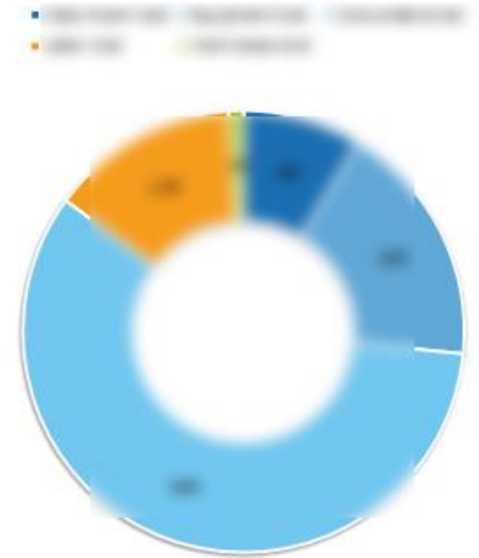
Top Module - Audio Codec Module Packaging Cost

	Low Yield	Medium Yield	High Yield
Audio Code Die Price	[illegible]	[illegible]	[illegible]
Operation Amplifier Die Price	[illegible]	[illegible]	[illegible]
Audio Amplier Die Price	[illegible]	[illegible]	[illegible]
Touch Controller Die Price	[illegible]	[illegible]	[illegible]
LED Driver Die Price	[illegible]	[illegible]	[illegible]
Circuit Regulator Die Price	[illegible]	[illegible]	[illegible]
Passive Compoents Cost	[illegible]	[illegible]	[illegible]
Total Cost of Dies and Passive Components	[illegible]	[illegible]	[illegible]
Dies per Reconstruct Panel	[illegible]	[illegible]	[illegible]
Reconstituted Wafer Cost	$ [illegible]	[illegible]	[illegible]



Bottom SiP Module Assembly	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
PCB Substrate Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Clean Room Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Equipment Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Consumable Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Labor Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Package Manufacturing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
OSAT Gross Profit	[illegible]		[illegible]		[illegible]	
Package Manufacturing Price	[illegible]		[illegible]		[illegible]	

The **Total Cost of Dies and Passive components** is estimated at [illegible].

The Package Manufacturing Cost is estimated between $[illegible] and $[illegible]

We estimate a gross margin of 16% for the die packaging, which result in packaging price between $[illegible] and $[illegible].

The largest portion of the manufacturing cost is due to the [illegible]%.

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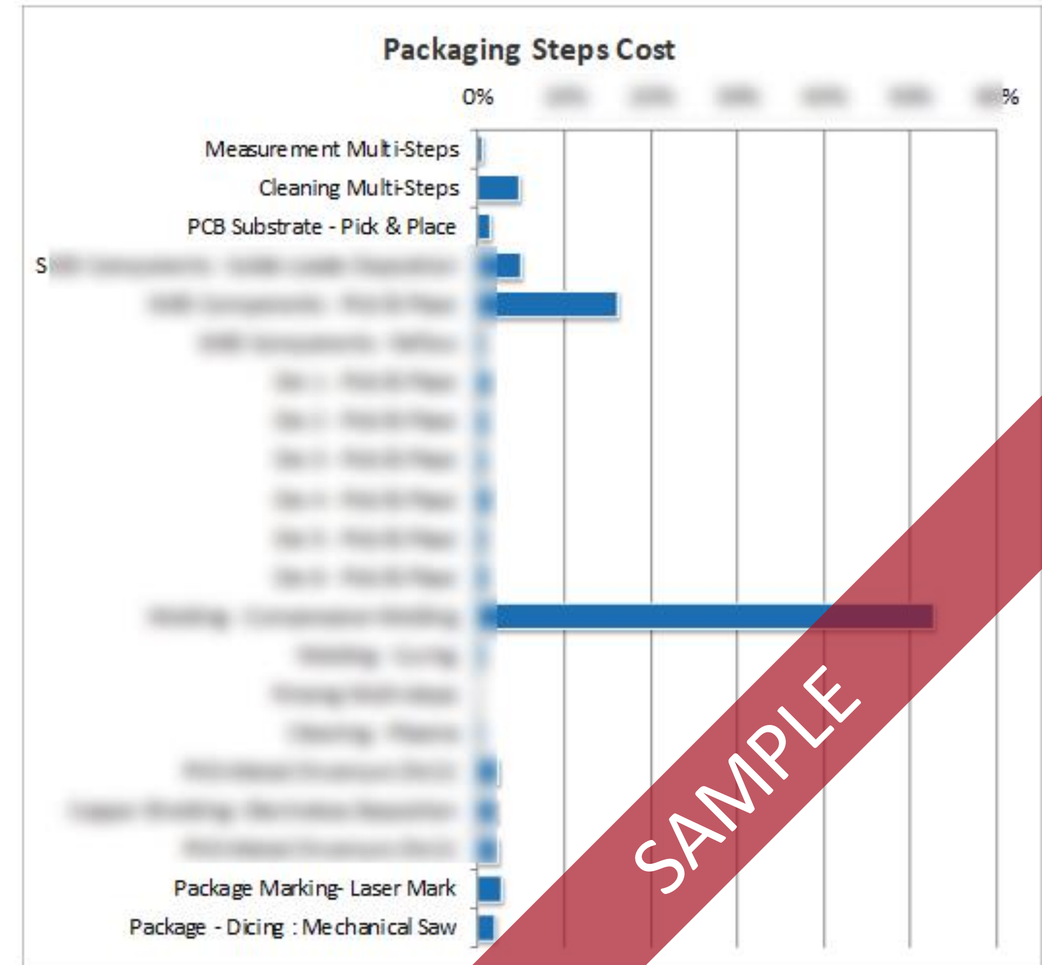
Audio Codec Module - Packaging cost per process steps

Packaging Total Cost Per Step		
Process Operation	TOTAL COST (USD / Unit)	Breakdown
Measurement Multi-Steps	[illegible]	0.4%
Cleaning Multi-Steps	[illegible]	4.8%
PCB Substrate - Pick & Place	[illegible]	1.4%
[illegible]	[illegible]	5.0%
[illegible]	$[illegible]	16.2%
[illegible]	[illegible]	0.7%
[illegible]	[illegible]	1.4%
[illegible]	[illegible]	1.0%
[illegible]	[illegible]	0.8%
[illegible]	[illegible]	1.4%
[illegible]	[illegible]	0.8%
[illegible]	[illegible]	1.0%
[illegible]	$[illegible]	52.8%
[illegible]	[illegible]	0.7%
[illegible]	[illegible]	0.1%
[illegible]	[illegible]	0.4%
[illegible]	[illegible]	2.3%
[illegible]	[illegible]	2.2%
[illegible]	[illegible]	2.3%
Package Marking - Laser Mark	[illegible]	2.7%
Package - Dicing : Mechanical Saw	[illegible]	1.9%
Total	$[illegible]	100.0%



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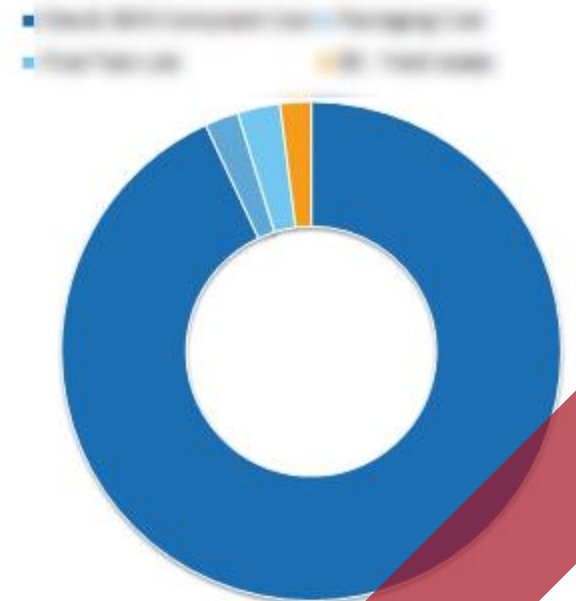
Bottom/H1 Module - Component Cost

	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Dies Cost per Reconstruct Panel& SMD	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Packaging Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Total Panel Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Nb of package per Panel	[illegible]		[illegible]		[illegible]	
Dies & SMD Compoent Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Packaging Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Final Test cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
BE : Yield losses	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Component Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]



The total **panel cost** ranges from $[illegible] according to yield variations.

The number of **good packages per wafer/panel** is estimated at [illegible] which results in a **die cost** ranging from [illegible]

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Module Assembly Cost

The package manufacturing cost is estimated between [illegible]

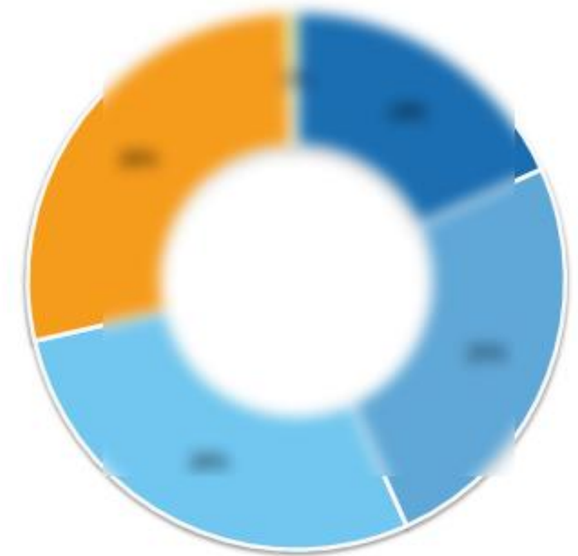
The largest portion of the manufacturing cost is due to the [illegible]

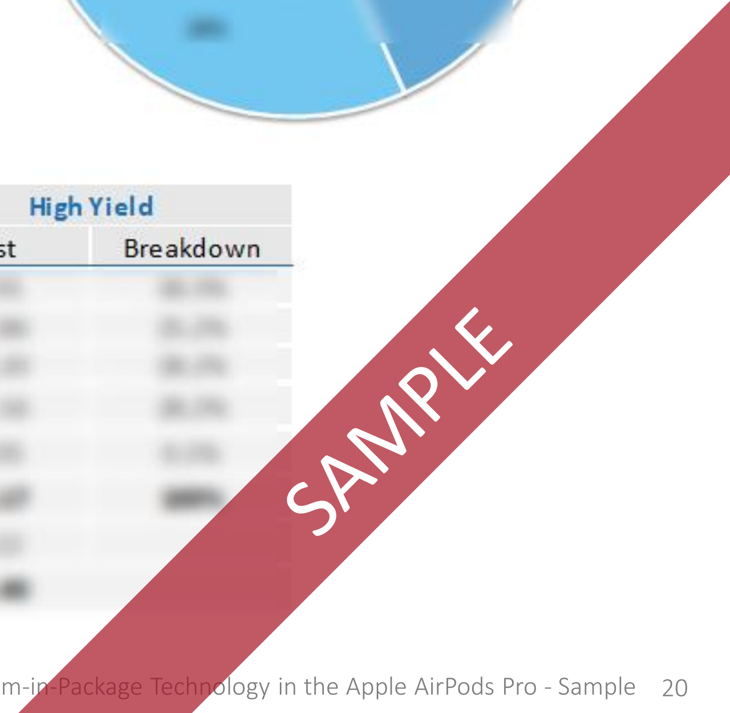
We estimate the packaging gross margin of [illegible], this results at the packaging price varying from [illegible]

	Low Yield	Medium Yield	High Yield
Top Module	[illegible]	[illegible]	[illegible]
Bottom H1 Module	[illegible]	[illegible]	[illegible]
ST Microelectronics MEMS Module	[illegible]	[illegible]	[illegible]
Bosch MEMS Module	[illegible]	[illegible]	[illegible]
Passive Components & Antenna	[illegible]	[illegible]	[illegible]
2-Layer Added PCB	[illegible]	[illegible]	[illegible]
Total	[illegible]	[illegible]	[illegible]
Dies per Reconstruct Panel	[illegible]	[illegible]	[illegible]
Reconstituted Wafer Cost	$[illegible]	[illegible]	[illegible]

Final Module Assembly	Low Yield		Medium Yield		High Yield	
	Cost	Breakdown	Cost	Breakdown	Cost	Breakdown
Clean Room Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Equipment Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Consumable Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Labor Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Yield losses Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
Package Manufacturing Cost	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
OSAT Gross Profit	[illegible]		[illegible]		[illegible]	
Package Manufacturing Price	[illegible]		[illegible]		[illegible]	

Package Manufacturing Cost Breakdown (Medium Yield)

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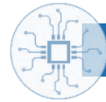

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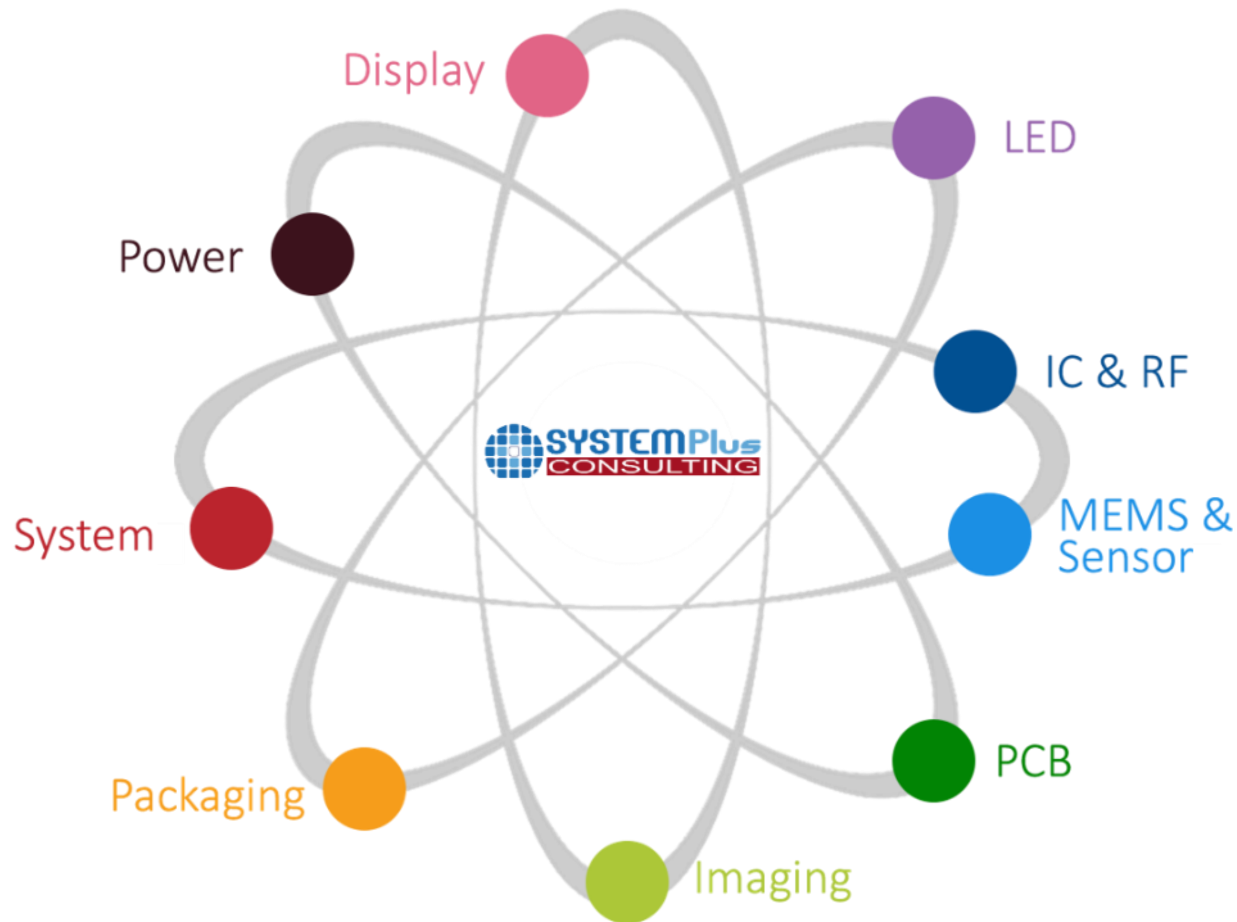

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