A Quick Look at 14-nm and 10-nm Devices

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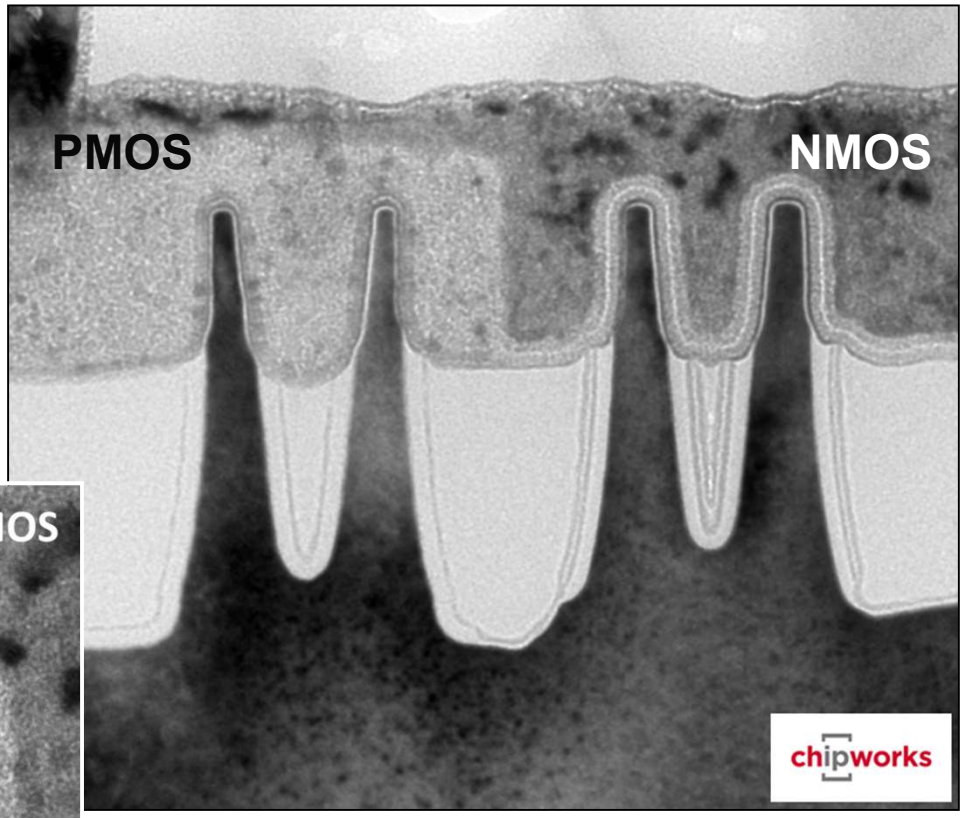
Siliconics

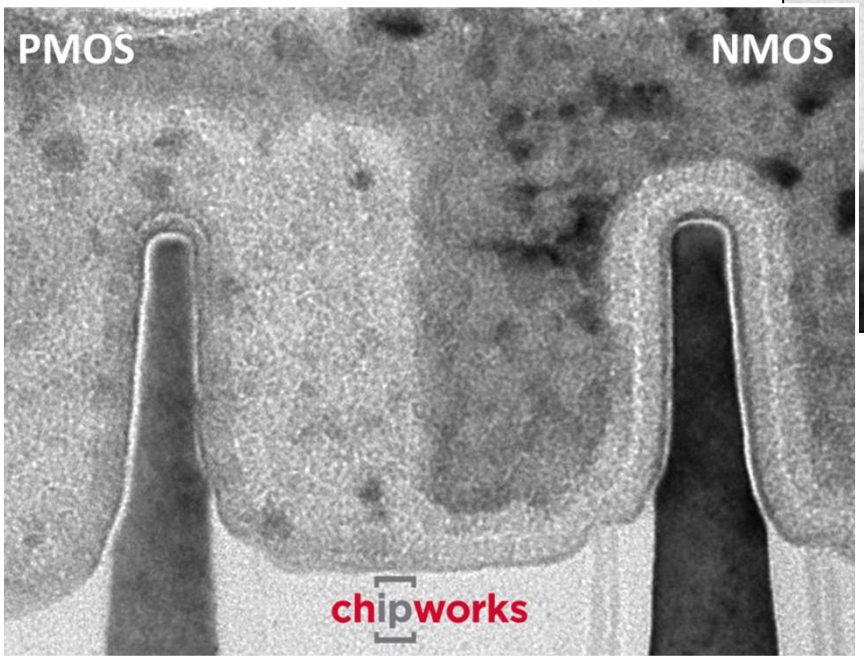
Outline

- Intel 14-nm & 14+
- Intel 10-nm announcements
- TSMC 10-nm
- Samsung 10-nm
- GLOBALFOUNDRIES announcements

Intel 14-nm Broadwell

- Vertical fins! But still rounded fin tops.
- PMOS gates formed first
- W fill in NMOS
- Multiple steps to achieve fin profiles after fin etch





- Asymmetric stress deforms fins
  - Leftmost fin leans left
  - Rightmost fin leans right

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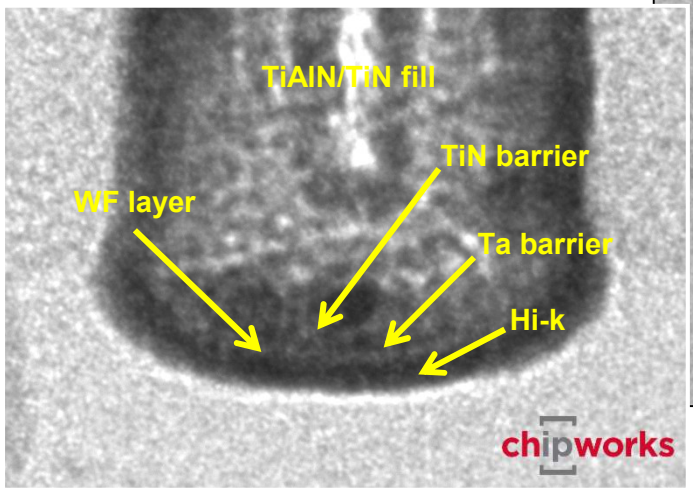
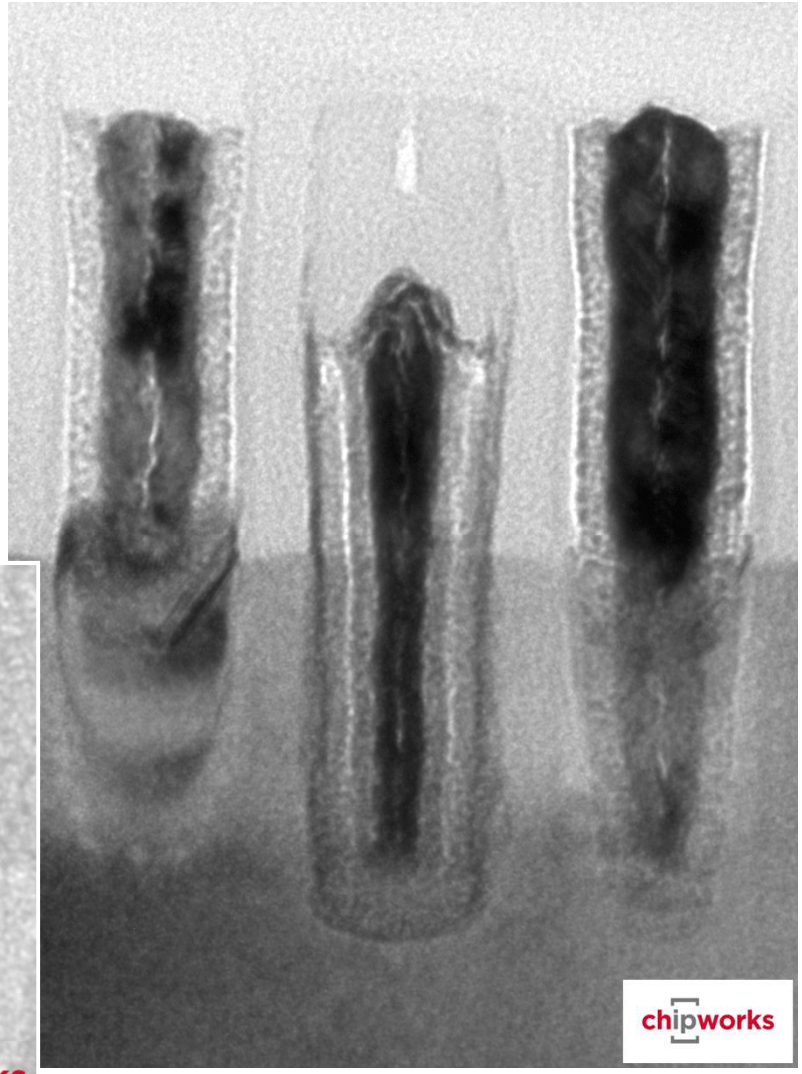
Intel 14-nm – PMOS Gates

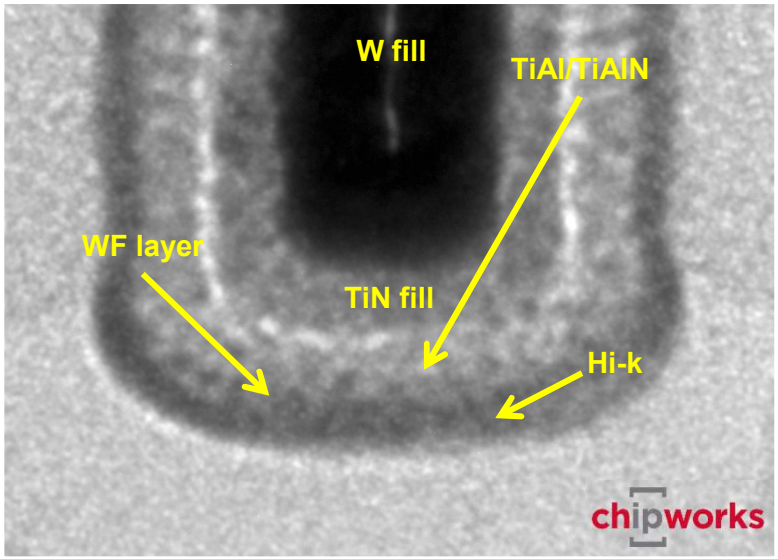
- Minimum gate length observed ~22 nm
- TiN work-function metal
- Epi SiGe in PMOS source-drains, isotropic cavity etch without tilt implant
- Gates back-etched and filled with dielectric, allows self-aligned contacts



Intel 14-nm – NMOS Gates

- TiAlN work-function metal
- SWS etched before S/D epi growth
- Ti silicide, not Ni





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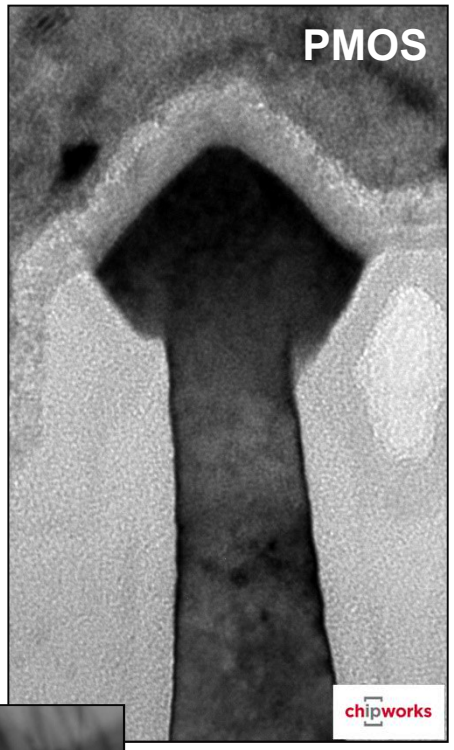
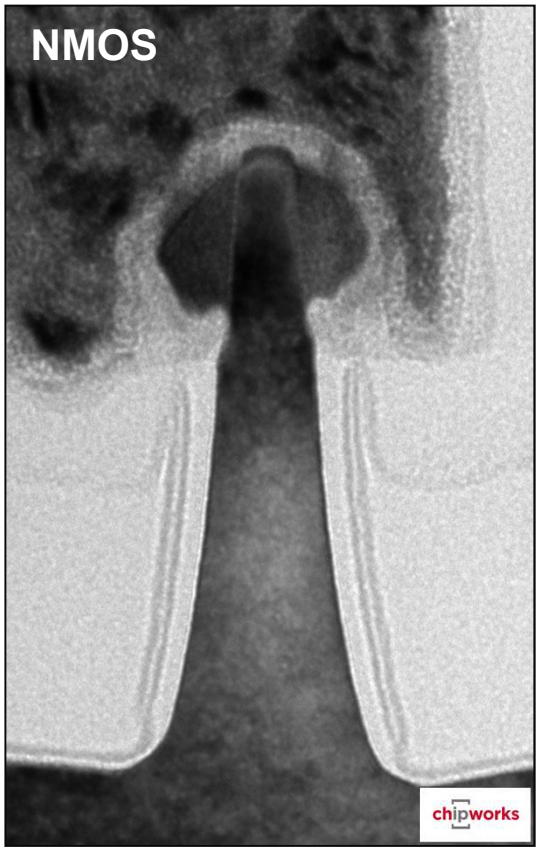
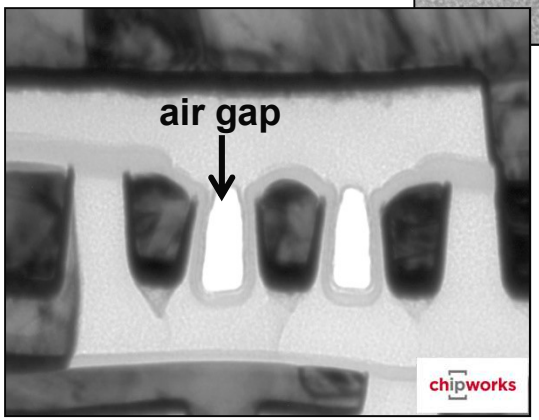
Intel 14-nm – Source/Drains

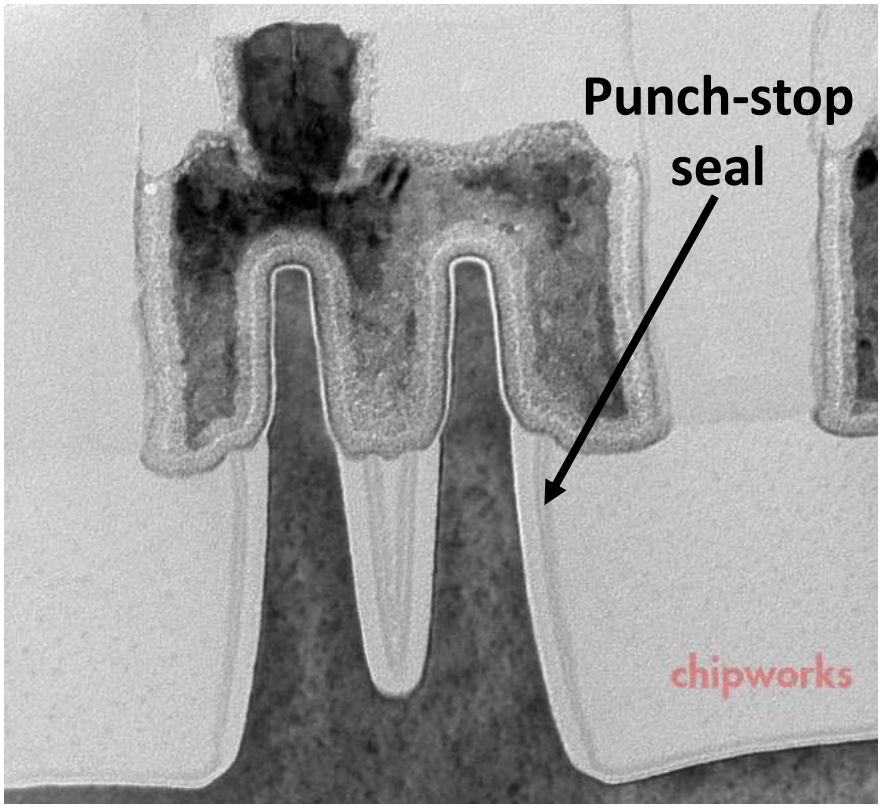
- PMOS epi-SiGe takes <111> planes as in 22-nm
- NMOS epi takes <111> planes at base
  - Cavity etch used
- SWS etched before S/D epi growth in PMOS and NMOS
- And.. here be airgaps!







Intel Solid-Source Diffusion Punch-stopper



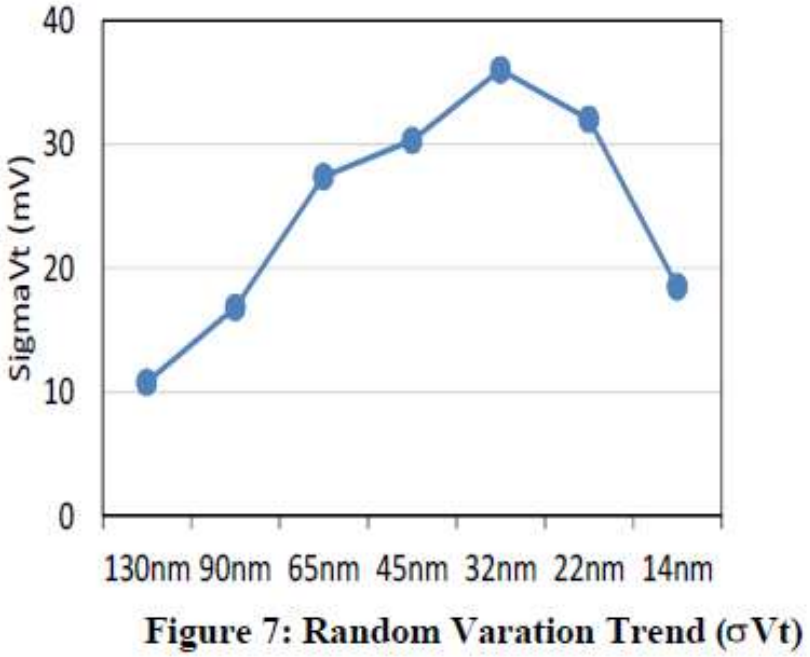


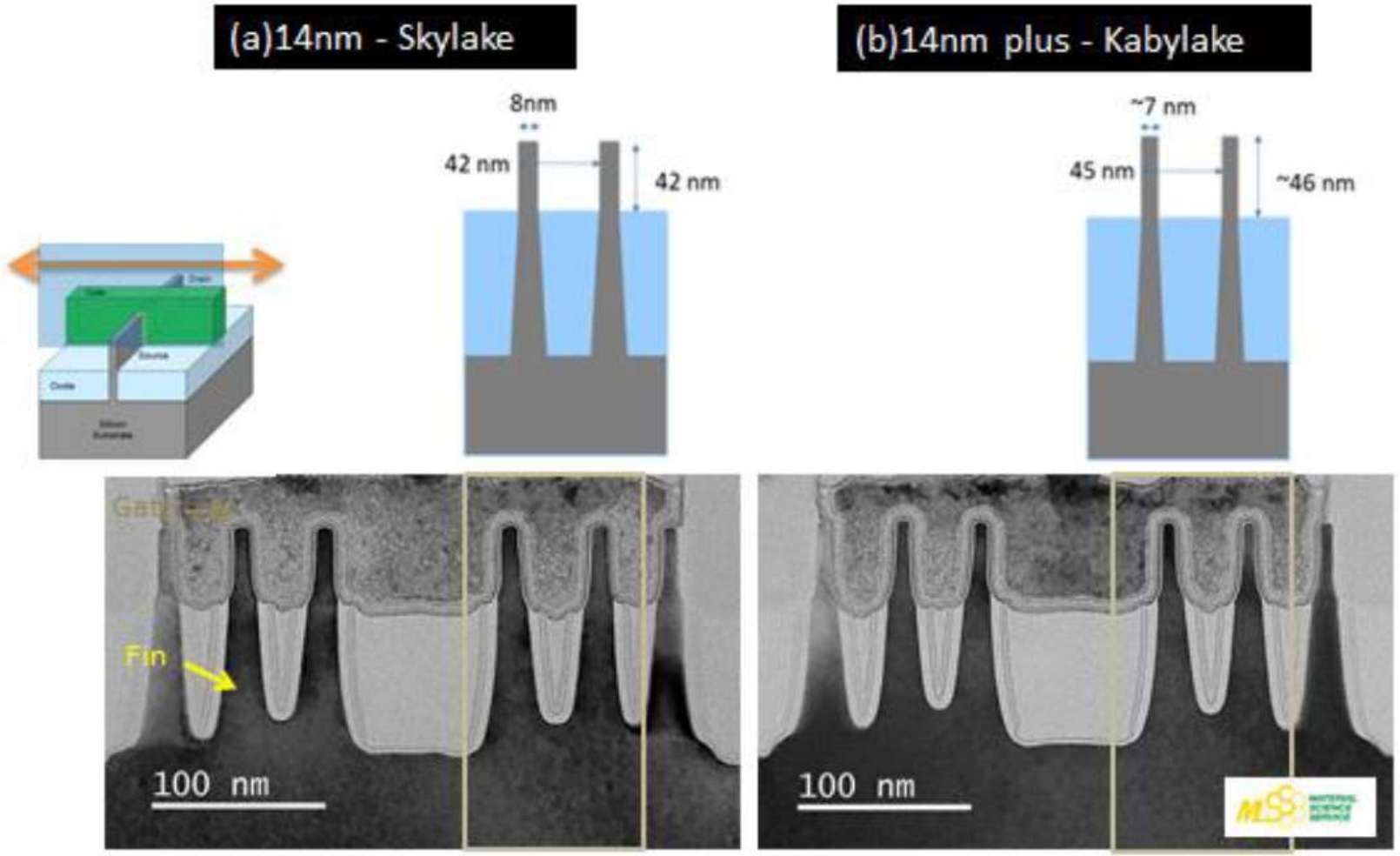
Figure 7: Random Varation Trend (σVt)

Natarajan, et al. "A 14nm Logic Technology Featuring 2nd-Generation FinFET , Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588 μm2 SRAM cell size", IEDM 2014

- Intel solved one of the biggest problems with bulk FinFETs by putting in a self-aligned punch-stop diffusion
- Allows bulk FinFET to be undoped, assuming multi-WF RMG

Intel 14 nm Skylake vs 14+ Kaby Lake

- Fin geometry improved, narrower and taller fins



Source: MSSCorps

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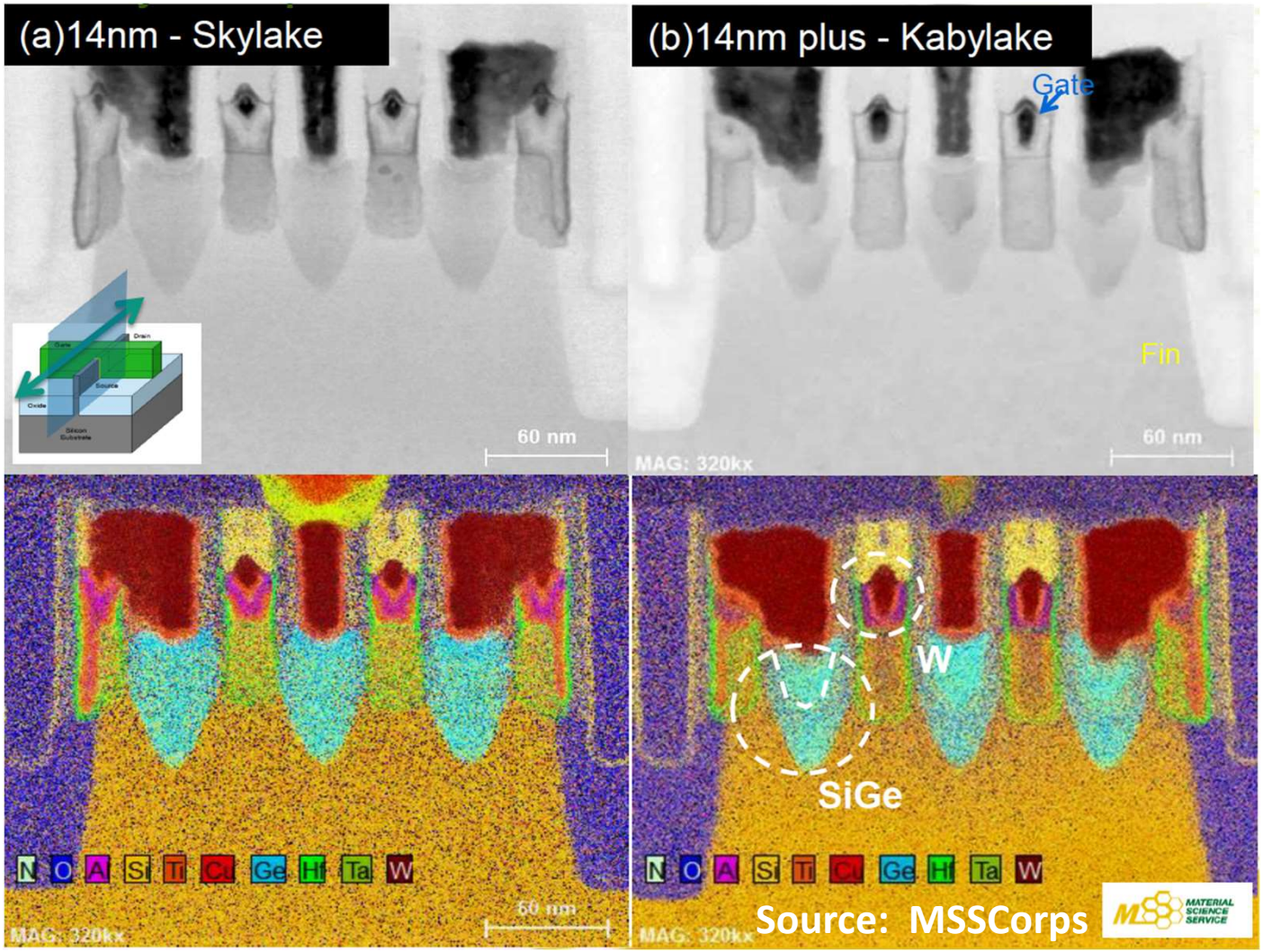
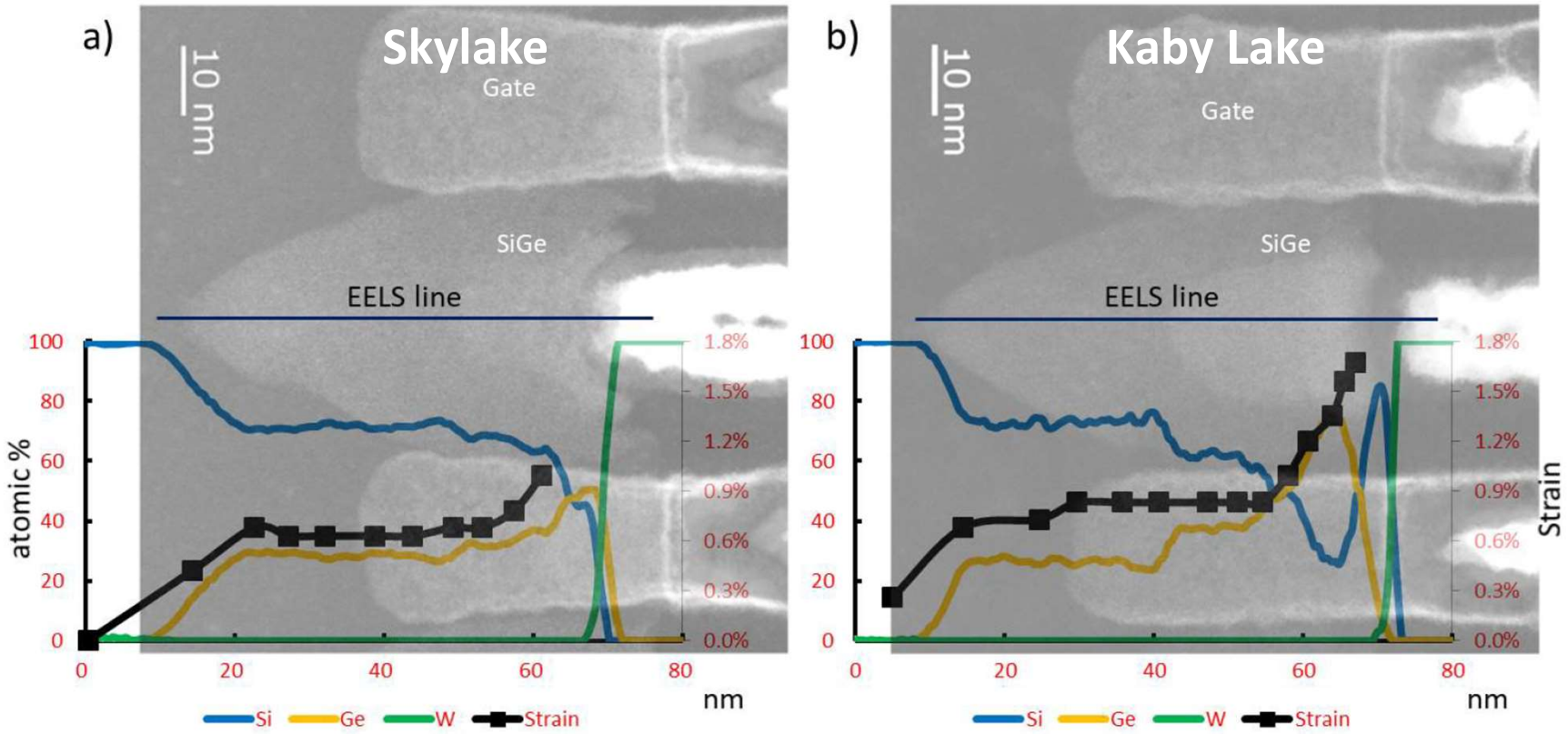
Intel 14 nm Skylake vs 14+ Kaby Lake



- TEM & EDS show more Ge in PMOS source/drains, more tungsten in gate stack

Intel 14 nm Skylake vs 14+ Kaby Lake



Source: MSSCorps

- Higher Ge confirmed with EELS, higher strain monitored with STEM Moiré analysis

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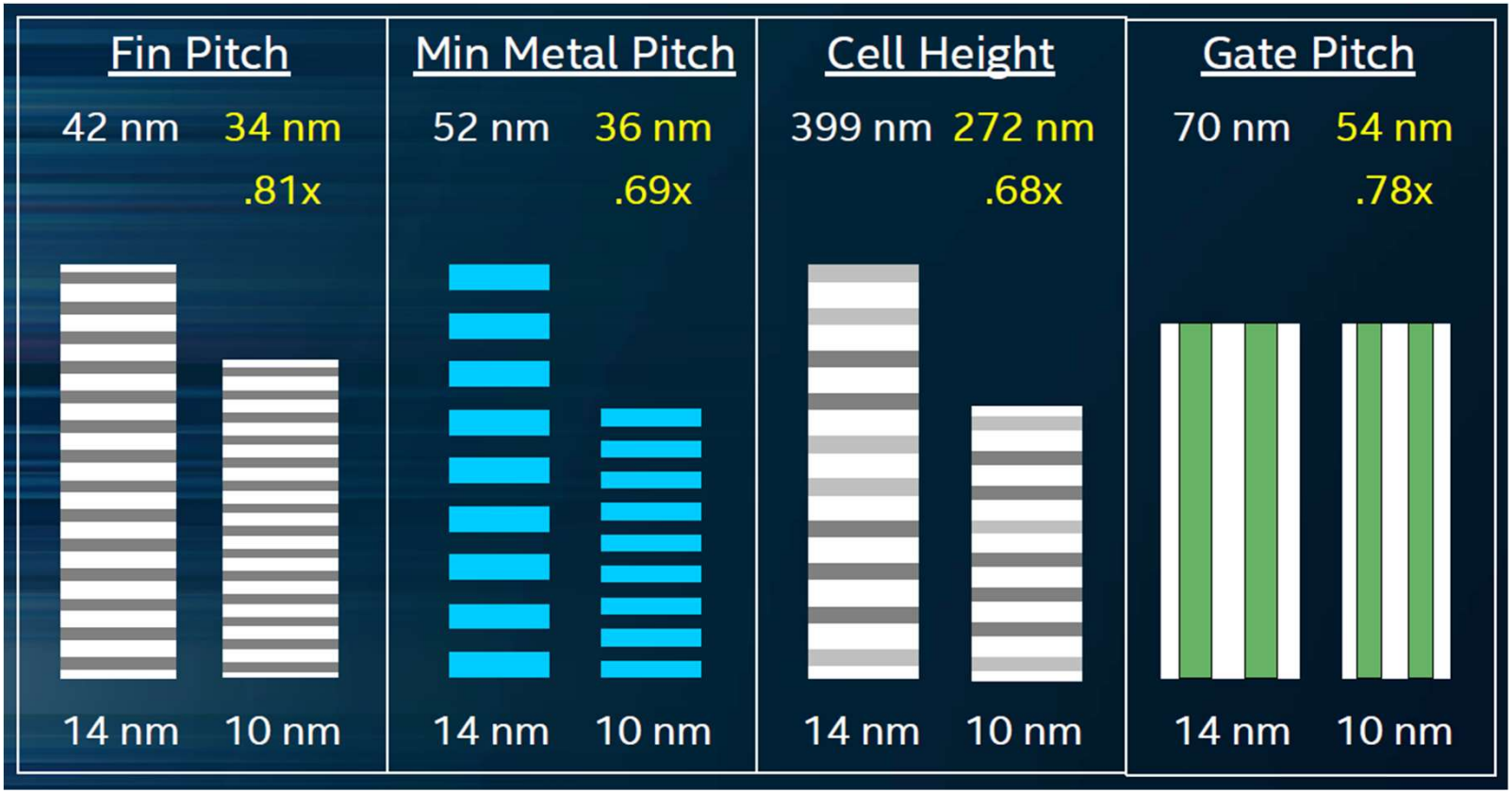
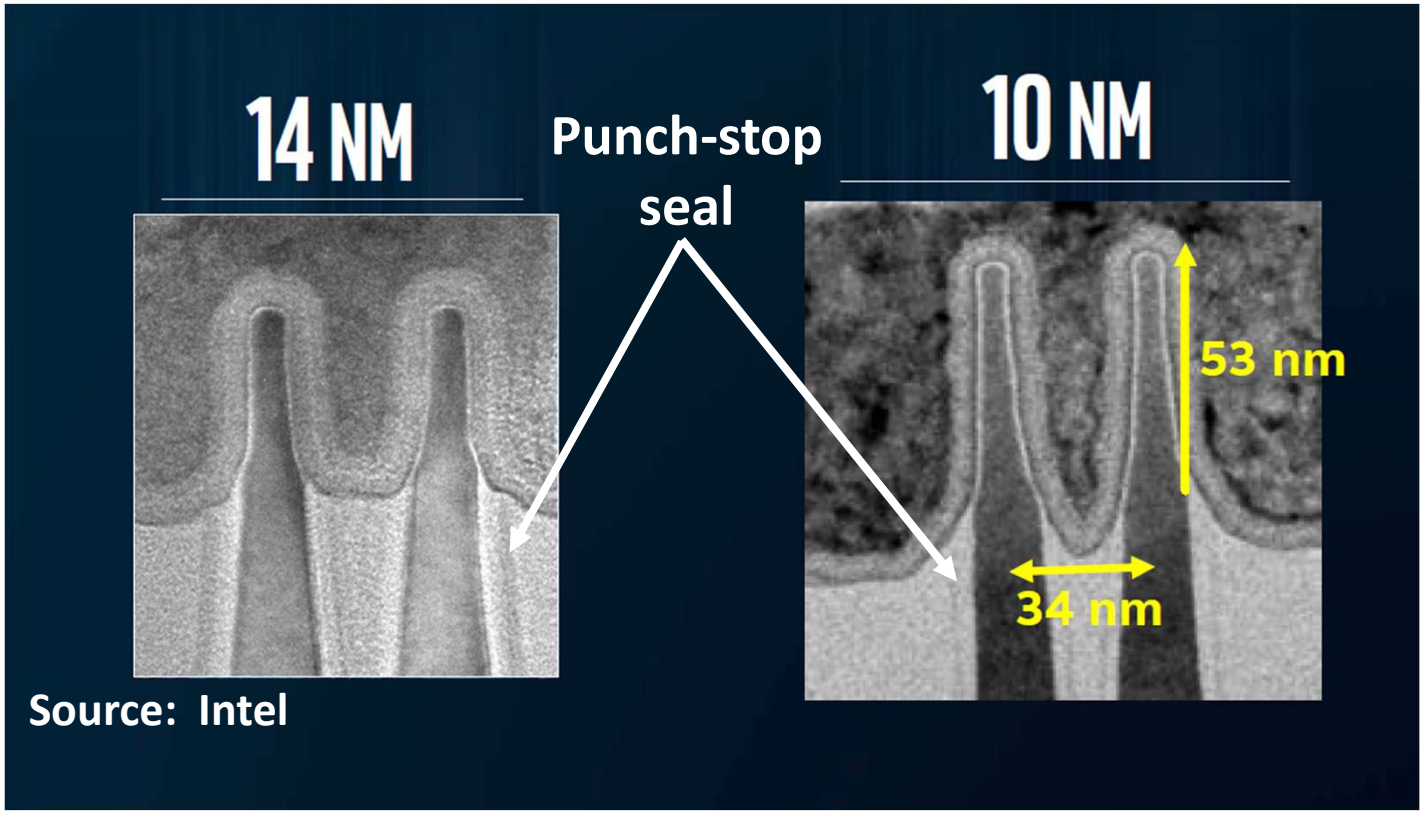
Intel 10-nm Announcements



Source: Intel

- Self-aligned quad patterning (SAQP) used for fins and M1
- 13 layers of metal (including M0), ULK throughout the stack
- With process and design changes, Intel claims scaling of 63%

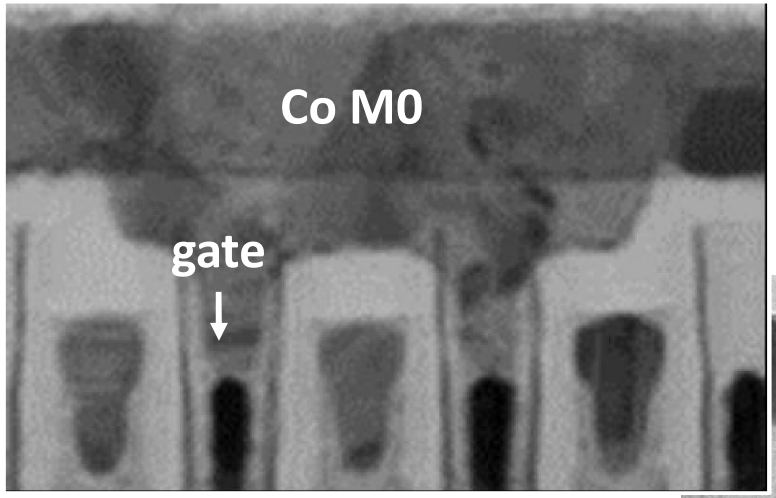
Intel 10-nm Announcements



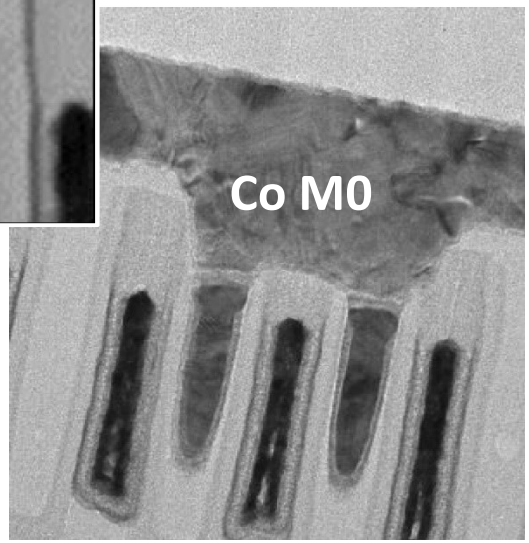
- Fin height up from 34 to 42 to 53 nm, (IEDM17 46 nm) fin width 5 – 15 nm, ~7 nm at half height. Fin height is tunable with a range of ~10 nm.
- Solid-source diffusion punch-stopper used again
- Gate stack looks similar, 5th generation HKMG but 4 – 6 WFs, 7th gen strain

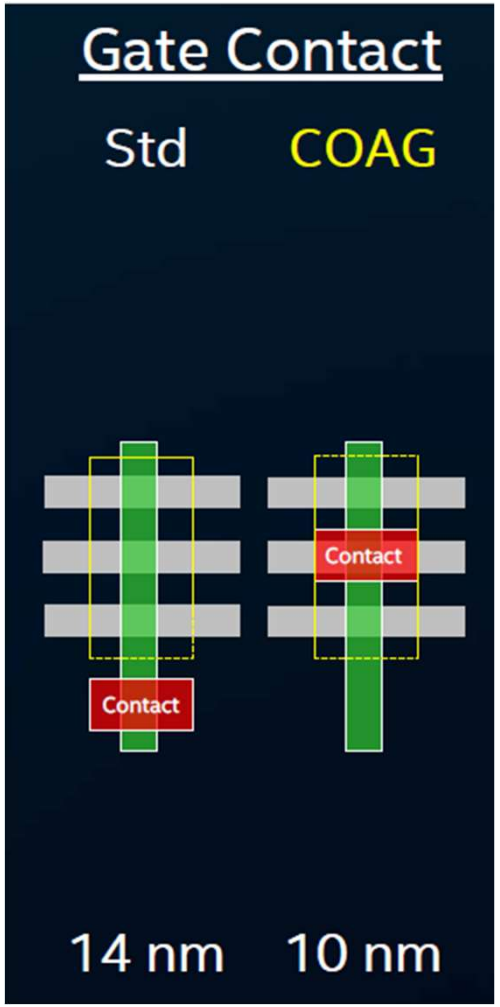
Intel 10-nm Hyper Scaling – COAG

- COAG – contact over active gate – 2-step contact etch with SiN mask over gate and SiC mask over contact trenches
- Cobalt M0 & M1 (with Ru?), Co cap on M2 – M5



Source: Intel/IEDM

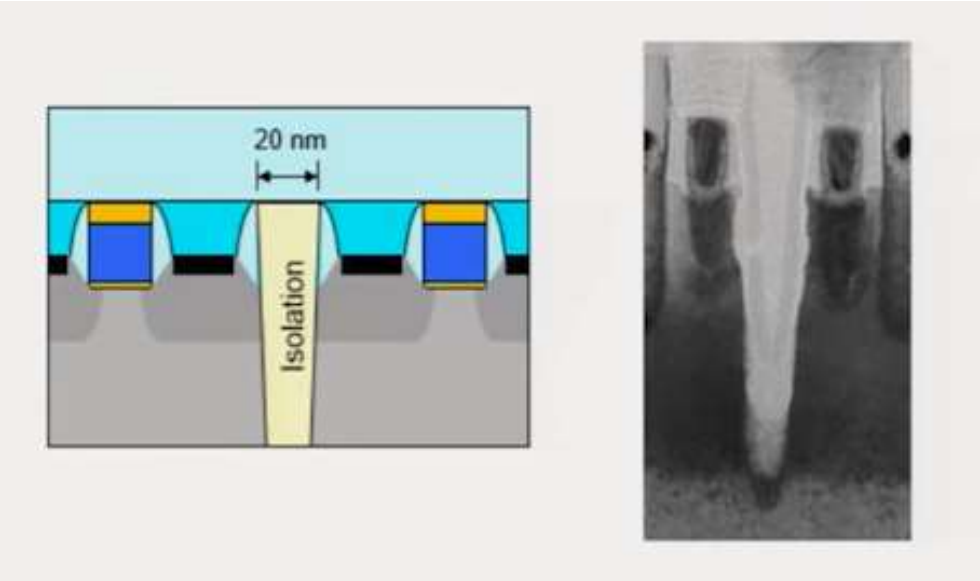


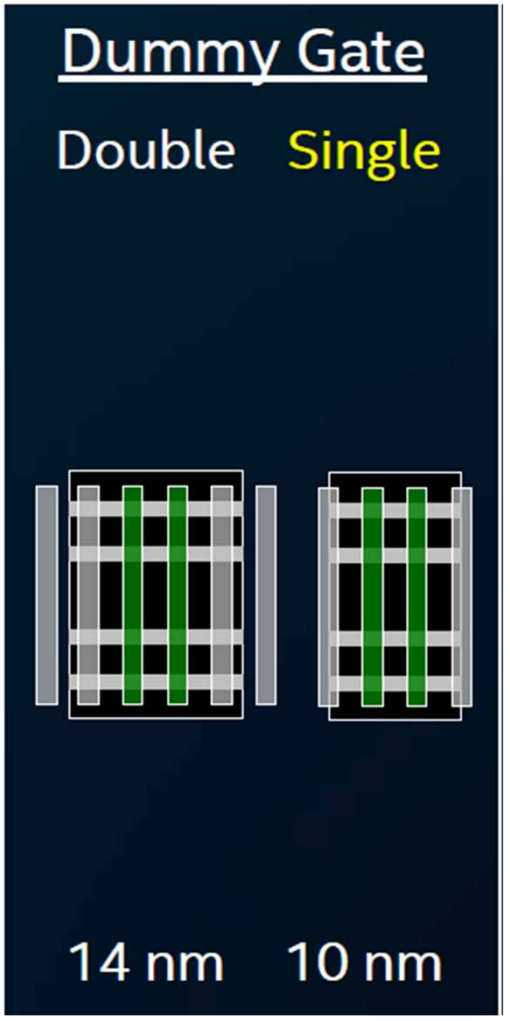


Source: Intel

Intel 10-nm Hyper Scaling – Single Dummy Gate

- Dummy gates normally on fin ends
- Single dummy gate spacing between fin ends, saves a gate pitch when packing two cells together, a claimed 20% cell area saving
  - No dummy gate in the finished product, just the fin etched in single dummy gate position.
  - Dummy polySi gate used, allowing source/drain formation without risking the fin edge; polySi removal etches fin to separate the cells.

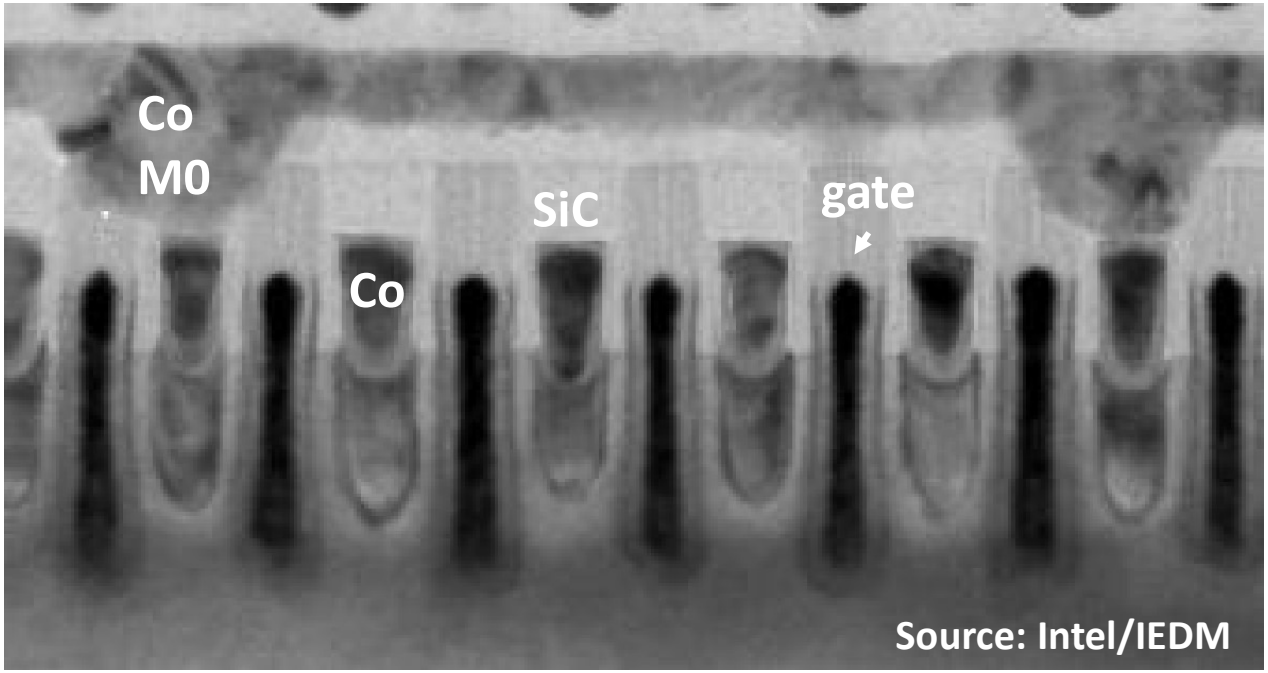


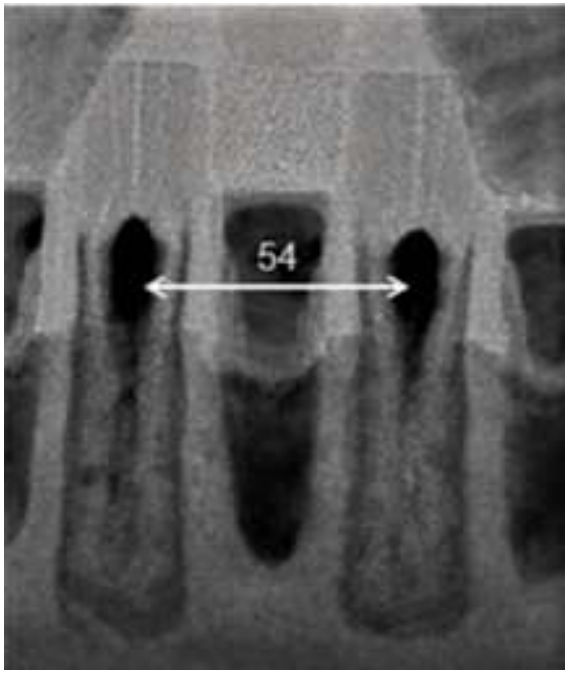


Source: Intel

Intel 10-nm

- Minimum gate length 18 nm, gate width ~97 nm with 46 nm fin height, cf ~85/73 nm in 14/22-nm
- K-value of sidewall spacers lowered, reducing C_{cg} by 10%
- Source/drain epis in-situ doped, add strain (N- & P-MOS or both?), NMOS also has ILD stress, giving ~10% improvement

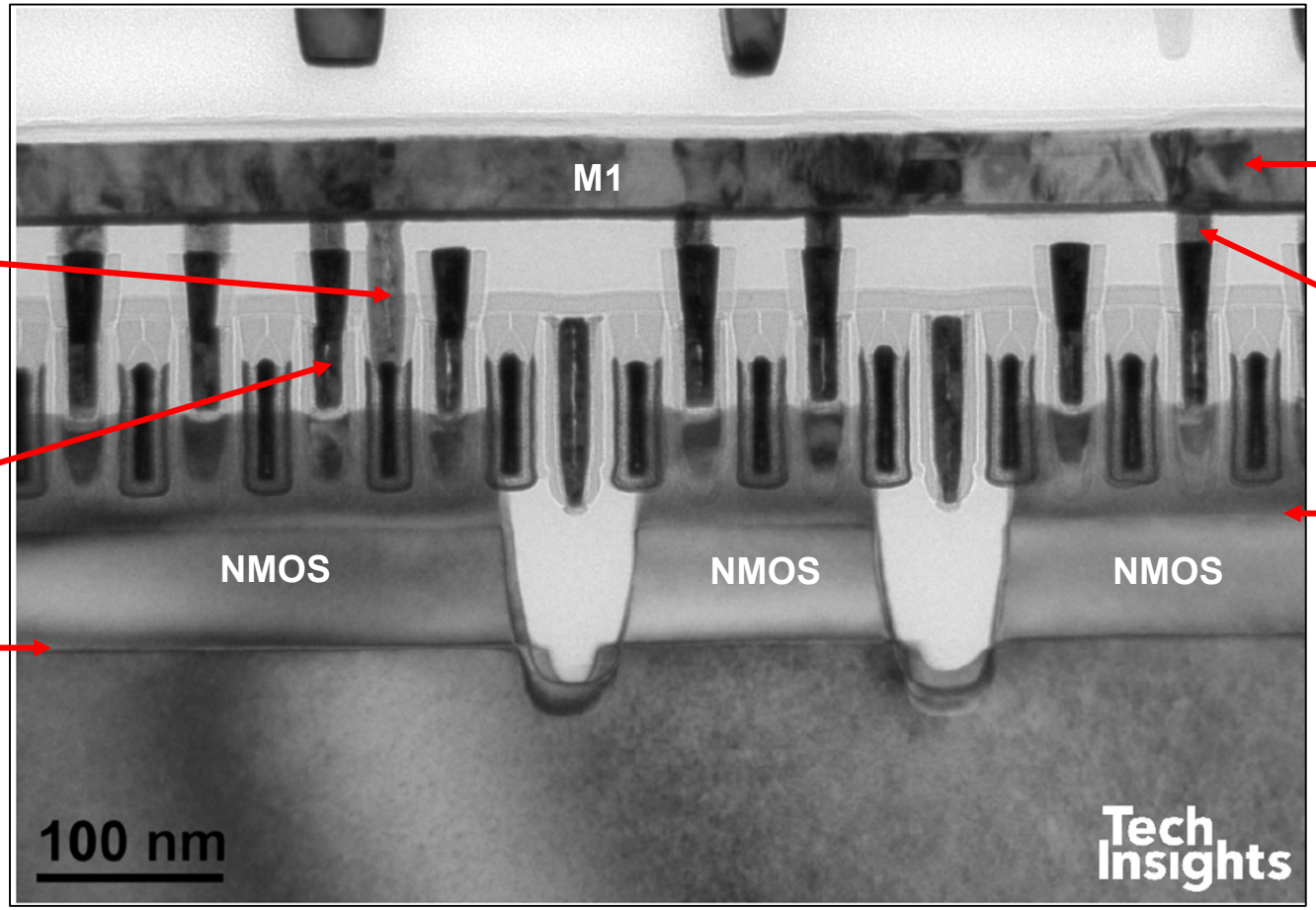




Source: Intel

TSMC 10 nm – Apple APL1071 (A10X)

- Multiple work-function transistors, double dummy gate
- Contacted gate pitch 66 nm, minimum Lg ~25 nm, MMP 44 nm



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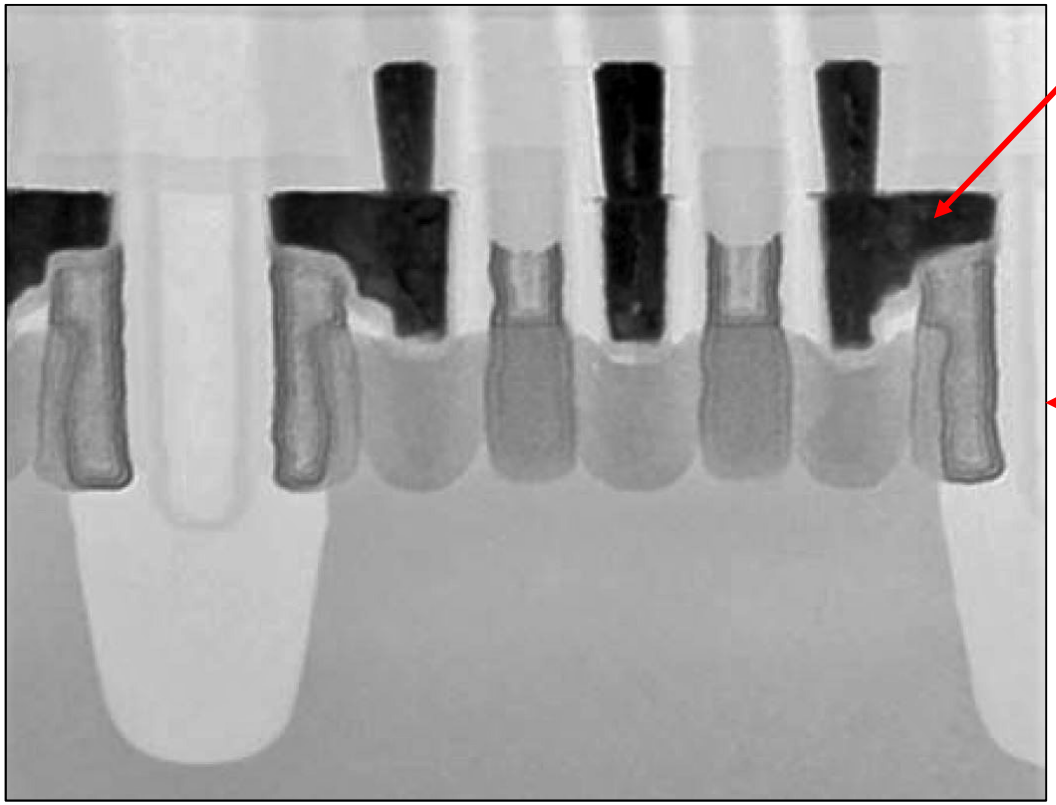
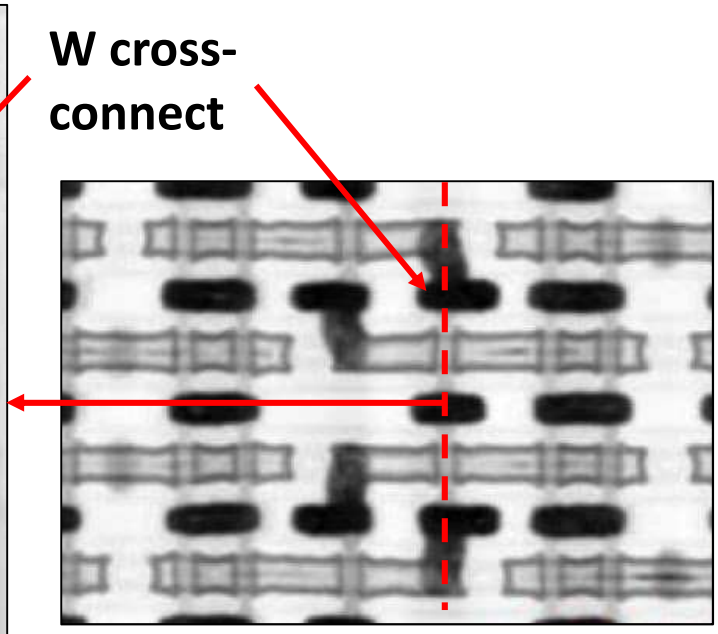
TSMC 10 nm – Apple APL1W72 (A11)

- PMOS transistors in SRAM array – 6-transistor cell
- Thin sample, ~10 nm, shows gate widening on fin sides
- Gates back-etched, capped with SiN, self-aligned contacts, minimal gouging into S/D epi



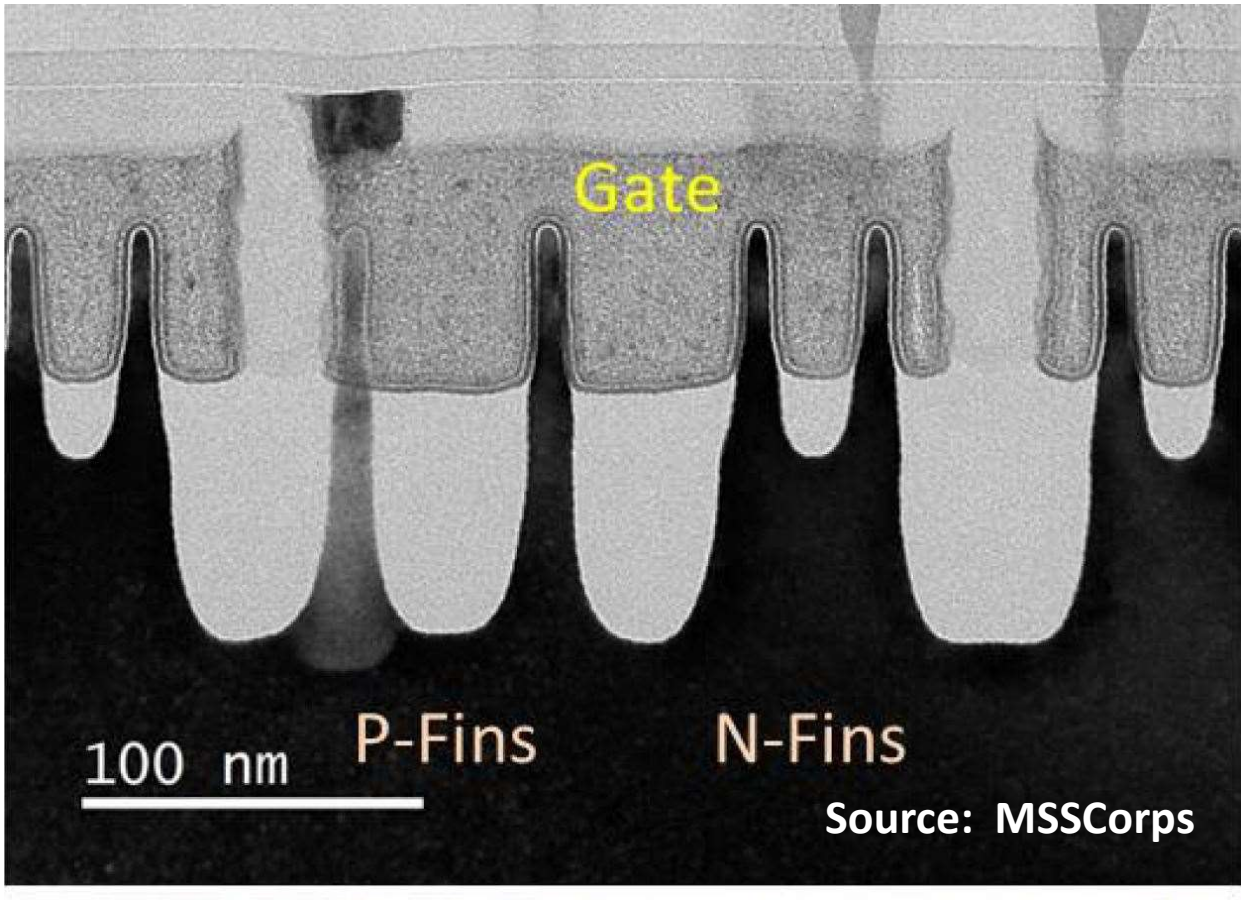


Plan-view TEM in SRAM area

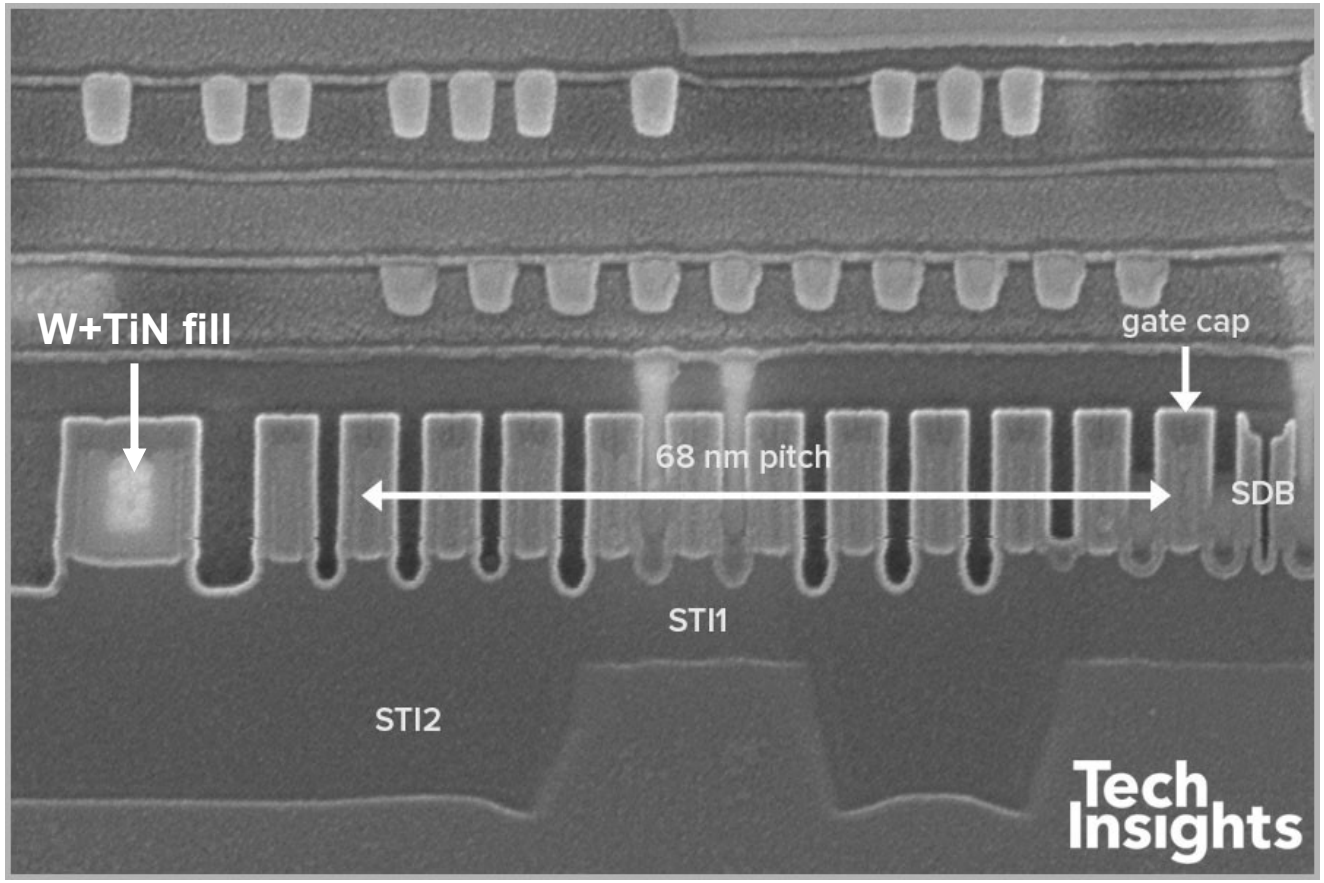
Source: MSSCorps

TSMC 10 nm – Apple APL1W72 (A11)

- SAQP minimum fin pitch ~33 nm, fin width ~6 nm, functional gate height ~44 nm, gate width ~95 nm
- Distinct fin isolation and well isolation

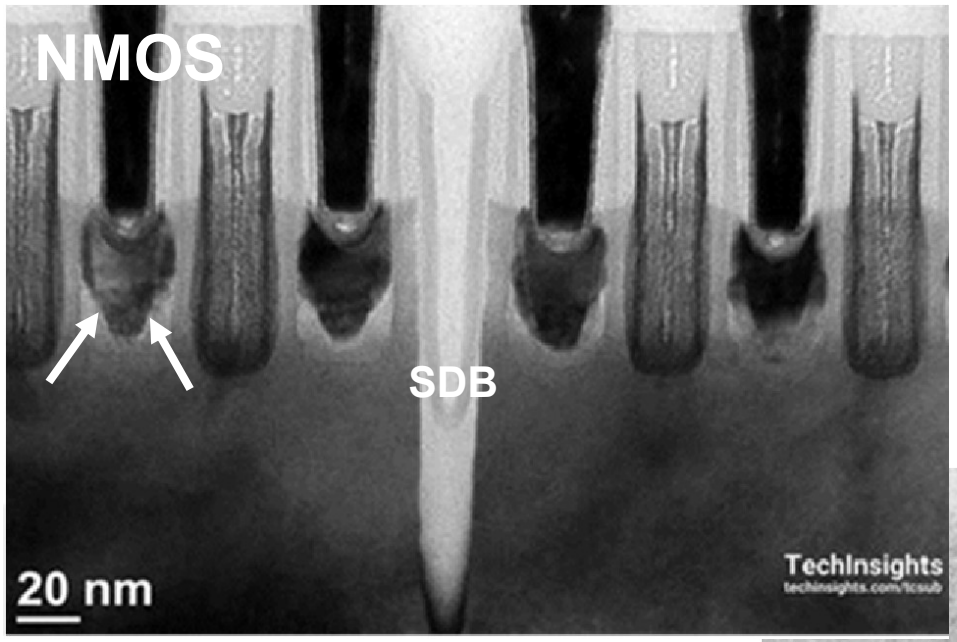


Samsung 10LPE (Qualcomm Snapdragon 835)

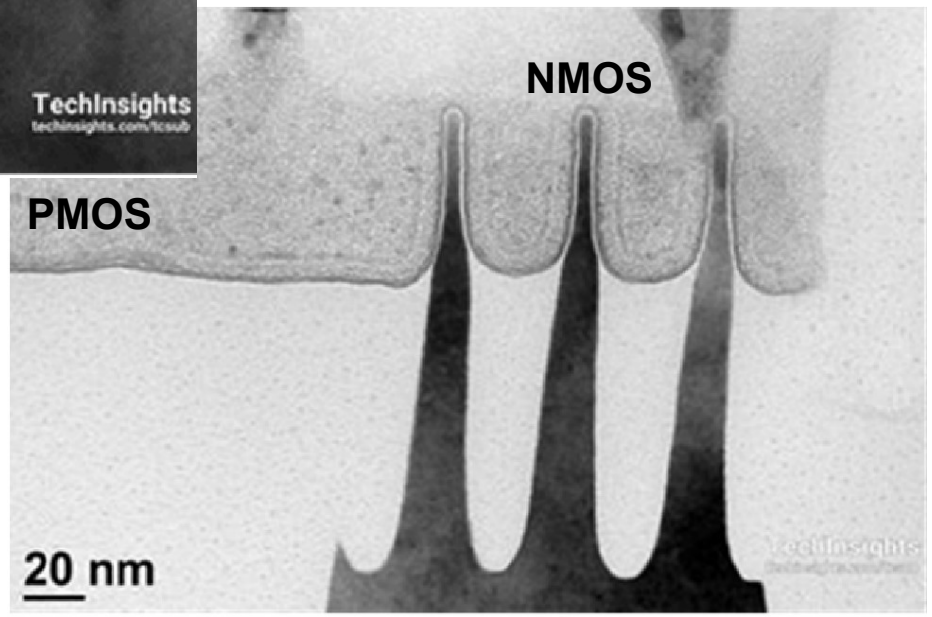


- Minimum CGP/MxP/FP 68/48/42 nm, SADP fins and gates, LELE metal
- Dual STI including single diffusion break (SDB) – but no dummy gate in break
- W/TiN fill in longer gates

Samsung 10LPE (Qualcomm Snapdragon 835)



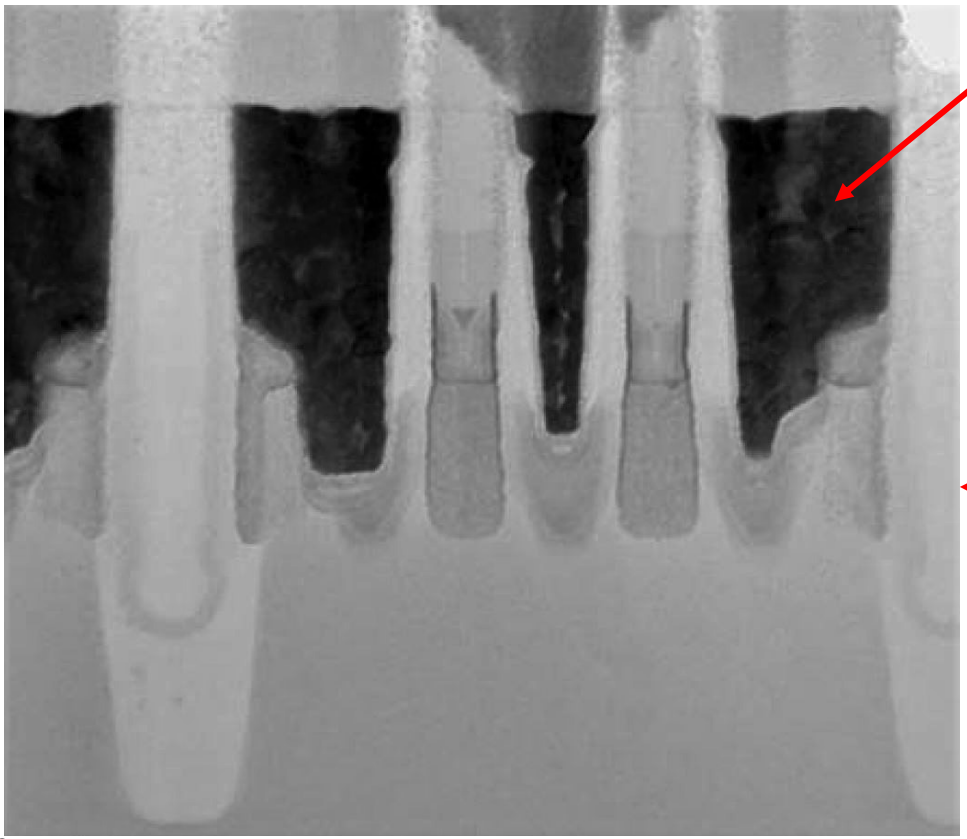
- Partial sigma-etch used for epi cavities
- Minimal gouging into S/D epi
- Work-function materials look similar to 14-nm

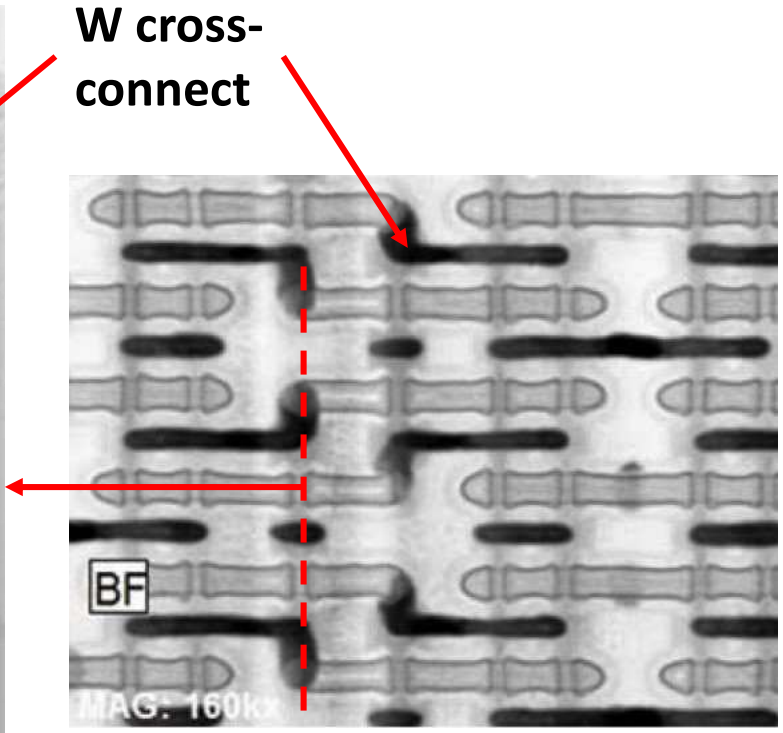


- Contacted gate pitch 68 nm
- Minimum Lg ~25 nm, functional gate height ~45 nm, gate width ~95 nm
- Fin width ~5 nm (pushing the limit!)

Samsung 10LPE (Exynos 8895)

- Thin sample, ~10 nm, shows gate widening on fin sides
- Gates back-etched, capped with SiN, non-self-aligned contacts, heavy gouging into S/D epi
- Contacts still not self-aligned, gate cap used

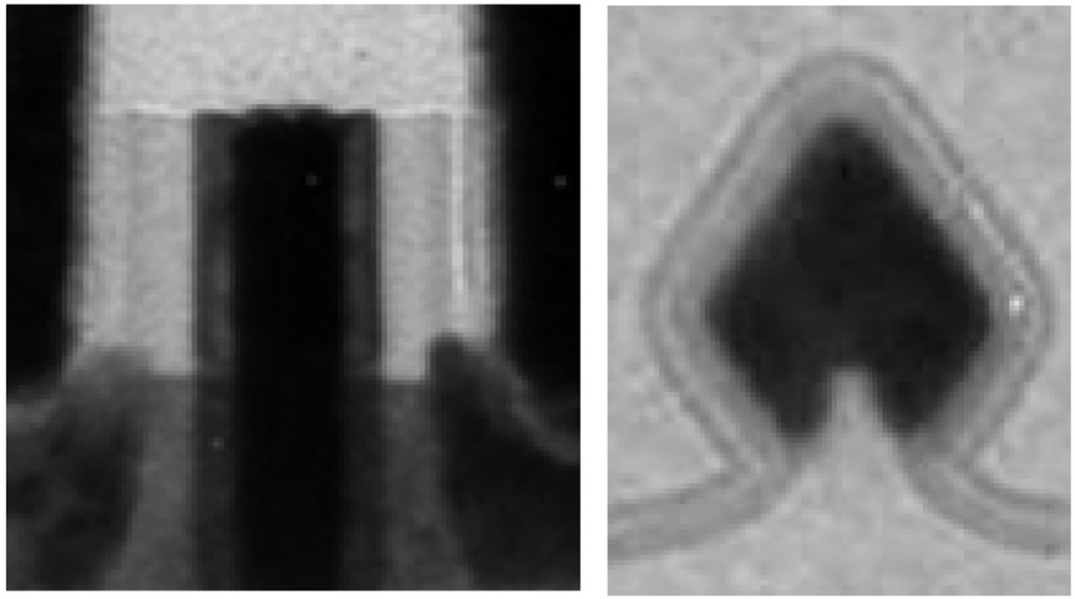




Source: MSSCorps

GLOBALFOUNDRIES 14HP Announcement

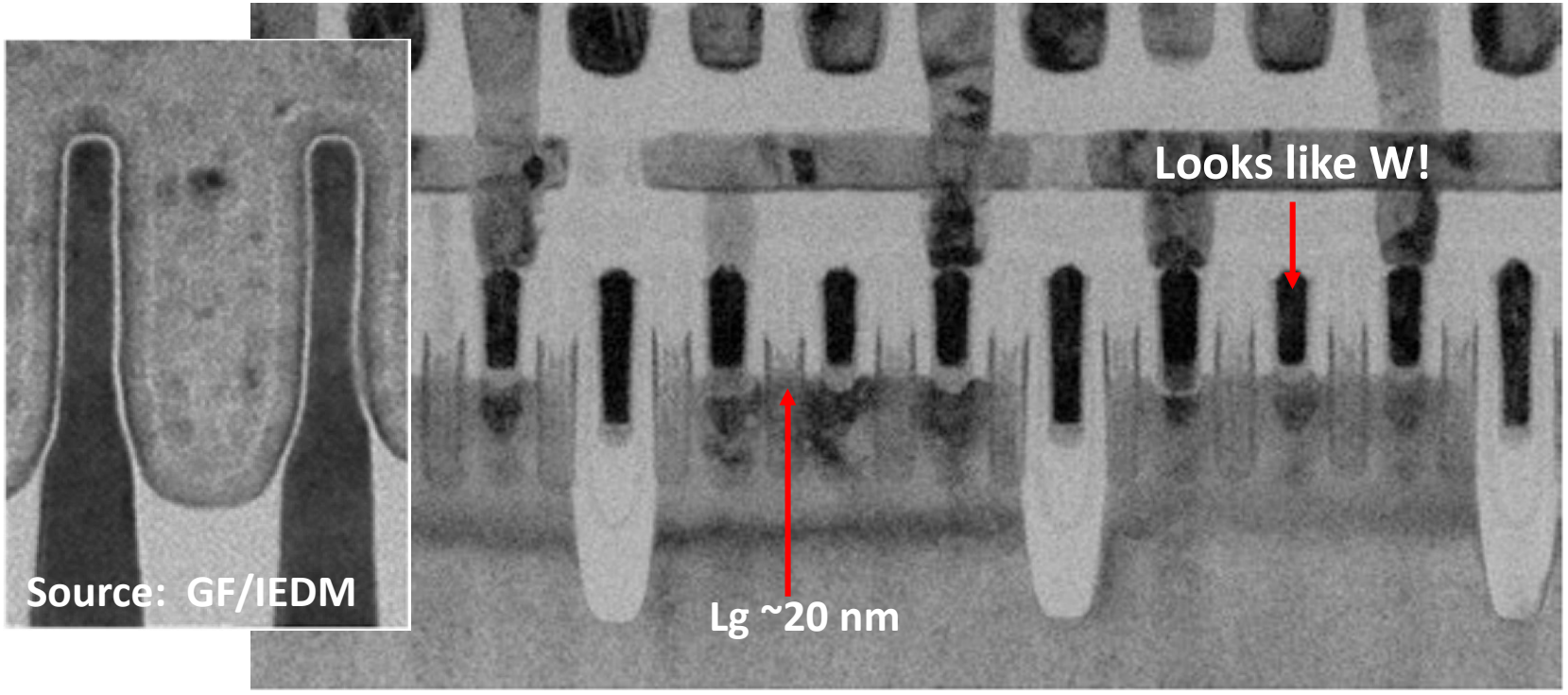
- "GLOBALFOUNDRIES Delivers Custom 14nm FinFET Technology for IBM Systems"
- IEDM 14 paper states FP 42 nm, CGP 80 nm, MMP 64 nm, dual-WF NFETs & PFETs
- 15 metal layers (17 in PR), e-DRAM (0.0174um^2 cell)



Source: IBM/IEDM

GLOBALFOUNDRIES 7 nm Announcement

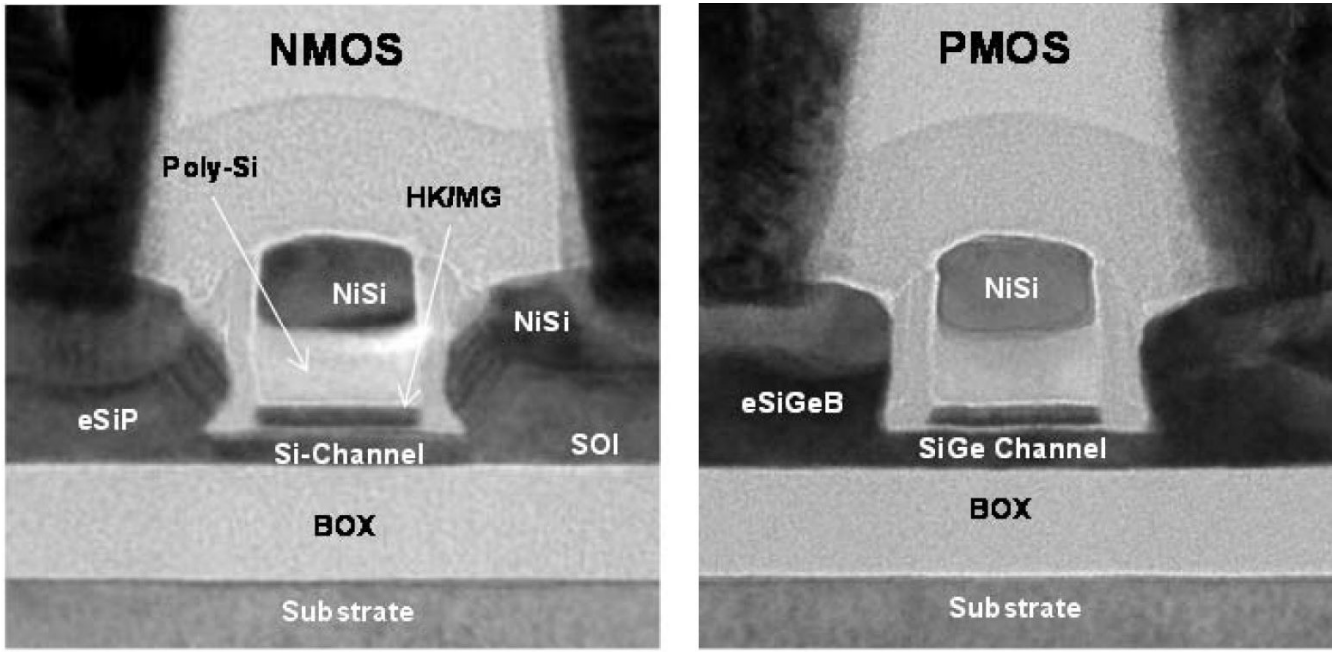
- IEDM 2017 paper states FP 30 nm, CGP 56 nm, MMP 40 nm, quad-WF NFETs & PFETs
- Active fin height ~41 nm, width ~6 nm, gate width ~ 88 nm
- Co contacts, up to 17 metal layers



Source: GF 7-nm product brief

GLOBALFOUNDRIES 22FDX (IEDM 2016)

- If SOI layer ~6 nm, BOX ~18 nm thick, CGP ~90 nm, L_g ~27 nm (20, 24, 28 nm offered)
- Raised in-situ-doped S/D epi, SiGe channel in PMOS, low-k sidewall spacer, four Vts
- Dual-patterned M1/M2



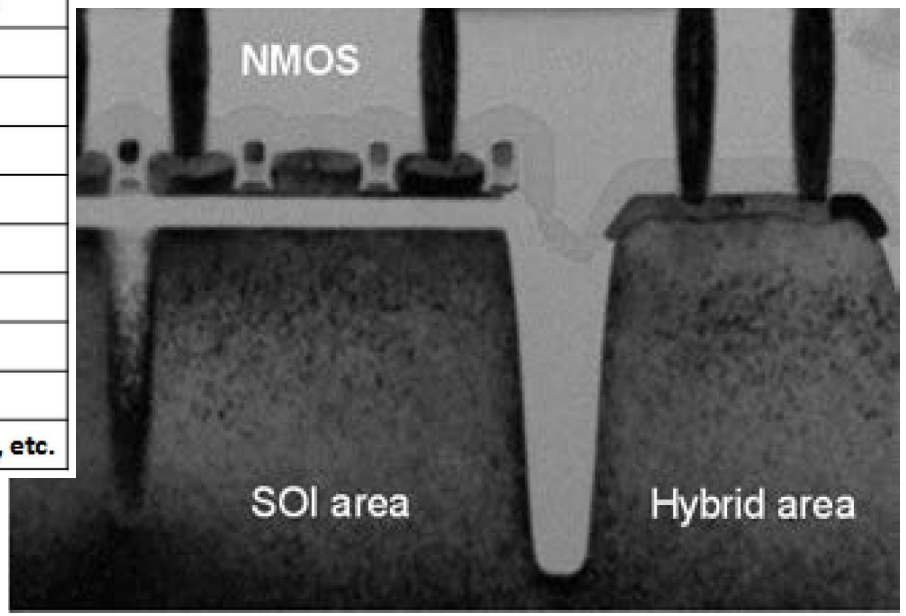
Source: GF/IEDM

GLOBALFOUNDRIES 22FDX (IEDM 2016)

- Hybrid process – devices in SOI or substrate SOI
- Conventional wells and flip-wells (NMOS over N-well, PMOS over P-well) in substrate for back-bias application
- Low-leakage option for PMOS using Si channel

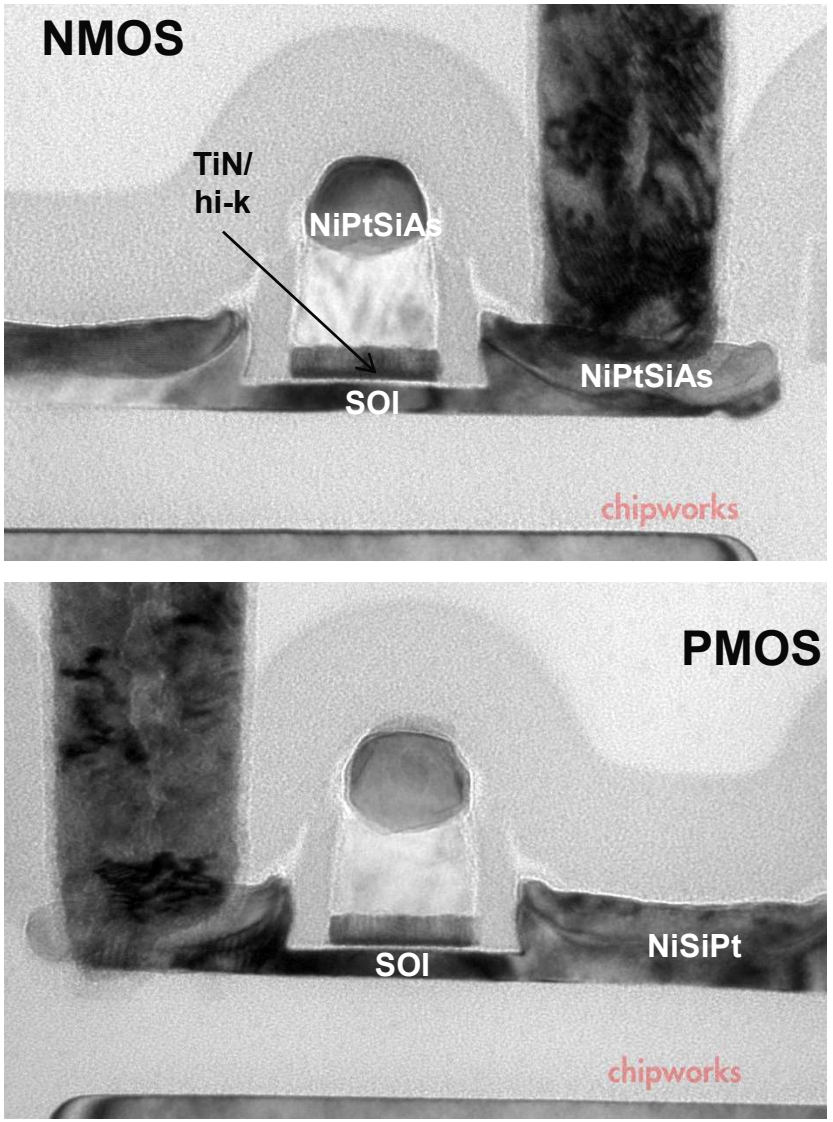
Device	SOI	Substrate	Comment
Core-FET	X		4 V_T flavors for logic + ULL devices
Io-FET	X		2 V_T flavors
LDMOS		X	Supporting 3.3V and 5.0V
Bitcells	X		HD, HC, LV, ULV, ULL, Two-port
Resistors	X	X	Poly, diffusion, well
BJT		X	
Varactors		X	
eFuse		X	
Diodes		X	
RF devices	X	X	Includes also inductors, APMOMs, etc.

Source: GF/IEDM



STMicroelectronics 28-nm FDSOI

- TiN metal layer under polysilicon gate
- CGP ~120 nm
- MOL_g ~32 nm, t_{ox} ~1.0 nm, $t_{hi\text{-}k}$ ~3 nm
- SOI layer ~6 nm, BOX ~26 nm thick
- Raised S/D epi, no Ge in PMOS



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Logic Technology Industry Roadmap

Actual or Estimated Date Production Part Available*

Foundry	2012	2013	2014	2015	2016	2017	2018	2019	2020
tsmc	28HPM		20SoC 28HPC	16FF-T 16FF+	16FFC	10FF 12FFC	7FF	7HPC 7FF+	5nm
SAMSUNG			20LPE	14LPE	14LPP	10LPE	10LPP 11LPP	8LPP	7LPP
GLOBAL FOUNDRIES					14LPP	22FDX	12LP	7LP 12FDX	
intel	22nm	22SoC	14nm	14SoC	14+	14++	10nm 10+	10++	7nm

*risk production and qualification start is typically 1 year ahead

Source: TechInsights

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