JEDEC

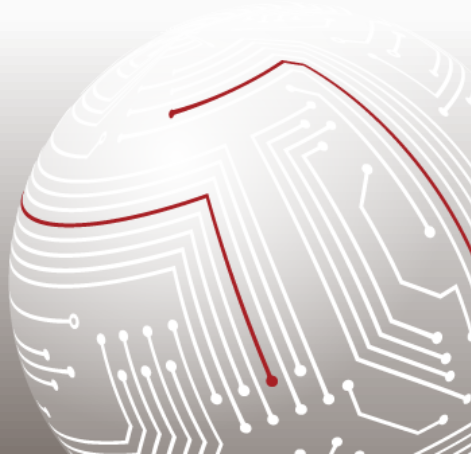
Global Standards for the Microelectronics Industry

LPDDR5 Workshop

Commands & New Features

Alex (Yeongkee) **Chang**

SK hynix



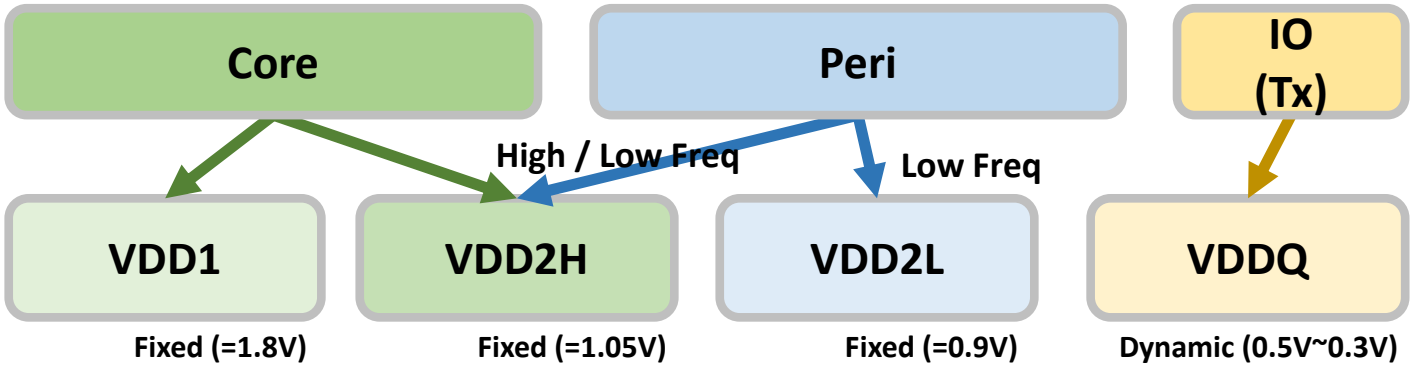
LPDDR5 Power Supplies

- Voltage reduction to improve power consumption
- VDD2H / VDD2L Separation for DVFSC
- Two ranges for VDDQ with DVFSQ operation

	Symbol		Min	Typ	Max	Unit	Remark
Core#1	**VDD1**		1.7	1.8	1.95	V	LPD4X : 1.8V
Core#2	**VDD2**		1.01	1.05	1.12	V	LPD4X : 1.1V
	VDD2L		0.87	0.9	0.97	V	-
IO Power	**VDDQ**	Range 1	0.47	0.5	0.57	V	LPD4X : 0.6V
		Range 2	0.27	0.3	0.37	V	

Power Rails for DVFS Operation

- The low frequency operation still requires VDD2H (1.05V) even with DVFSC on
  - It basically uses VDD2H as a power source for both low and high speed
  - Some circuits change a power source from VDD2H to VDD2L in low speed
- DRAM IO power follows the level of VDDQ input



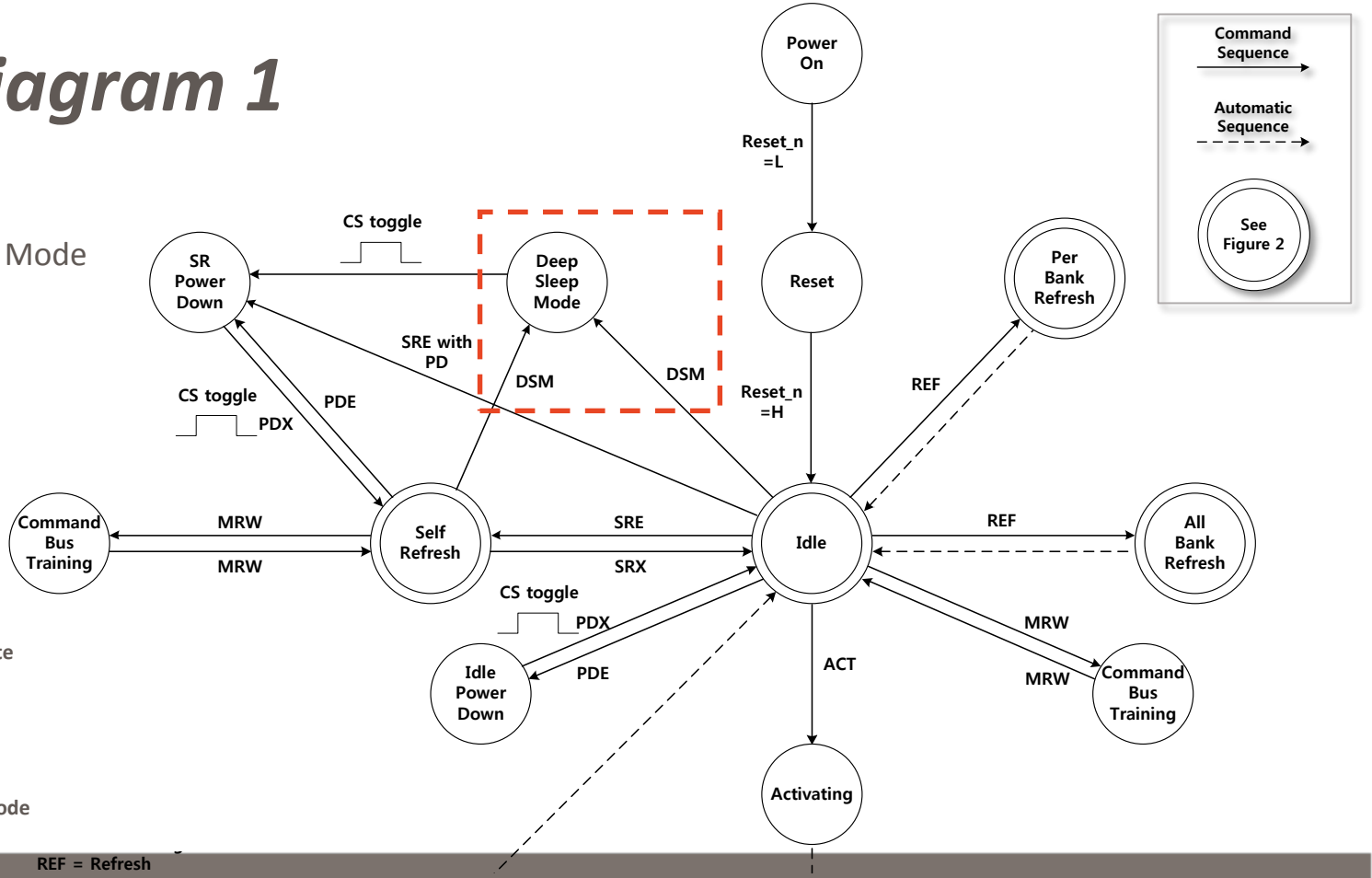
Operating Temperatures

- LPDDR5 expands its market to more applications with the power competitiveness
- Mobile → PC & Client → Mobile Consumer → Graphic → Auto

Condition	Symbol	Min	Max	Unit	Remark – LPD4x
Standard	$T_{oper\_standard}$	-25	85	°C	←
Elevated	$T_{oper\_elevated}$	85	105	°C	←
Automotive Grade 1	$T_{oper\_auto\_grade\ 1}$	-40	125	°C	N/A
Automotive Grade 2	$T_{oper\_auto\_grade\ 2}$	-40	105	°C	N/A
Automotive Grade 3	$T_{oper\_auto\_grade\ 3}$	-40	85	°C	N/A

State Diagram 1

- New State
  - Deep Sleep Mode

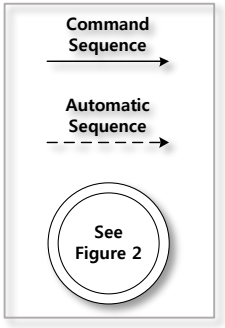


- ACT = Activate
- REF = Refresh
- MRR = Mode Register Read
- MRW = Mode Register Write
- SRE = Enter Self Refresh
- SRX = Exit Self Refresh
- PDE = Enter Power Down
- PDX = Exit Power Down
- DSM = Enter Deep Sleep Mode

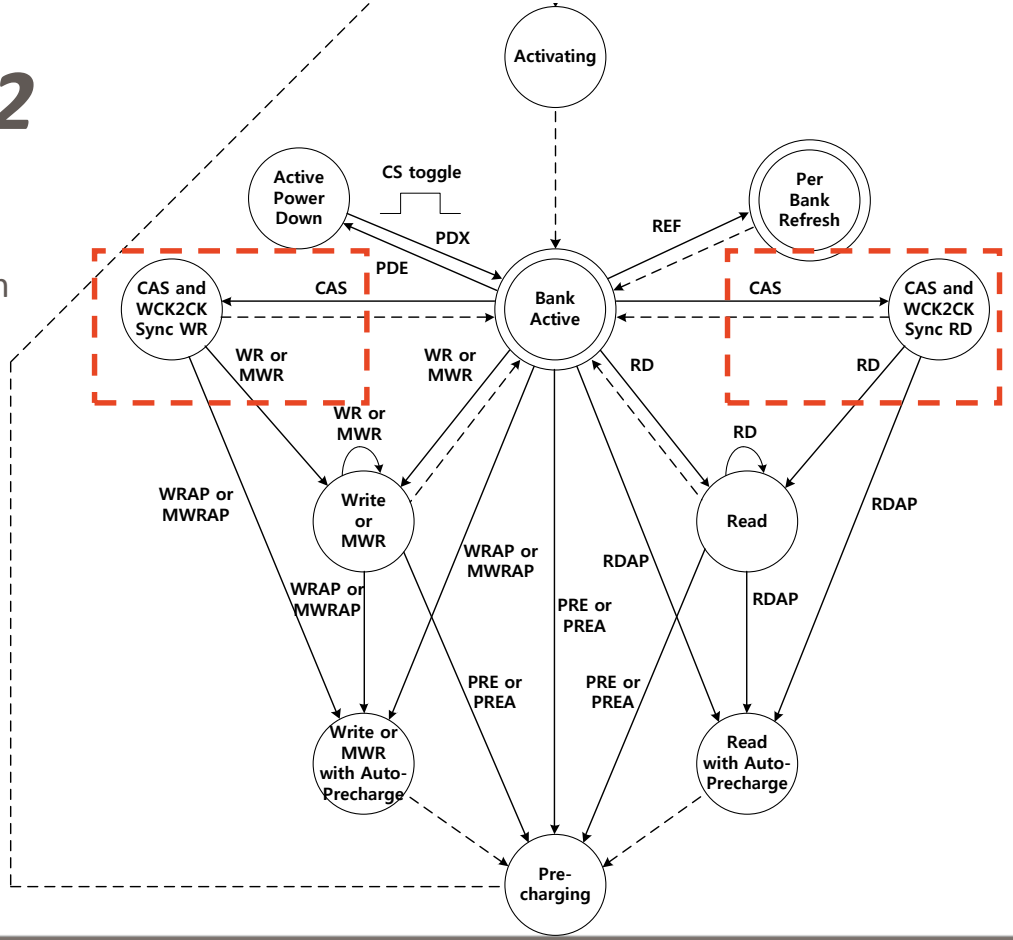
REF = Refresh

State Diagram 2

- New State
  - CAS / WCK2CK Sync Operation

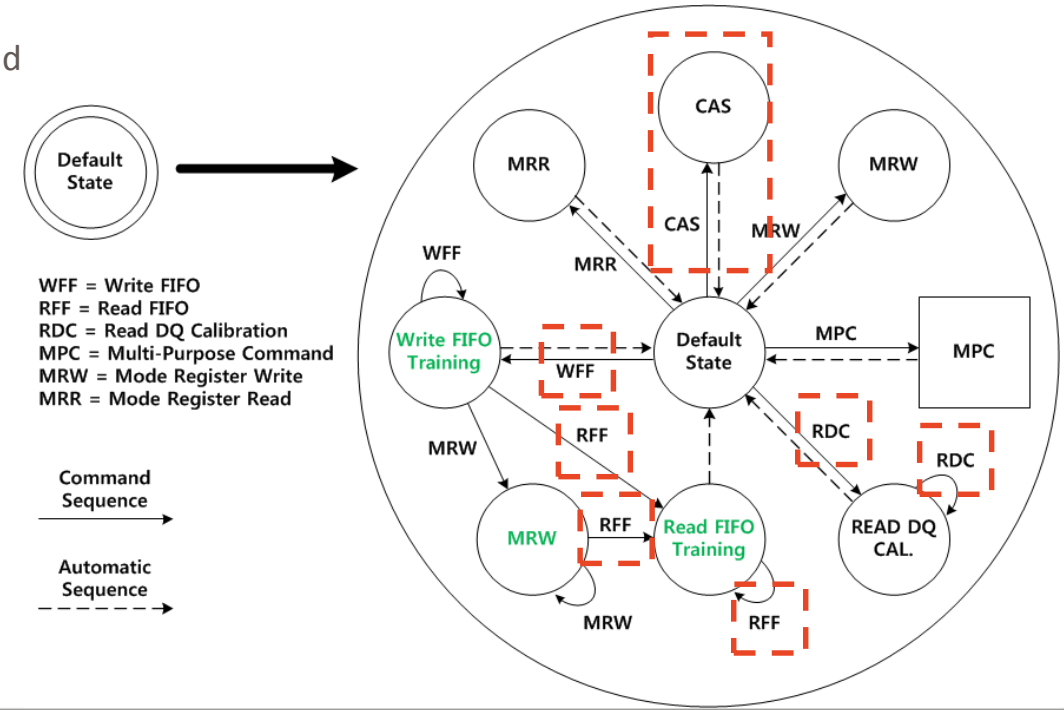


- PRE(A) = Precharge (All)
- WR (AP) = Write (w/ Auto Precharge)
- MWR(AP) = Mask Write (w/ Auto Precharge)
- RD(AP) = Read (w/ Auto Precharge)
- REF = Refresh



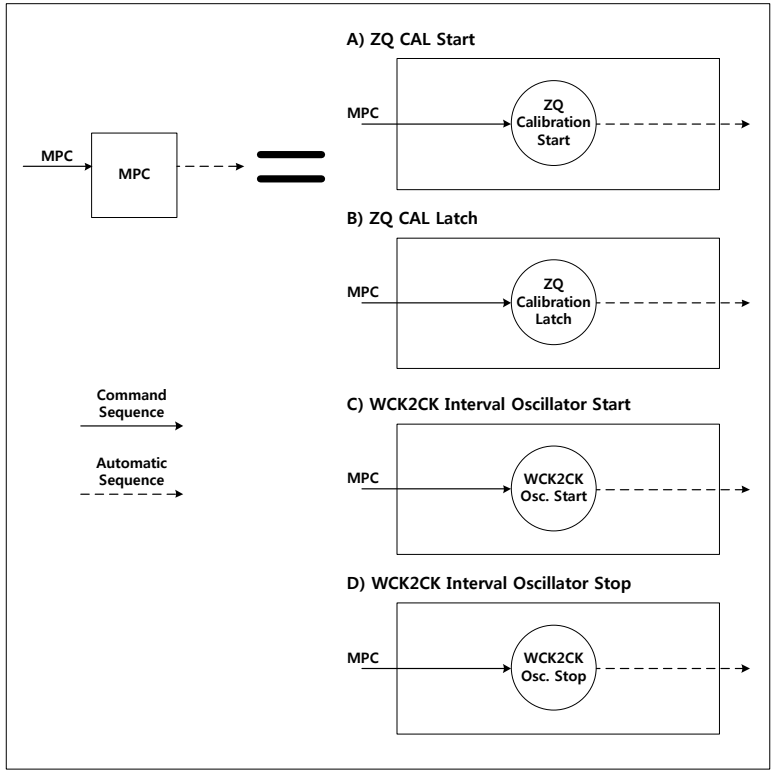
State Diagram 3

- New State
  - WFF / RFF / RDC defined as command



State Diagram 4

- Still use MPC (Multi Purpose Command)
  - ZQ Calibration Start / Latch
  - WCK2CK Interval Oscillator Start / Stop
  - ~~Read FIFO / Write FIFO / RDC (not defined in MPC)~~



Command Truth Table

- All Commands defined in the table are dependent on Bank Organization
  - Bank organization is programmed by MR3 OP[4:3]

Table 52 - MR3 Definition

Function	Register Type	Operand	Data	Notes
PDDS (Pull-Down Drive Strength)	Write-only	OP[2:0]	000_B: RFU 001_B: RZQ/1 010_B: RZQ/2 011_B: RZQ/3 100_B: RZQ/4 101_B: RZQ/5 110_B: RZQ/6 (default) 111_B: Reserved	1,2,3
BK/BG ORG (Bank/Bank Group Organization)		OP[4:3]	00_B: BG Mode 01_B: 8B Mode 10_B: 16B Mode 11_B: Reserved	2,3,5,6
WLS (Write Latency Set)		OP[5]	0_B: Write Latency Set "A" (default) 1_B: Write Latency Set "B"	2,3
DBI-RD (DBI-Read select)		OP[6]	0_B: Disabled (default) 1_B: Read DBI-DC Enabled	2,3
DBI-WR (DBI-Write select)		OP[7]	0_B: Disabled (default) 1_B: Write DBI-DC Enabled	2,3,4

Command Truth Table

- Commands recognize through both rising & falling edge of clocks (SDR @ CS/ DDR @ CA)
- LPDDR5 doesn't provide CKE, so PDE is issued with a command through CS/CA

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
DES (Deselect)	**Any**	L	X	X	X	X	X	X	X	R1
		X	X	X	X	X	X	X	X	F1
NOP (No Operation)	**Any**	H	L	L	L	L	L	L	L	R1
		X	X	X	X	X	X	X	X	F1
PDE (Power Down Entry)	**Any**	H	L	L	L	L	L	L	H	R1
		L	X	X	X	X	X	X	X	**R2**

Command Truth Table

- All commands are composed of 2 tick combinations
- Activate-1 command must be followed by ACTIVATE-2 command

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
ACT-1 (ACTIVATE-1)	**Any**	H	H	H	H	R14	R15	R16	R17	R1
	BG	X	BA0	BA1	BG0	BG1	R11	R12	R13	F1
	16B		BA0	BA1	BA2	BA3				
	8B		BA0	BA1	BA2	V				
ACT-2 (ACTIVATE-2)	**Any**	H	H	H	L	R7	R8	R9	R10	R1
		X	R0	R1	R2	R3	R4	R5	R6	F1

Command Truth Table

- Precharge and Refresh support both per-bank and all-bank operation as in LPDDR4

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
PRE -Per BK, All BK (PRECHARGE per Bank, All Banks)	**Any**	H	L	L	L	H	H	H	H	R1
	BG	X	BA0	BA1	BG0	BG1	V	V	AB	F1
	16B		BA0	BA1	BA2	BA3				
	8B		BA0	BA1	BA2	V				
REF -Per BK, All BK (REFRESH per Bank, All Banks)	**Any**	H	L	L	L	H	H	H	L	R1
	BG	X	BA0	BA1	BG0	RFM	SB0	V	AB	F1
	16B		BA0	BA1	BA2		SB0	V		
	8B		BA0	BA1	BA2		V	SB1		

Command Truth Table

- WRITE32 command is NOT allowed in 8 bank mode
  - WRITE : BL16 @ BG & 16BK mode, BL32 @ 8BK mode
  - WRITE 32 : BL32 @ BG & 16BK mode, Not allowed in 8BK mode

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
	Any	H	L	H	H	C0	C3	C4	C5	R1
WRITE (WR16 or WR)	**BG**	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1
	16B		BA0	BA1	BA2	BA3				
	8B		BA0	BA1	BA2	V				
WRITE32 (WR32)	**BG/16B**	H	L	L	H	L	C3	C4	C5	R1
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1
	16B		BA0	BA1	BA2	BA3				

Command Truth Table

- READ32 command is NOT allowed in 8 bank mode
  - READ: BL16 @ BG & 16BK mode, BL32 @ 8BK mode
  - READ 32 : BL32 @ BG & 16BK mode, Not allowed in 8BK mode

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
READ (RD16 or RD)	**Any**	H	H	L	L	C0	C3	C4	C5	R1
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1
	16B		BA0	BA1	BA2	BA3				
	8B		BA0	BA1	BA2	V				
READ32 (RD32)	**BG/16B**	H	H	L	H	C0	C3	C4	C5	R1
	BG	X	BA0	BA1	BG0	BG1	C1	C2	AP	F1
	16B		BA0	BA1	BA2	BA3				

Command Truth Table

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS	R1
		X	DC0	DC1	DC2	DC3	WRX	V	B3	F1

BL / n Definition

- BL/n indicates “effective” burst length and tCCD(min)
  - BL/n_min = minimum burst data transfer time in DQ bus
  - BL/n_max = required column array cycle time to allow next column array cycle

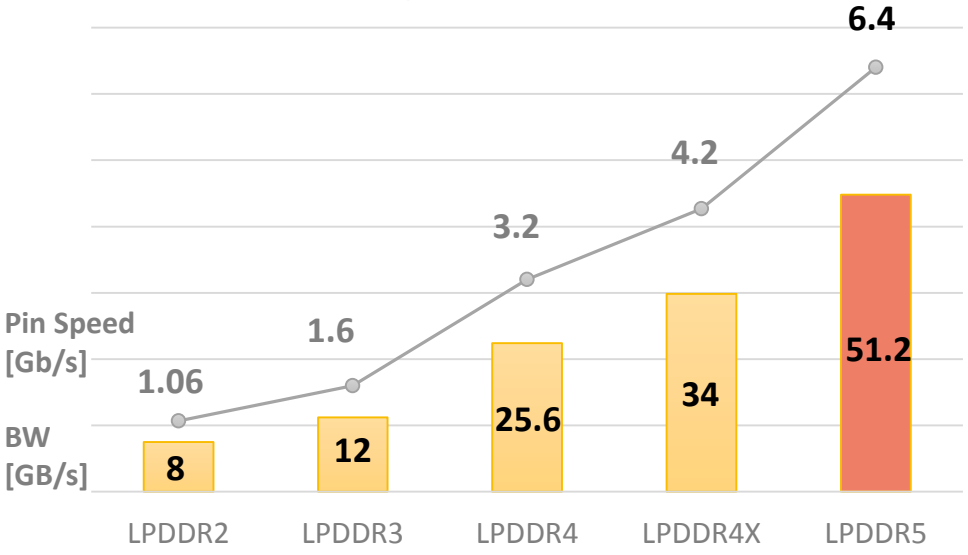
WCK:CK Ratio	Bank ORG	Bank-to-Bank Constraints	WCK Frequency	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
2:1	16B Mode	Any Bank to Bank	≤ 1600MHz	BL16	4*tCK (BL/4)	4*tCK (BL/4)	4*tCK (BL/4)
				BL32	8*tCK (BL/4)	8*tCK (BL/4)	8*tCK (BL/4)
	8B Mode	Any Bank to Bank	≤ 1600MHz	BL32	8*tCK (BL/4)	8*tCK (BL/4)	8*tCK (BL/4)
		MRR, WFF, RFF, RDC	≤ 1600MHz	BL16	8*tCK (BL/2)	8*tCK (BL/2)	8*tCK (BL/2)

BL / n Definition

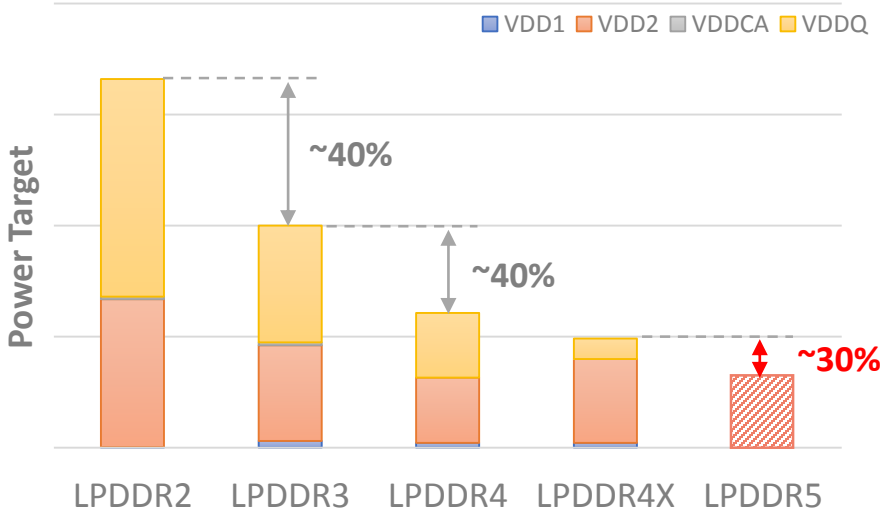
WCK:CK Ratio	Bank ORG	Bank-to-Bank Constraints	WCK Frequency	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
4:1	16B Mode	Any Bank to Bank	≤ 1600MHz	BL16	2*tCK (BL/8)	2*tCK (BL/8)	2*tCK (BL/8)
				BL32	4*tCK (BL/8)	4*tCK (BL/8)	4*tCK (BL/8)
	BG Mode	Same BG	> 1600MHz	BL16	4*tCK (2*BL/8)	2*tCK (BL/8)	4*tCK (2*BL/8)
		Different BG			2*tCK (BL/8)		
		Same BG		BL32	8*tCK (2*BL/8)	6*tCK (1.5*BL/8)	8*tCK (2*BL/8)
		Different BG			2*tCK (0.5*BL/8)		
	8B Mode	Any Bank to Bank	Any Frequency	BL32	4*tCK (BL/8)	4*tCK (BL/8)	4*tCK (BL/8)
		MRR, WFF, RFF, RDC	Any Frequency	BL16	4*tCK (BL/4)	4*tCK (BL/4)	4*tCK (BL/4)

New Features

Speed Trend



Power Trend



New Features – Power

1) Data Copy

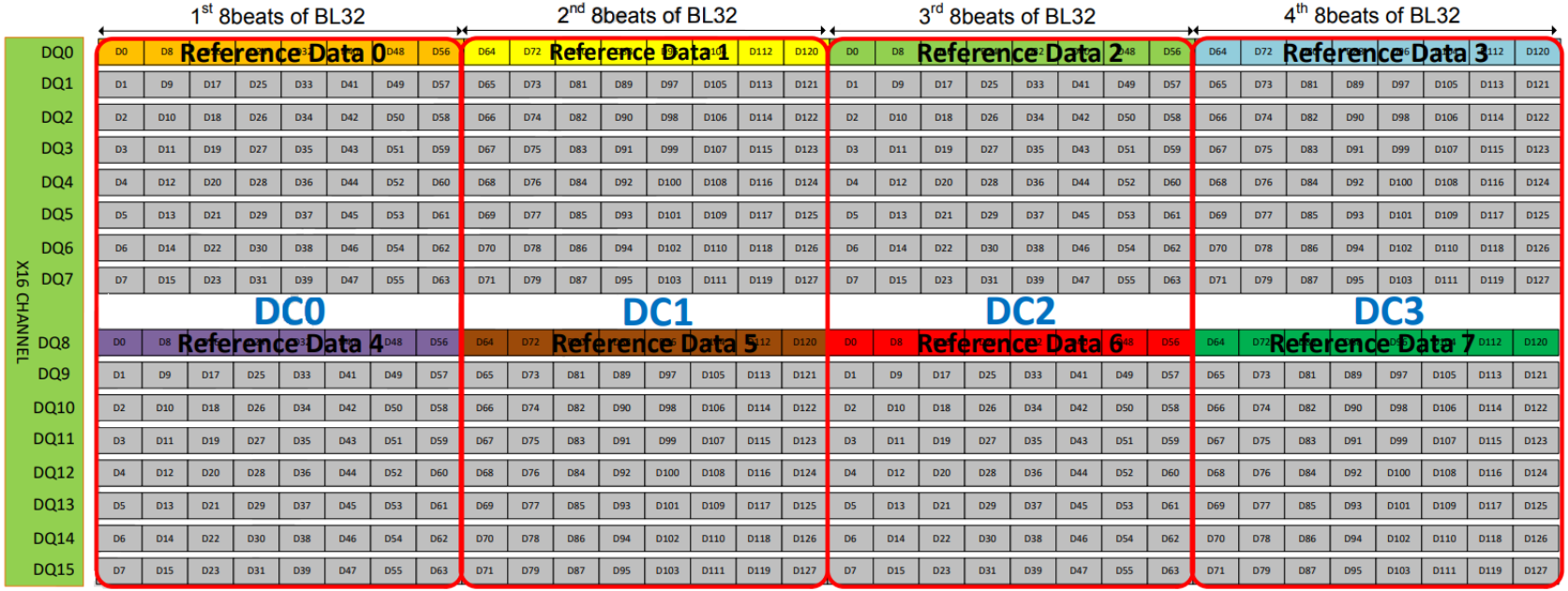
- Provides an opportunity for data burst power reduction – esp. in high BW usage cases – by exploiting data repeatability

- Whenever data pattern is repeated over 8-byte data, only one DQ (per DQ byte) is utilized, hence enabling power reduction
  - only reference data is transferred through the DQ and copied internally
  - 8 byte of data copy granularity

- Applicable to both Write and Read operation
  - Data copy hit/miss information indicated by DC0-DC3 operands in CAS for Write;
  - by 1st and 9th beat of DM burst for Read

New Features – Power

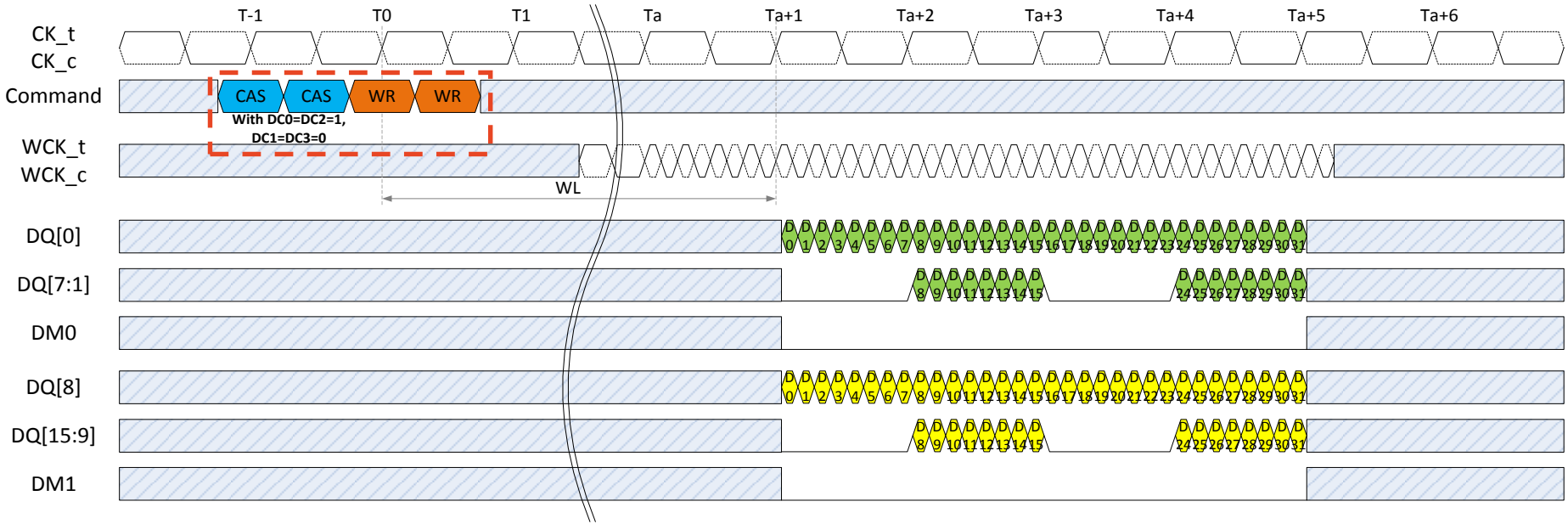
1) Data Copy



Data Copy Granularity and Reference Data Configuration in BL 32

New Features – Power

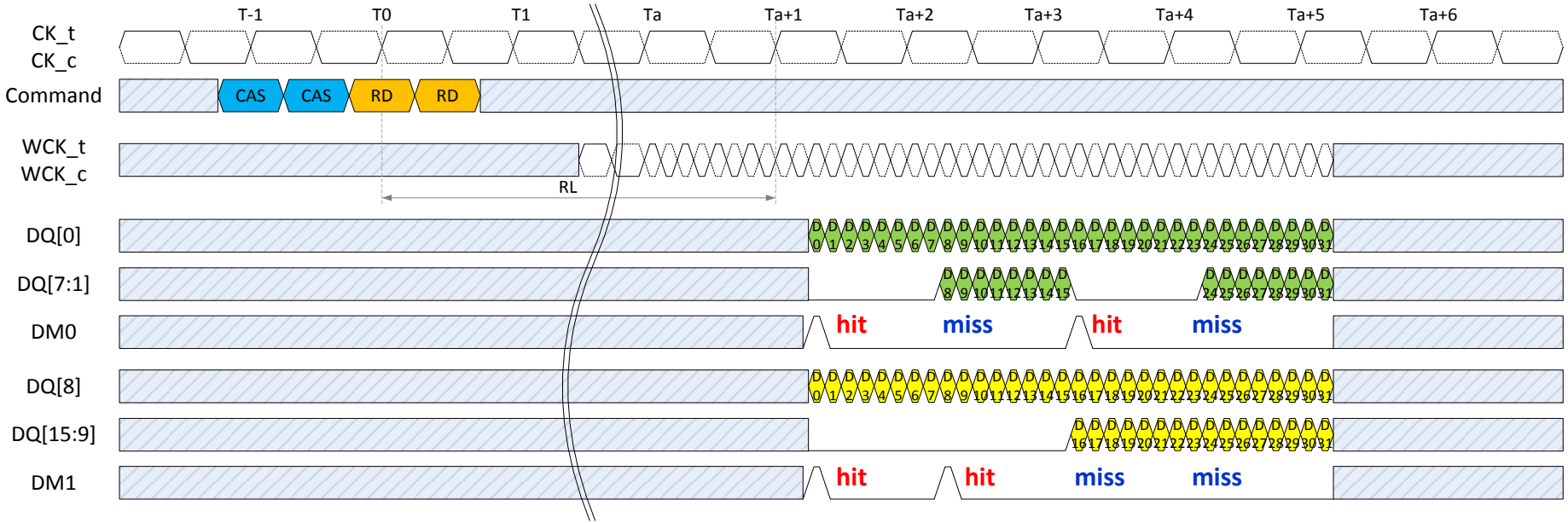
1) Data Copy



Write Data Copy Operation

New Features – Power

1) Data Copy



Read Data Copy Operation

New Features – Power

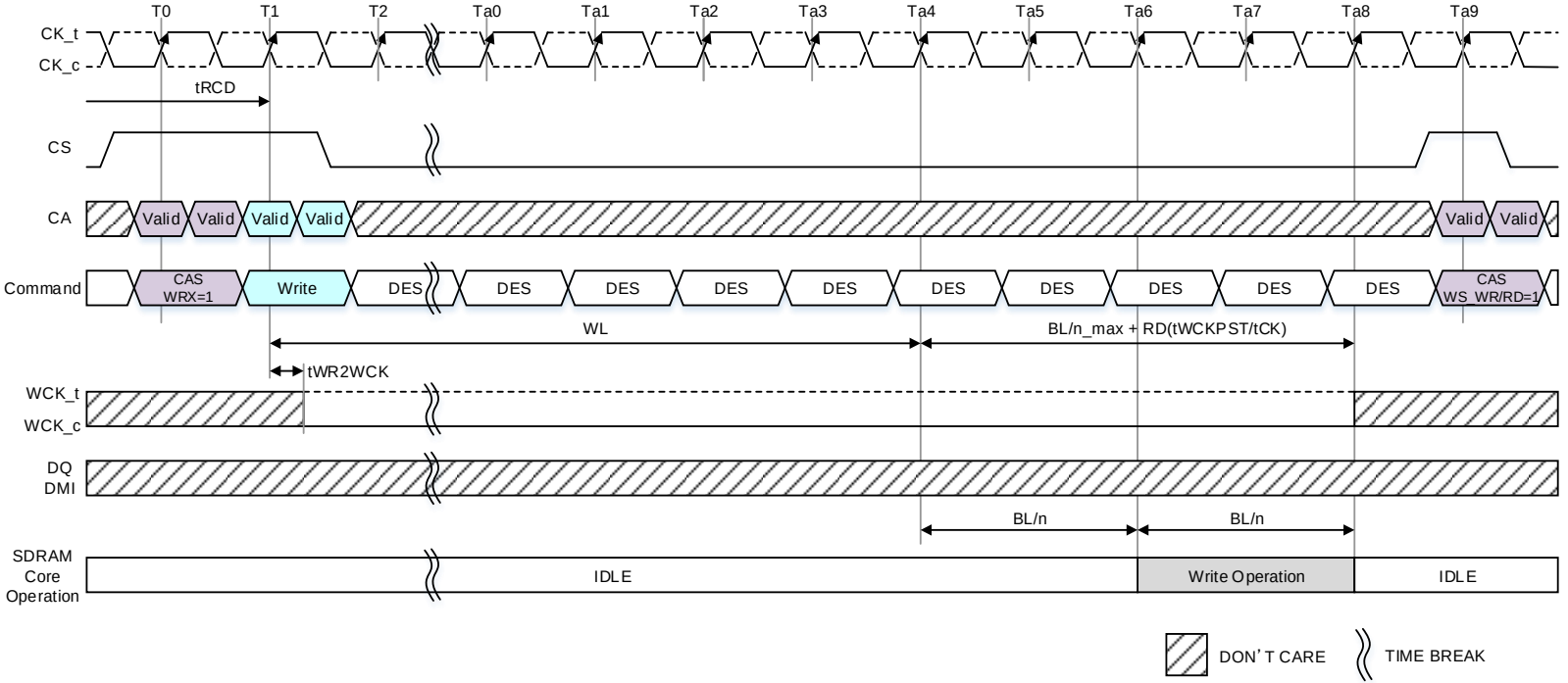
2) Write X

- Reduces power in write operation by exploiting data repeatability
  - Certain data values (e.g. Zero) appear frequently than “average”
- During Write X, data bus + WCK are not utilized
  - WRX, WXSA, WXSB in CAS determine data pattern on a byte level (e.g. WXSA = H → DQ[7:0] all 1’s)
- Benefits:
  - Saves power as data bus is not activated
  - Saves bus BW in multi-rank systems (other ranks can use DQ bus during Write X)

SDRAM Command	SDR	DDR							CK_t
	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	H	L	L	H	H	V	V	V	R1
	X	DC0=0	DC1=0	DC2=0	DC3=0	WRX	V	Xfunc = H or L	F1

New Features – Power

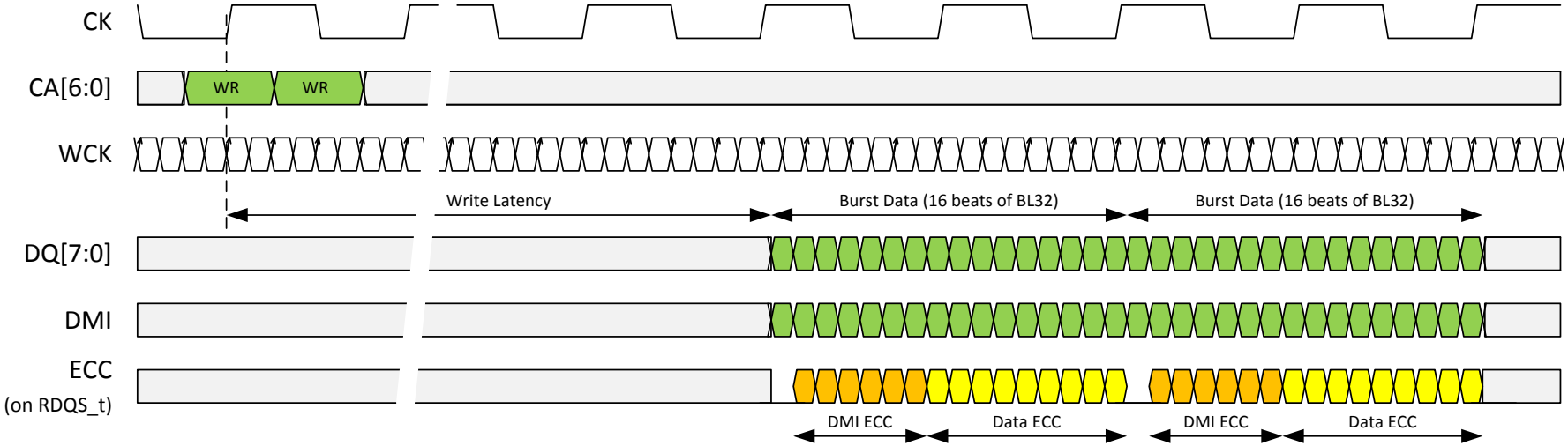
2) Write X



New Features – Channel

1) Link ECC

- To overcome the increase in BER per DQ, LPDDR5 supports Link ECC to correct bit error through the channel

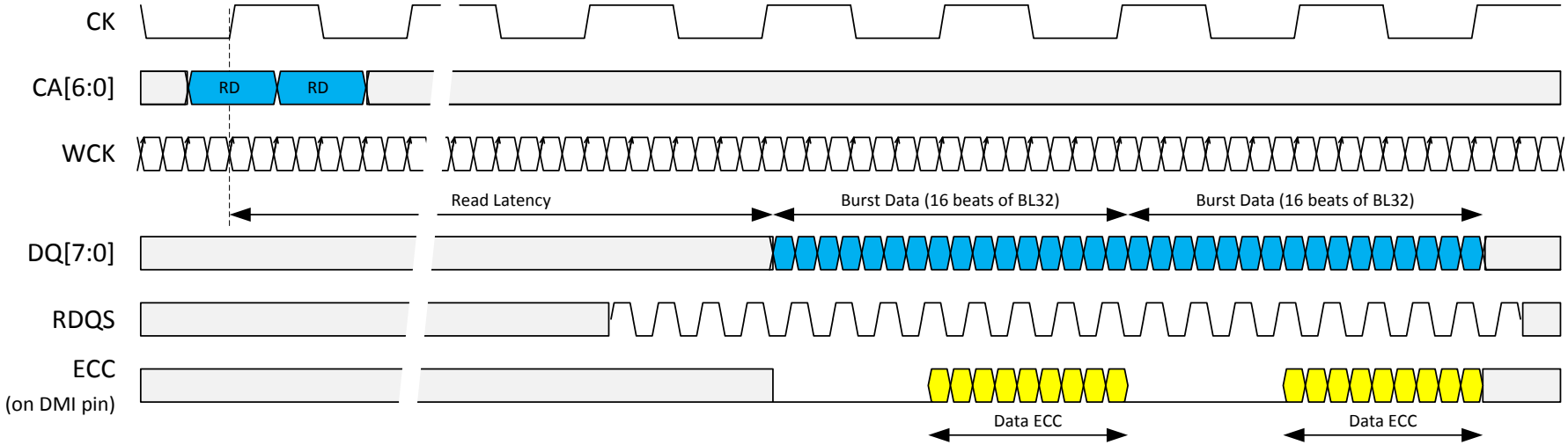


Write with ECC Transfer

New Features – Channel

1) Link ECC

- To overcome the increase in BER per DQ, LPDDR5 supports Link ECC to correct bit error through the channel



Read with ECC Transfer

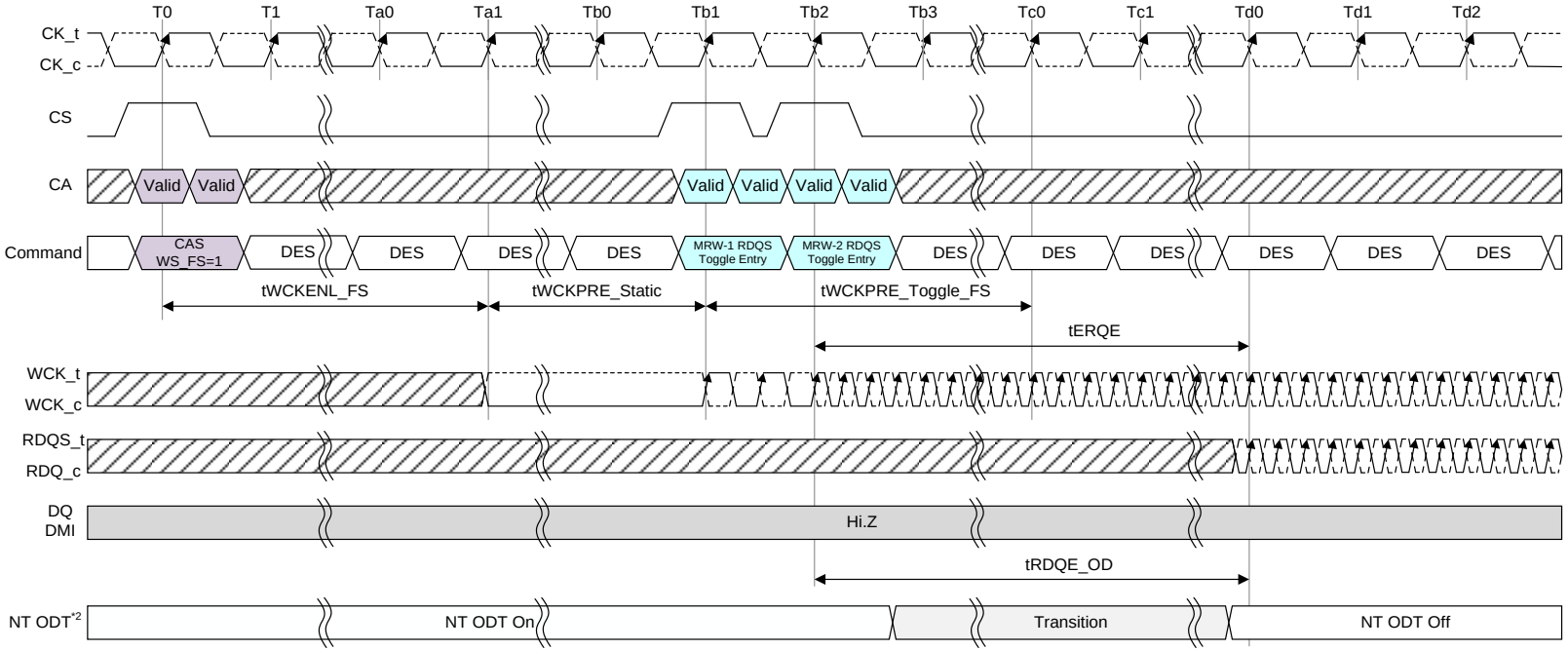
New Features – Channel

2) RDQS toggle

- RDQS toggle mode outputs continuous toggle pattern on RDQS pin
- Entry into and exit from the mode is initiated by programming MR46 OP[1]
  - CAS WS_FS must be issued before MRW command for entry
- RDQS_t/_c behavior follows the definition in MR20 OP[1:0]
  - Disabled, single-ended, differential
- Restrictions on operation during this mode
  - WCK must be toggled for the duration of the mode
  - Change in MRs concerned with output control not allowed

New Features – Channel

2) RDQS toggle



Entry Timing

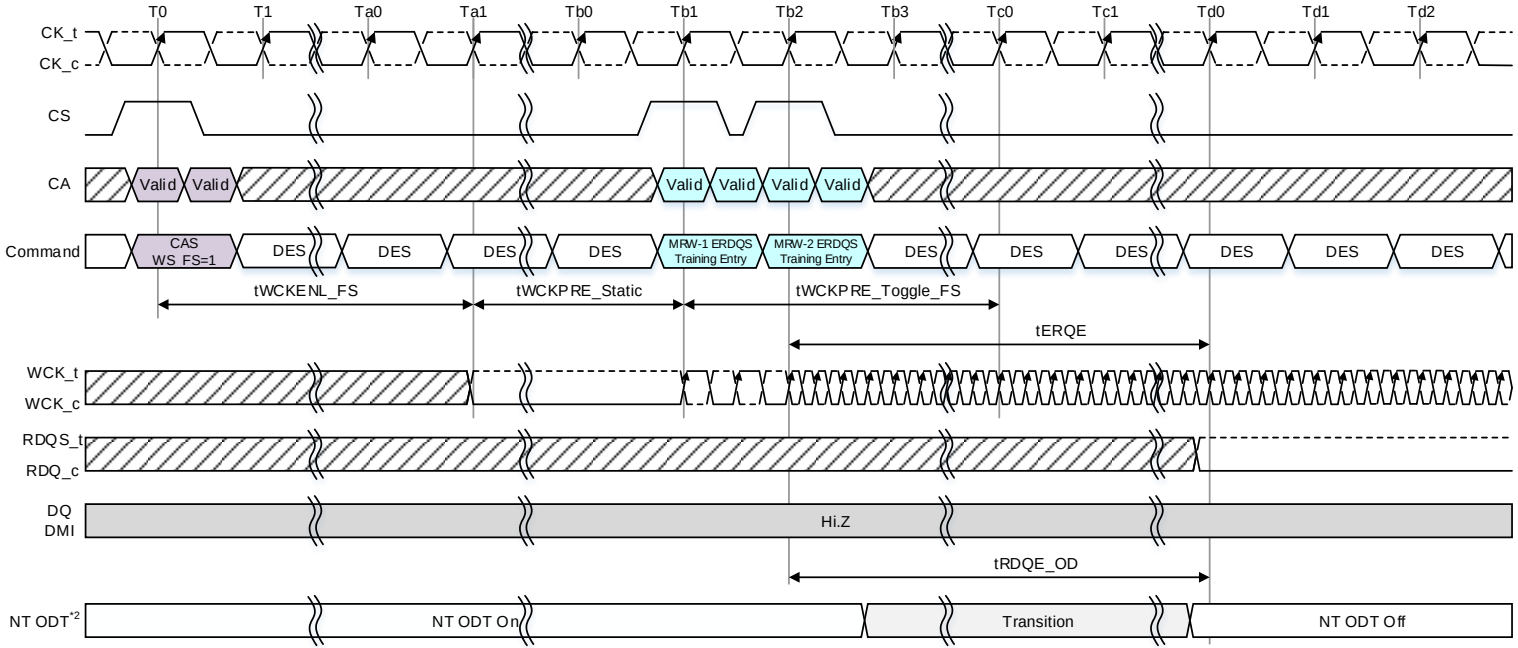
New Features – Channel

3) Enhanced RDQS Training

- Enhanced RDQS training mode keeps RDQS in low-Z state
  - RDQS_t is driven LOW and RDQS_c HIGH
- Entry into and exit from the mode is initiated by programming MR46 OP[0]
  - CAS WS_FS must be issued before MRW command for entry
- Restrictions on operation during this mode
  - WCK must be toggled for the duration of the mode
  - Change in MRs concerned with output control not allowed
- Enhanced RDQS and RDQS toggle modes are mutually exclusive

New Features – Channel

3) Enhanced RDQS Training



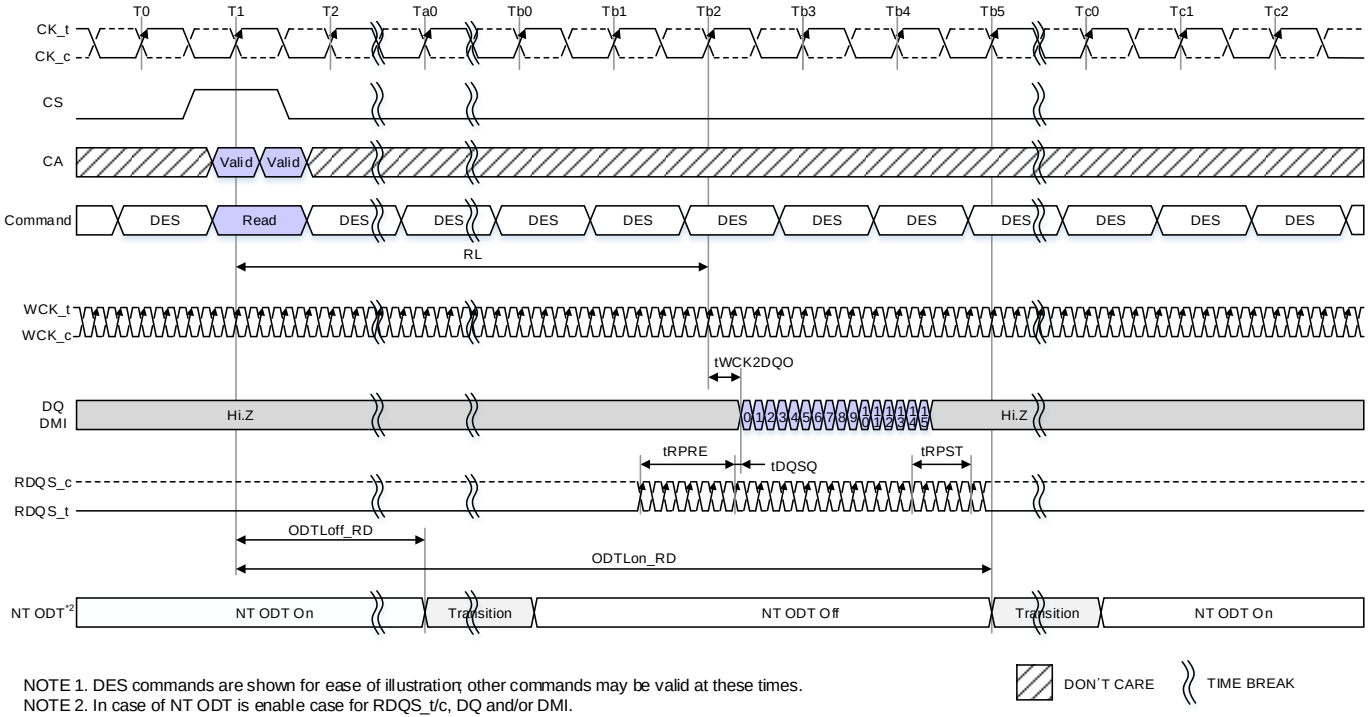
NOTE 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 2. In case of NT ODT is enable case for RDQS_t/c, DQ and/or DMI

DON'T CARE TIME BREAK

Entry Timing

New Features – Channel

3) Enhanced RDQS Training



NOTE 1. DES commands are shown for ease of illustration; other commands may be valid at these times.
NOTE 2. In case of NT ODT is enable case for RDQS_t/c, DQ and/or DMI.

Read During Enhanced RDQS Training

Package Solution Summary

	Ball	Ball pitch	Body Size	Configuration
PoP	496b	0.4mm	14 x 12.4 mm^2	4Ch x64
	436b	0.4mm	14 x 14 mm^2	4Ch x64
Discrete	441b	0.65mm	14 x 14 mm^2	4Ch x64
	315b	0.8(X) / 0.7(Y)	-	2Ch x32
	315b	0.8(X) / 0.7(Y)	-	1Ch x16
uMCP	297b	0.5mm	-	2Ch x32

Package Solution

1) PoP – 496ball

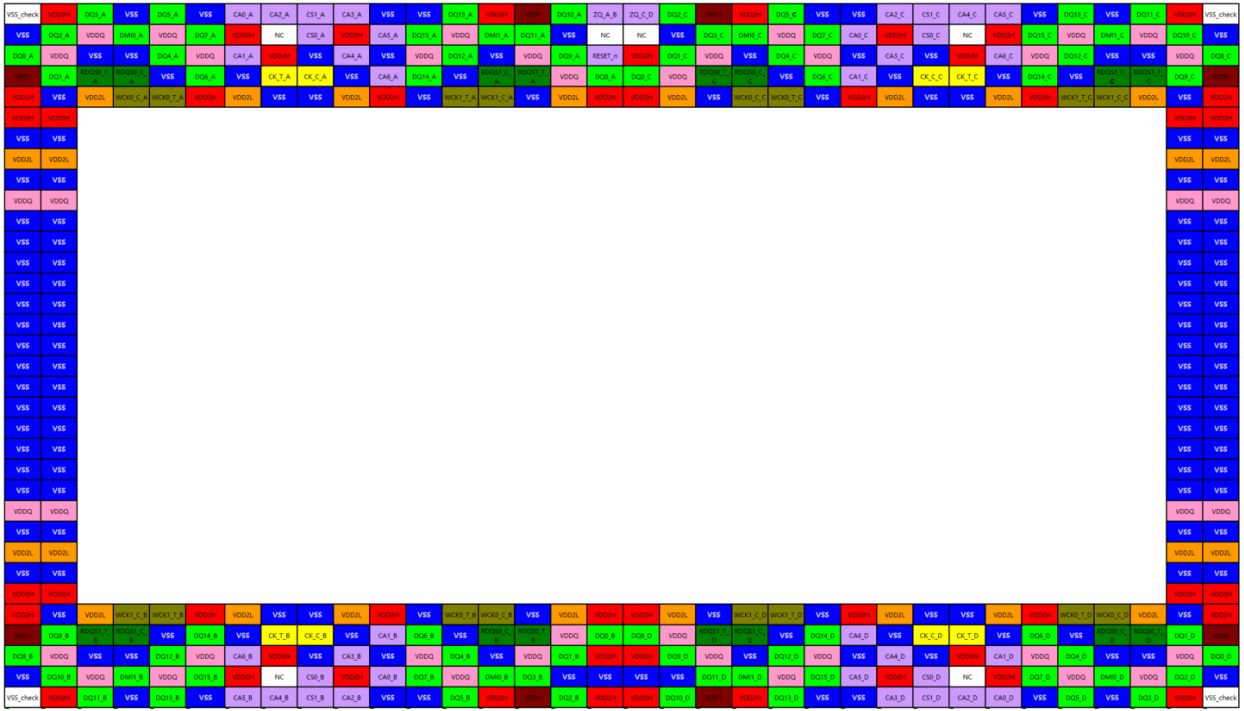
- 4Ch x16 (Total x64)
- Ball Pitch:
  - 0.4 mm
- Body Size:
  - 14.0 mm X 12.4 mm

NC	NC	VDD1	VDD2H	VDD2L	VDDQ	VSS	VDD2H	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD1	VDDQ	VDD2H	VDD2H	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD2H	VDD1	NC	NC
NC	DQ3_A	RDQS0_T_A	VSS	DQ5_A	VSS	CS1_A	VSS	VSS	DQ13_A	VSS	RDQS1_T_A	VSS	DQ9_A	DQ1_C	VSS	RDQS0_T_C	VSS	DQ5_C	VSS	CS1_C	VSS	VSS	DQ13_C	VSS	RDQS1_T_C	DQ11_C	NC
DQ1_A	VSS	RDQS0_C_A	DMI0_A	VDDQ	CA0_A	CS0_A	CA4_A	CA6_A	VDDQ	DMI1_A	RDQS1_C_A	DQ11_A	VDDQ	VDDQ	DQ3_C	RDQS0_C_C	DMI0_C	VDDQ	CA0_C	CS0_C	CA4_C	CA6_C	VDDQ	DMI1_C	RDQS1_C_C	VSS	DQ9_C
VDDQ	DQ2_A	VDDQ	VSS	DQ6_A	VSS	CA2_A	CA3_A	VSS	DQ14_A	VSS	VDDQ	VSS	DQ8_A	DQ0_C	VSS	VDDQ	VSS	DQ6_C	VSS	CA2_C	CA3_C	VSS	DQ14_C	VSS	VDDQ	DQ10_C	VDDQ
DQ0_A	VDDQ	WCK0_C_A	DQ4_A	VDDQ	CA1_A	VDD2H	VDD2L	CA5_A	VDDQ	DQ12_A	WCK1_C_A	DQ10_A	VDDQ	VDDQ	DQ2_C	WCK0_C_C	DQ4_C	VDDQ	CA1_C	VDD2H	VDD2L	CA5_C	VDDQ	DQ12_C	WCK1_C_C	VDDQ	DQ8_C
VSS	VSS	WCK0_T_A	VSS	DQ7_A	VSS	CK_T_A	CK_C_A	VSS	DQ15_A	VSS	WCK1_T_A	VSS	ZQ_A_C	RESET_n	VSS	WCK0_T_C	VSS	DQ7_C	VSS	CK_T_C	CK_C_C	VSS	DQ15_C	VSS	WCK1_T_C	VSS	VSS
VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDD2L	VSS	VDD2H	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H
VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS
VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H
VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDD2L	VSS	VDD2H	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H
VSS	VSS	WCK1_T_B	VSS	DQ15_B	VSS	CK_C_B	CK_T_B	VSS	DQ7_B	VSS	WCK0_T_B	VSS	RFU	ZQ_B_D	VSS	WCK1_T_D	VSS	DQ15_D	VSS	CK_C_D	CK_T_D	VSS	DQ7_D	VSS	WCK0_T_D	VSS	VSS
DQ8_B	VDDQ	WCK1_C_B	DQ12_B	VDDQ	CA5_B	VDD2L	VDD2H	CA1_B	VDDQ	DQ4_B	WCK0_C_B	DQ2_B	VDDQ	VDDQ	DQ10_D	WCK1_C_D	DQ12_D	VDDQ	CA5_D	VDD2L	VDD2H	CA1_D	VDDQ	DQ4_D	WCK0_C_D	VDDQ	DQ0_D
VDDQ	DQ10_B	VDDQ	VSS	DQ14_B	VSS	CA3_B	CA2_B	VSS	DQ6_B	VSS	VDDQ	VSS	DQ0_B	DQ8_D	VSS	VDDQ	VSS	DQ14_D	VSS	CA3_D	CA2_D	VSS	DQ6_D	VSS	VDDQ	DQ2_D	VDDQ
DQ9_B	VSS	RDQS1_C_B	DMI1_B	VDDQ	CA6_B	CA4_B	CS0_B	CA0_B	VDDQ	DMI0_B	RDQS0_C_B	DQ3_B	VDDQ	VDDQ	DQ11_D	RDQS1_C_D	DMI1_D	VDDQ	CA6_D	CA4_D	CS0_D	CA0_D	VDDQ	DMI0_D	RDQS0_C_D	VSS	DQ1_D
NC	DQ11_B	RDQS1_T_B	VSS	DQ13_B	VSS	VSS	CS1_B	VSS	DQ5_B	VSS	RDQS0_T_B	VSS	DQ1_B	DQ9_D	VSS	RDQS1_T_D	VSS	DQ13_D	VSS	VSS	CS1_D	VSS	DQ5_D	VSS	RDQS0_T_D	DQ3_D	NC
NC	NC	VDD1	VDD2H	VDD2L	VDDQ	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD1	VDDQ	VDD2H	VDD2H	VDD2L	VDD2H	VSS	VDDQ	VDD2L	VDD2H	VDD1	NC	NC

Package Solution

2) PoP – 436ball

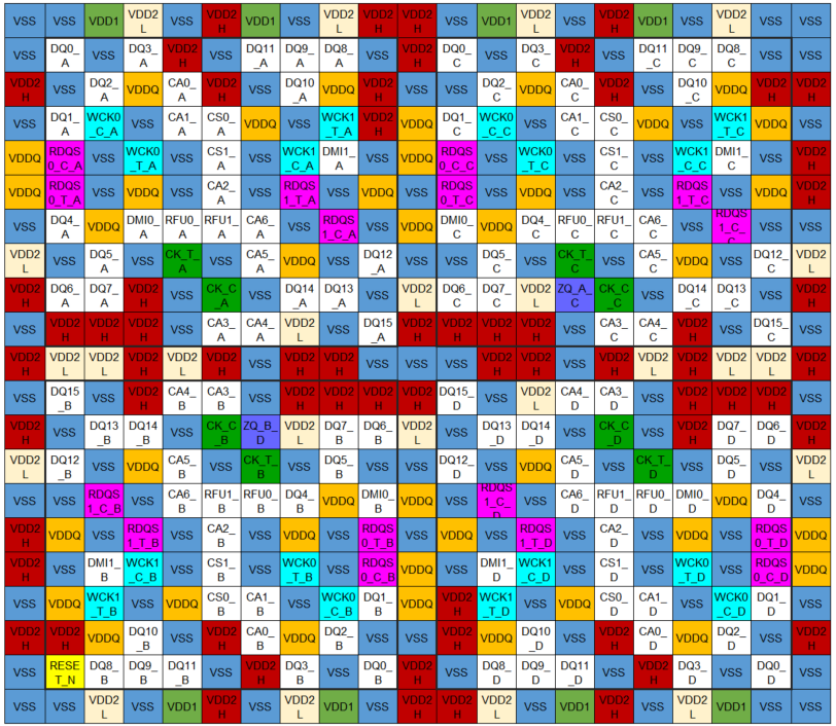
- 4Ch x16 (Total x64)
- Ball Pitch:
  - 0.4 mm
- Body Size:
  - 14.0 mm X 14.0 mm



Package Solution

3) Discrete – 441ball

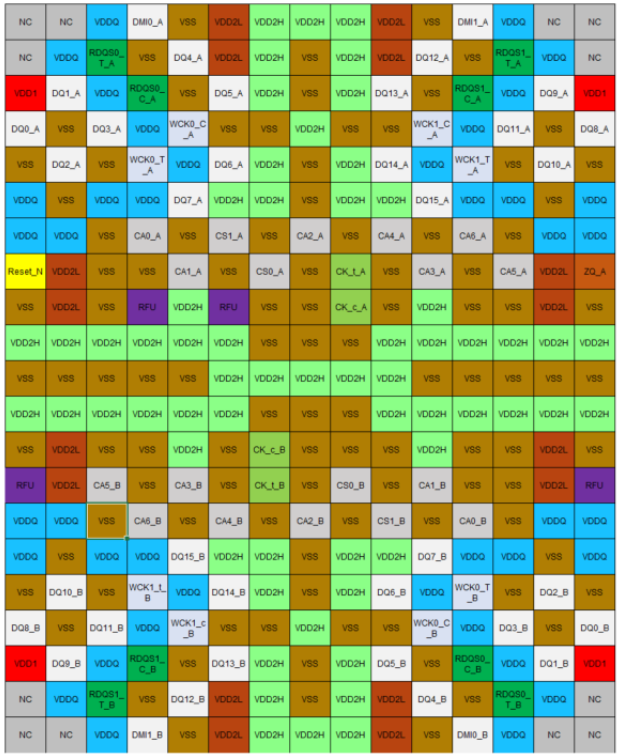
- 4Ch x64
- Ball Pitch:
  - 0.65 mm
- Body Size:
  - 14 mm x 14 mm



Package Solution

4) Discrete – 315ball

- Application:
  - Client & Various Application (like 200b in LPDDR4)
- Ball Pitch
  - 0.8mm(X) , 0.7mm (Y)
- Body Size



Package Solution

5) uMCP – 297ball

- Application:
  - Mobile
- Ball Pitch:
  - 0.5 mm
- Body Size:
  - 11.5 mm X 13.0 mm