



Global Standards for the Microelectronics Industry

LPDDR5 Workshop

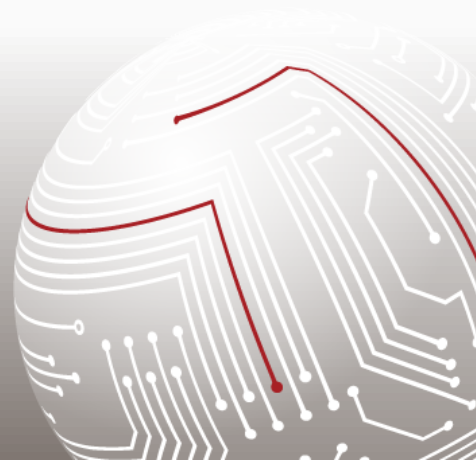
Commands & New Features

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LPDDR5 Workshop

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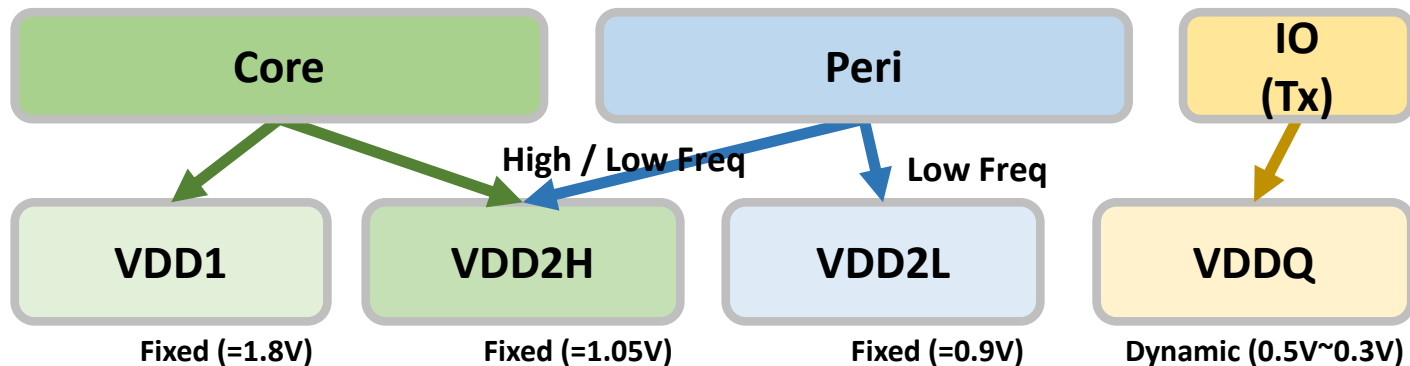
LPDDR5 Power Supplies

- Voltage reduction to improve power consumption
- VDD2H / VDD2L Separation for DVFS
- Two ranges for VDDQ with DVFSQ operation

	Symbol	Min	Typ	Max	Unit	Remark	
Core#1	VDD1	1.7	1.8	1.95	V	LPD4X : 1.8V	
Core#2	VDD2	1.01	1.05	1.12	V	LPD4X : 1.1V	
	VDD2L	0.87	0.9	0.97	V	-	
IO Power	VDDQ	Range 1	0.47	0.5	0.57	V	LPD4X : 0.6V
		Range 2	0.27	0.3	0.37	V	

Power Rails for DVFS Operation

- The low frequency operation still requires VDD2H (1.05V) even with DVFSC on
 - It basically uses VDD2H as a power source for both low and high speed
 - Some circuits change a power source from VDD2H to VDD2L in low speed
- DRAM IO power follows the level of VDDQ input



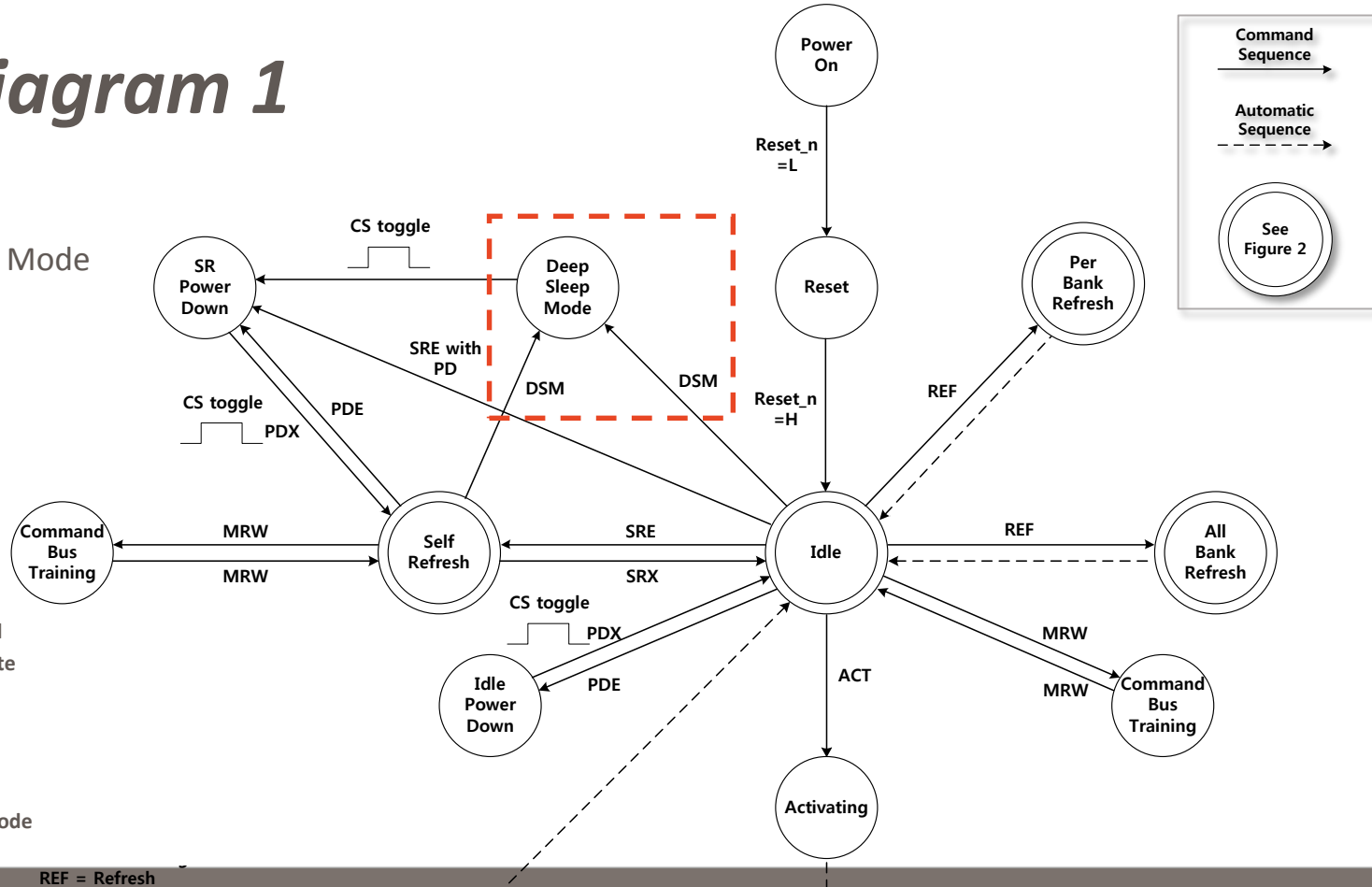
Operating Temperatures

- LPDDR5 expands its market to more applications with the power competitiveness
- Mobile → PC & Client → Mobile Consumer → Graphic → Auto

Condition	Symbol	Min	Max	Unit	Remark – LPD4x
Standard	$T_{\text{oper_standard}}$	-25	85	°C	←
Elevated	$T_{\text{oper_elevated}}$	85	105	°C	←
Automotive Grade 1	$T_{\text{oper_auto_grade 1}}$	-40	125	°C	N/A
Automotive Grade 2	$T_{\text{oper_auto_grade 2}}$	-40	105	°C	N/A
Automotive Grade 3	$T_{\text{oper_auto_grade 3}}$	-40	85	°C	N/A

State Diagram 1

- New State
 - Deep Sleep Mode

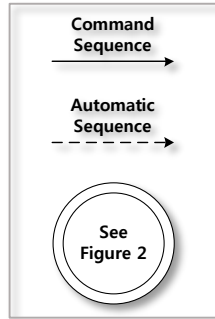


- ACT = Activate
- REF = Refresh
- MRR = Mode Register Read
- MRW = Mode Register Write
- SRE = Enter Self Refresh
- SRX = Exit Self Refresh
- PDE = Enter Power Down
- PDX = Exit Power Down
- DSM = Enter Deep Sleep Mode

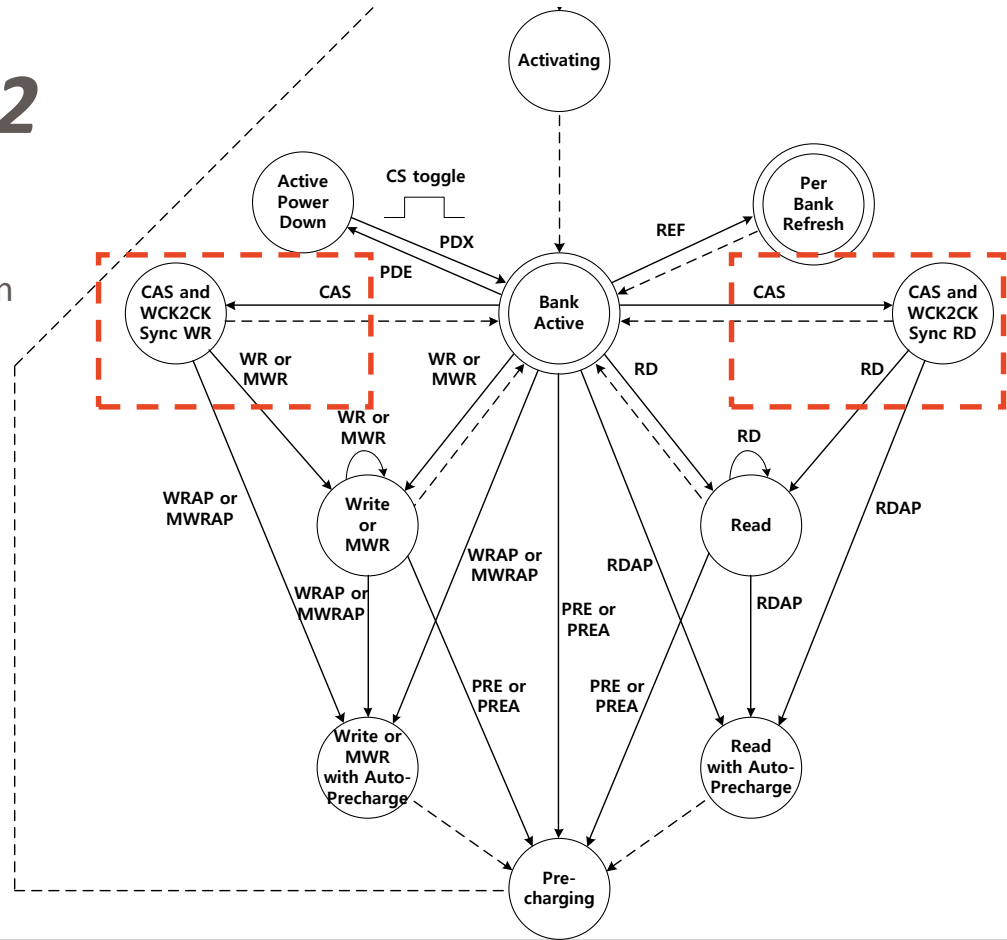
REF = Refresh

State Diagram 2

- New State
 - CAS / WCK2CK Sync Operation

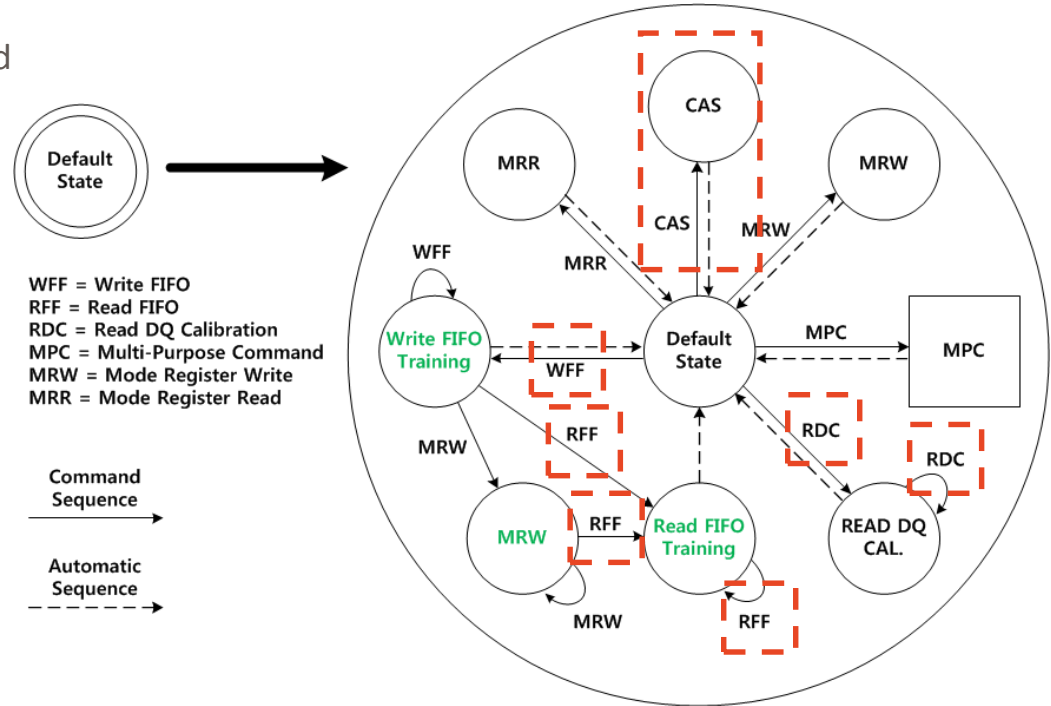


- PRE(A) = Precharge (All)
- WR (AP) = Write (w/ Auto Precharge)
- MWR(AP) = Mask Write (w/ Auto Precharge)
- RD(AP) = Read (w/ Auto Precharge)
- REF = Refresh



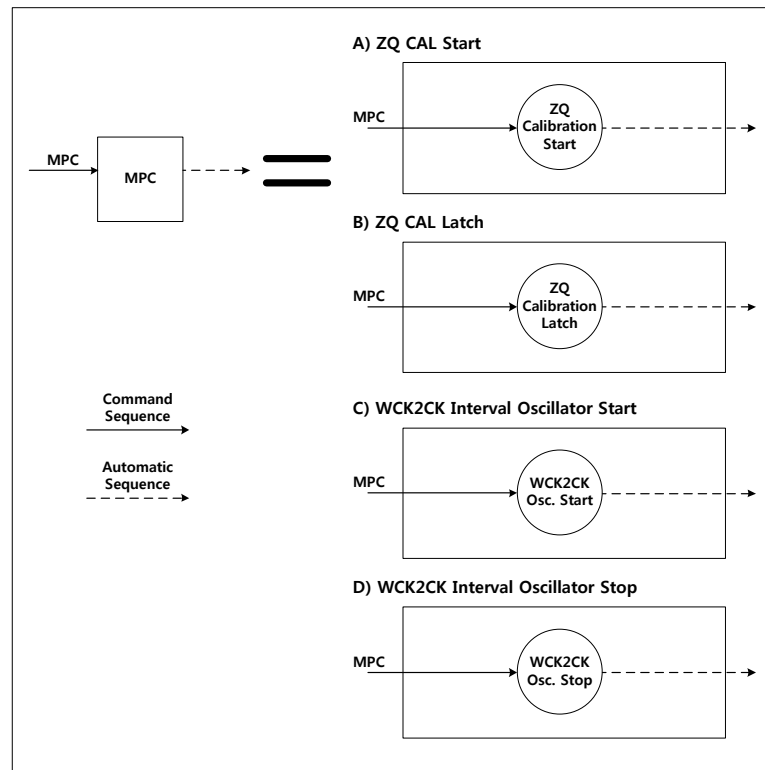
State Diagram 3

- New State
 - WFF / RFF / RDC defined as command



State Diagram 4

- Still use MPC (Multi Purpose Command)
 - ZQ Calibration Start / Latch
 - WCK2CK Interval Oscillator Start / Stop
 - ~~Read FIFO / Write FIFO / RDC (not defined in MPC)~~



Command Truth Table

- All Commands defined in the table are dependent on Bank Organization
 - Bank organization is programmed by MR3 OP[4:3]

Table 52 - MR3 Definition

Function	Register Type	Operand	Data	Notes
PDDS (Pull-Down Drive Strength)	Write-only	OP[2:0]	00 _B : RFU 001 _B : RZQ/1 010 _B : RZQ/2 011 _B : RZQ/3 100 _B : RZQ/4 101 _B : RZQ/5 110 _B : RZQ/6 (default) 111 _B : Reserved	1,2,3
BK/BG ORG (Bank/Bank Group Organization)		OP[4:3]	00 _B : BG Mode 01 _B : 8B Mode 10 _B : 16B Mode 11 _B : Reserved	2,3,5,6
WLS (Write Latency Set)		OP[5]	0 _B : Write Latency Set "A" (default) 1 _B : Write Latency Set "B"	2,3
DBI-RD (DBI-Read select)		OP[6]	0 _B : Disabled (default) 1 _B : Read DBI-DC Enabled	2,3
DBI-WR (DBI-Write select)		OP[7]	0 _B : Disabled (default) 1 _B : Write DBI-DC Enabled	2,3,4

Command Truth Table

- Commands recognize through both rising & falling edge of clocks (SDR @ CS/ DDR @ CA)
- LPDDR5 doesn't provide CKE, so PDE is issued with a command through CS/CA

SDRAM Command	BK ORG	SDR	DDR						CK_t	
		CS	CA0	CA1	CA2	CA3	CA4	CA5		CA6
DES (Deselect)	Any	L	X	X	X	X	X	X	X	R1
		X	X	X	X	X	X	X	X	F1
NOP (No Operation)	Any	H	L	L	L	L	L	L	L	R1
		X	X	X	X	X	X	X	X	F1
PDE (Power Down Entry)	Any	H	L	L	L	L	L	L	H	R1
		L	X	X	X	X	X	X	X	R2

Command Truth Table

- All commands are composed of 2 tick combinations
- Activate-1 command must be followed by ACTIVATE-2 command

SDRAM Command	BK ORG	SDR	DDR						CK _t	
		CS	CA0	CA1	CA2	CA3	CA4	CA5		CA6
ACT-1 (ACTIVATE-1)	Any	H	H	H	H	R14	R15	R16	R17	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	R11	R12	R13	F1
	8B		BA0	BA1	BA2	V				
ACT-2 (ACTIVATE-2)	Any	H	H	H	L	R7	R8	R9	R10	R1
		X	R0	R1	R2	R3	R4	R5	R6	F1

Command Truth Table

- Precharge and Refresh support both per-bank and all-bank operation as in LPDDR4

SDRAM Command	BK ORG	SDR	DDR							CK _t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
PRE -Per BK, All BK (PRECHARGE per Bank, All Banks)	Any	H	L	L	L	H	H	H	H	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	V	V	AB	F1
	8B		BA0	BA1	BA2	V				
REF -Per BK, All BK (REFRESH per Bank, All Banks)	Any	H	L	L	L	H	H	H	L	R1
	BG		BA0	BA1	BG0		SB0	V		
	16B	X	BA0	BA1	BA2	RFM	SB0	V	AB	F1
	8B		BA0	BA1	BA2		V	SB1		

Command Truth Table

- WRITE32 command is NOT allowed in 8 bank mode
 - WRITE : BL16 @ BG & 16BK mode, BL32 @ 8BK mode
 - WRITE 32 : BL32 @ BG & 16BK mode, Not allowed in 8BK mode

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
WRITE (WR16 or WR)	Any	H	L	H	H	C0	C3	C4	C5	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	C1	C2	AP	F1
	8B		BA0	BA1	BA2	V				
WRITE32 (WR32)	BG/16B	H	L	L	H	L	C3	C4	C5	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	C1	C2	AP	F1

Command Truth Table

- READ32 command is NOT allowed in 8 bank mode
 - READ: BL16 @ BG & 16BK mode, BL32 @ 8BK mode
 - READ 32 : BL32 @ BG & 16BK mode, Not allowed in 8BK mode

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
READ (RD16 or RD)	Any	H	H	L	L	C0	C3	C4	C5	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	C1	C2	AP	F1
	8B		BA0	BA1	BA2	V				
READ32 (RD32)	BG/16B	H	H	L	H	C0	C3	C4	C5	R1
	BG		BA0	BA1	BG0	BG1				
	16B	X	BA0	BA1	BA2	BA3	C1	C2	AP	F1

Command Truth Table

SDRAM Command	BK ORG	SDR	DDR							CK_t
		CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	Any	H	L	L	H	H	WS_WR	WS_RD	WS_FS	R1
		X	DC0	DC1	DC2	DC3	WRX	V	B3	F1

BL / n Definition

- BL/n indicates “effective” burst length and tCCD(min)
 - BL/n_min = minimum burst data transfer time in DQ bus
 - BL/n_max = required column array cycle time to allow next column array cycle

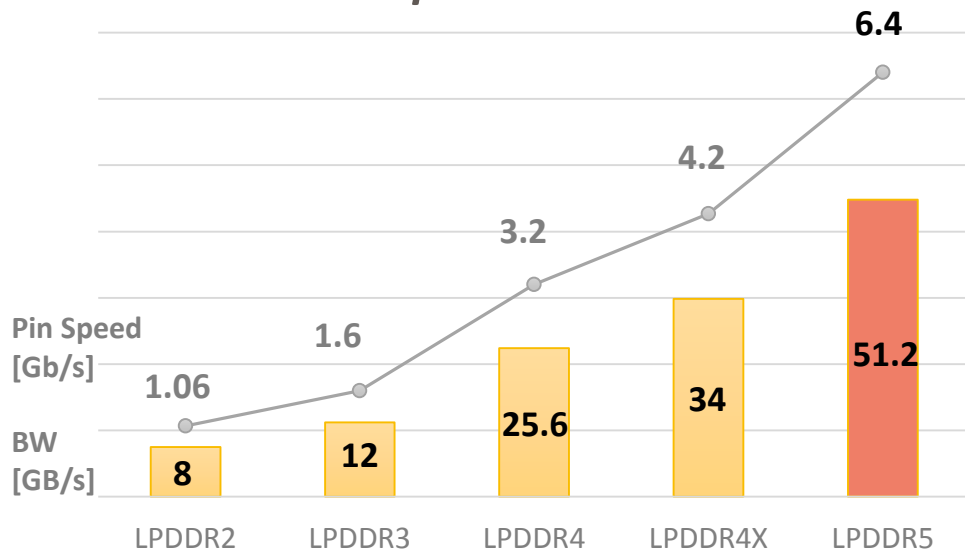
WCK:CK Ratio	Bank ORG	Bank-to-Bank Constraints	WCK Frequency	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
2:1	16B Mode	Any Bank to Bank	≤ 1600MHz	BL16	4*tCK (BL/4)	4*tCK (BL/4)	4*tCK (BL/4)
				BL32	8*tCK (BL/4)	8*tCK (BL/4)	8*tCK (BL/4)
	8B Mode	Any Bank to Bank	≤ 1600MHz	BL32	8*tCK (BL/4)	8*tCK (BL/4)	8*tCK (BL/4)
				MRR, WFF, RFF, RDC	≤ 1600MHz	BL16	8*tCK (BL/2)

BL / n Definition

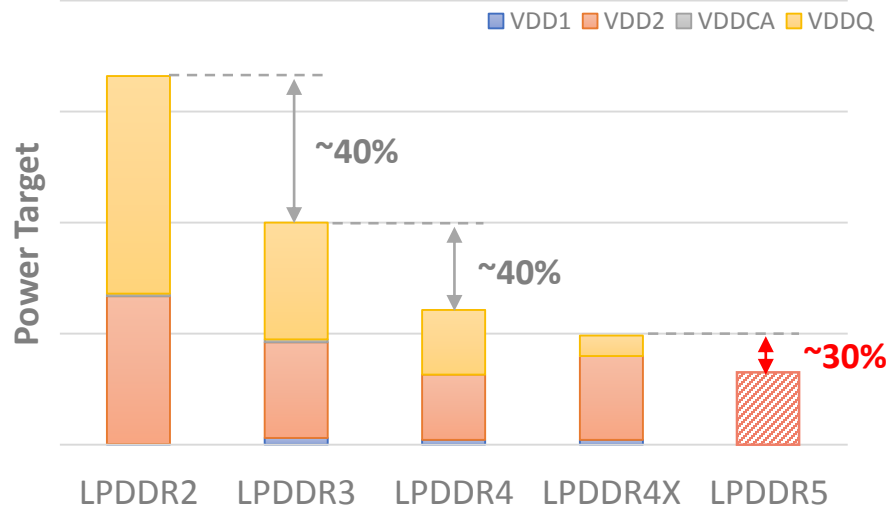
WCK:CK Ratio	Bank ORG	Bank-to-Bank Constraints	WCK Frequency	Burst Length (BL)	BL/n	BL/n_min	BL/n_max
4:1	16B Mode	Any Bank to Bank	$\leq 1600\text{MHz}$	BL16	$2 * t_{CK} (BL/8)$	$2 * t_{CK} (BL/8)$	$2 * t_{CK} (BL/8)$
				BL32	$4 * t_{CK} (BL/8)$	$4 * t_{CK} (BL/8)$	$4 * t_{CK} (BL/8)$
	BG Mode	Same BG Different BG Same BG Different BG	$> 1600\text{MHz}$	BL16	$4 * t_{CK} (2 * BL/8)$	$2 * t_{CK} (BL/8)$	$4 * t_{CK} (2 * BL/8)$
					$2 * t_{CK} (BL/8)$		
				BL32	$8 * t_{CK} (2 * BL/8)$	$6 * t_{CK} (1.5 * BL/8)$	$8 * t_{CK} (2 * BL/8)$
					$2 * t_{CK} (0.5 * BL/8)$		
	8B Mode	Any Bank to Bank MRR, WFF, RFF, RDC	Any Frequency Any Frequency	BL32	$4 * t_{CK} (BL/8)$	$4 * t_{CK} (BL/8)$	$4 * t_{CK} (BL/8)$
				BL16	$4 * t_{CK} (BL/4)$	$4 * t_{CK} (BL/4)$	$4 * t_{CK} (BL/4)$

New Features

Speed Trend



Power Trend



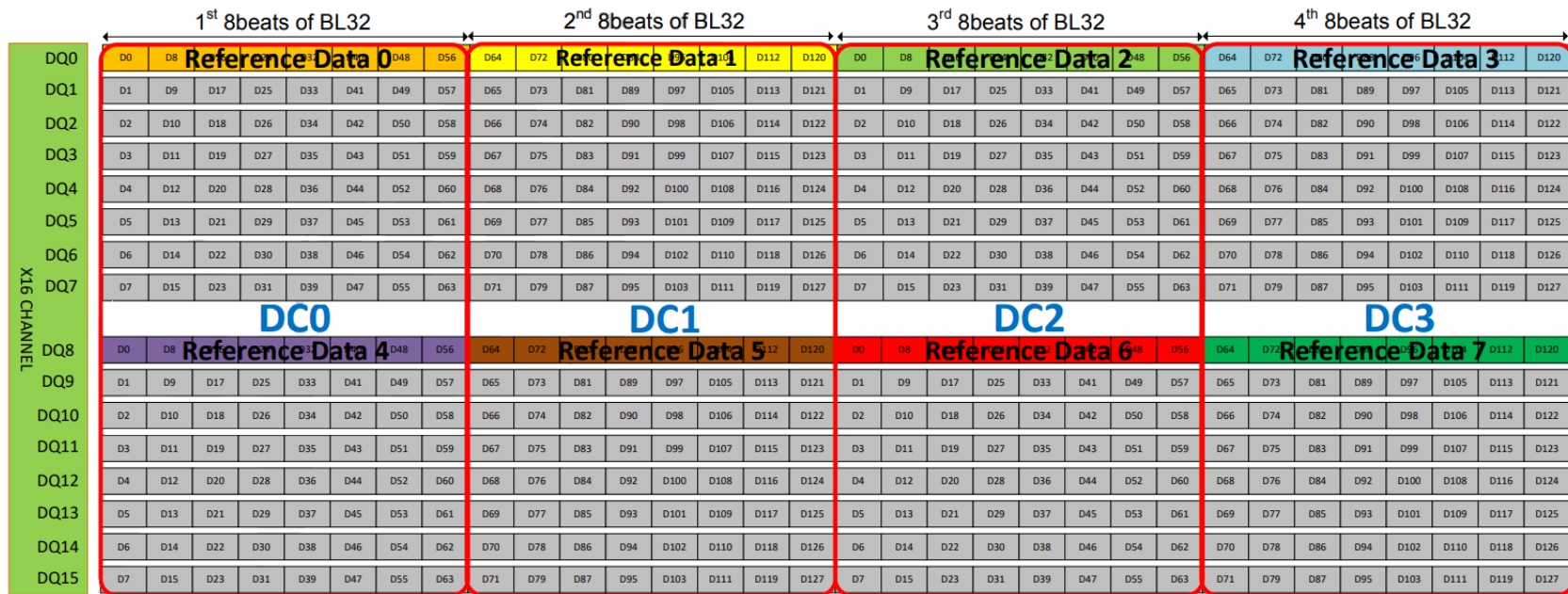
New Features – Power

1) Data Copy

- Provides an opportunity for data burst power reduction – esp. in high BW usage cases – by exploiting data repeatability
- Whenever data pattern is repeated over 8-byte data, only one DQ (per DQ byte) is utilized, hence enabling power reduction
 - only reference data is transferred through the DQ and copied internally
 - 8 byte of data copy granularity
- Applicable to both Write and Read operation
 - Data copy hit/miss information indicated by DC0-DC3 operands in CAS for Write;
 - by 1st and 9th beat of DM burst for Read

New Features – Power

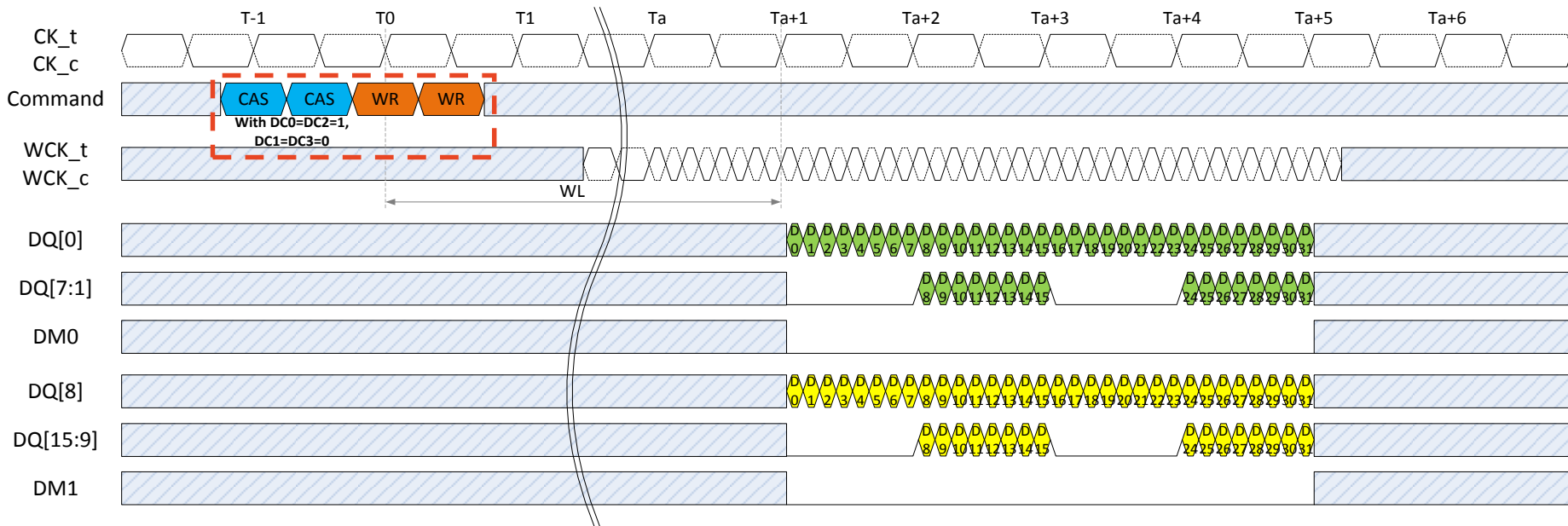
1) Data Copy



Data Copy Granularity and Reference Data Configuration in BL 32

New Features – Power

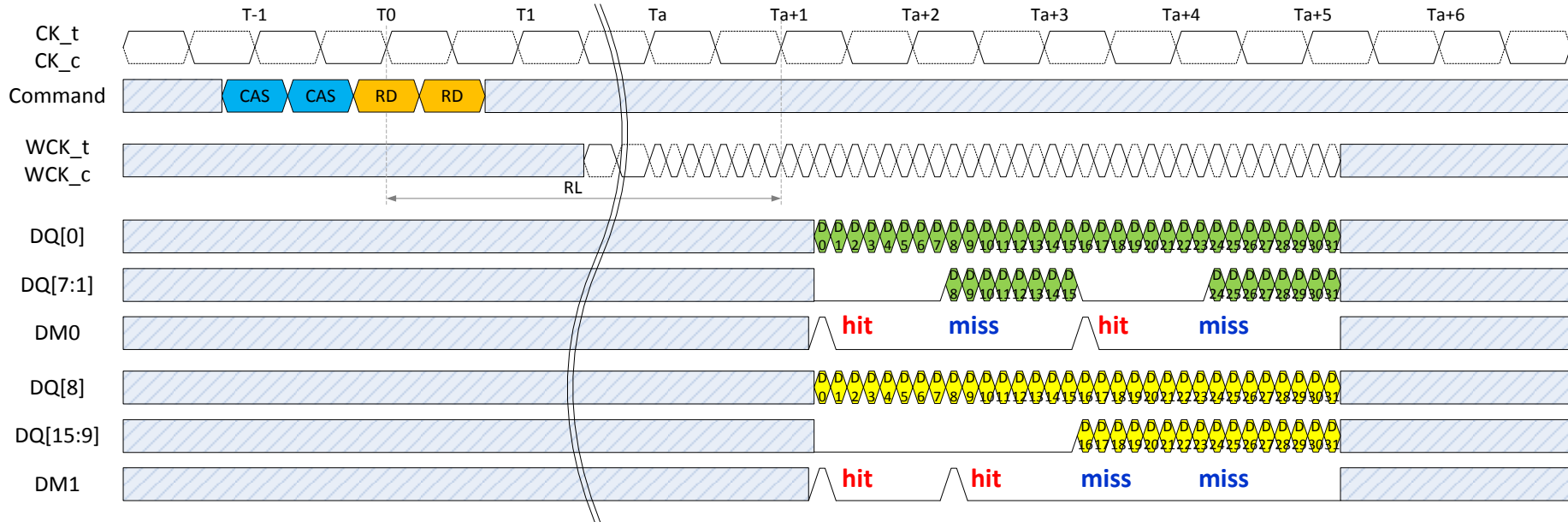
1) Data Copy



Write Data Copy Operation

New Features – Power

1) Data Copy



Read Data Copy Operation

New Features – Power

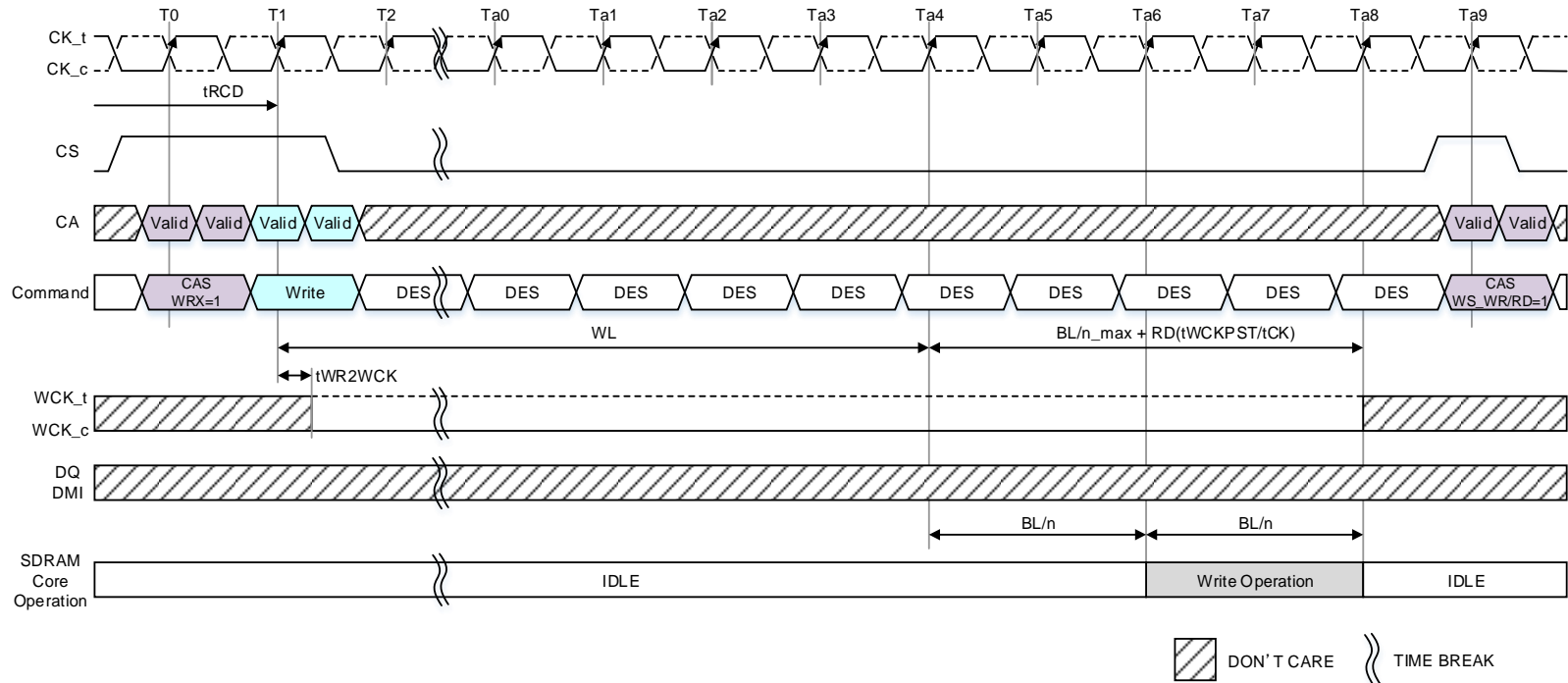
2) Write X

- Reduces power in write operation by exploiting data repeatability
 - Certain data values (e.g. Zero) appear frequently than “average”
- During Write X, data bus + WCK are not utilized
 - WRX, WXSA, WXSb in CAS determine data pattern on a byte level (e.g. WXSA = H → DQ[7:0] all 1's)
- Benefits:
 - Saves power as data bus is not activated
 - Saves bus BW in multi-rank systems (other ranks can use DQ bus during Write X)

SDRAM Command	SDR	DDR							CK_t
	CS	CA0	CA1	CA2	CA3	CA4	CA5	CA6	
CAS	H	L	L	H	H	V	V	V	R1
	X	DC0=0	DC1=0	DC2=0	DC3=0	WRX	V	Xfunc = H or L	F1

New Features – Power

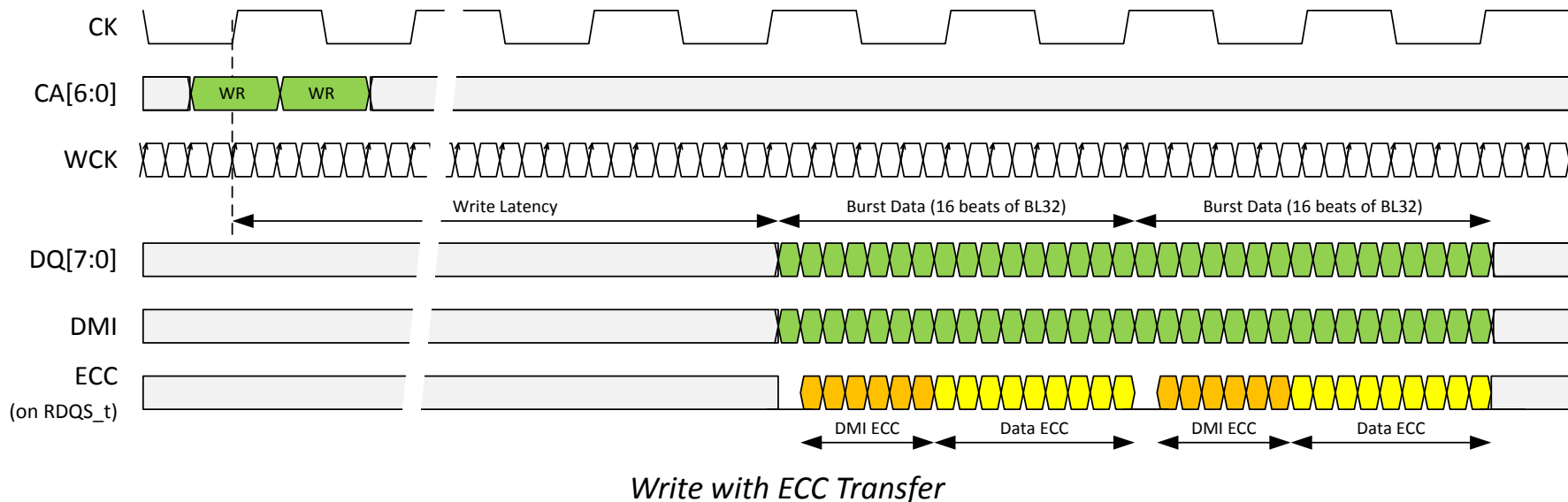
2) Write X



New Features – Channel

1) Link ECC

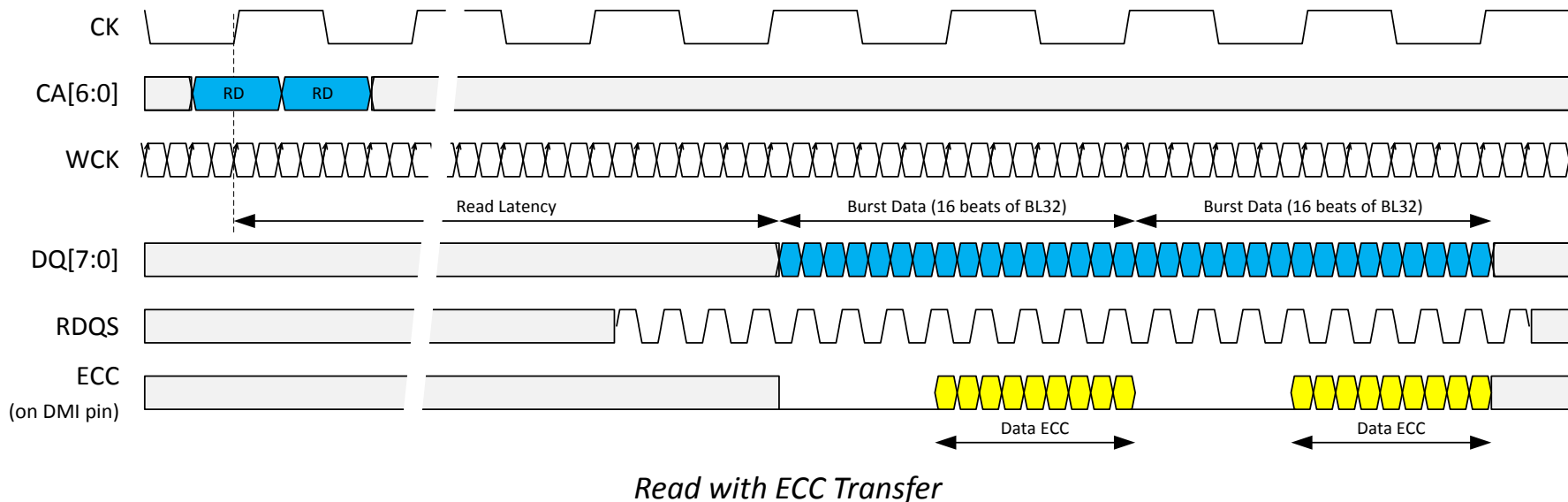
- To overcome the increase in BER per DQ, LPDDR5 supports Link ECC to correct bit error through the channel



New Features – Channel

1) Link ECC

- To overcome the increase in BER per DQ, LPDDR5 supports Link ECC to correct bit error through the channel



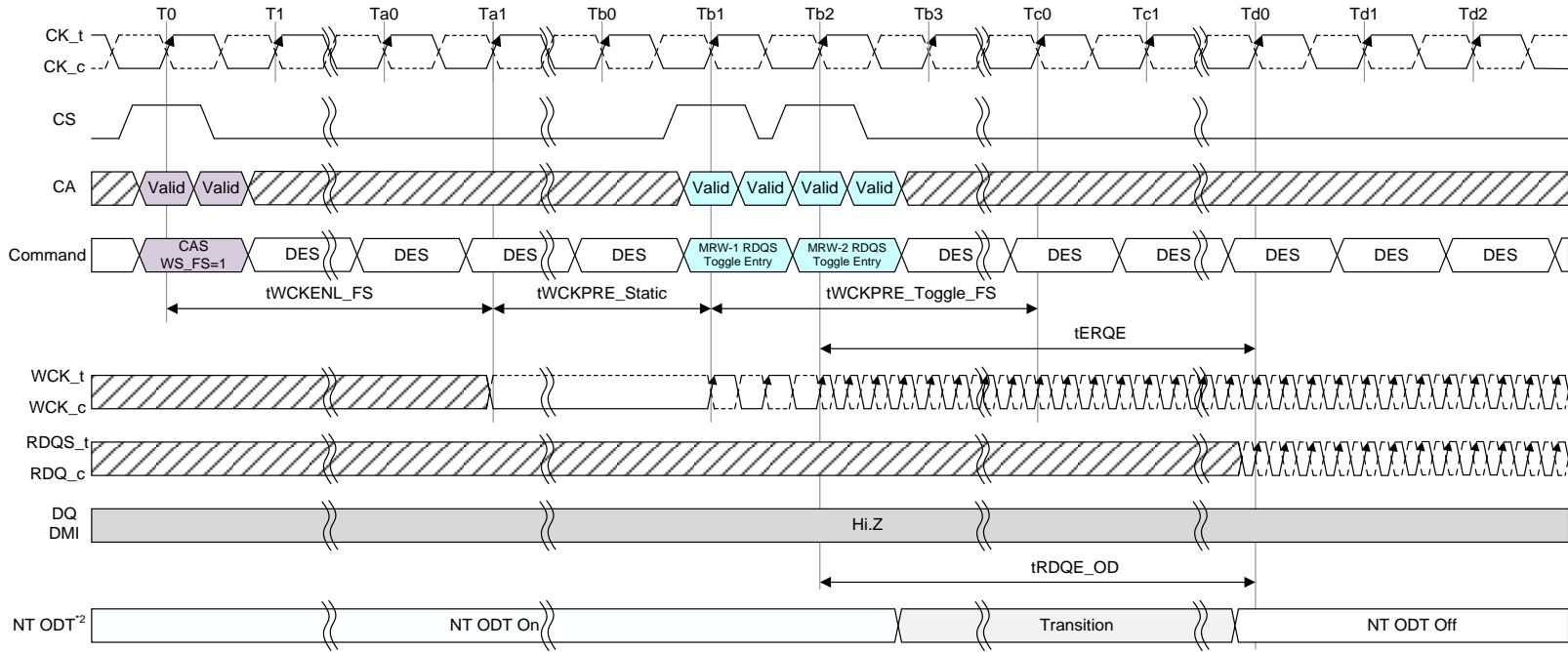
New Features – Channel

2) RDQS toggle

- RDQS toggle mode outputs continuous toggle pattern on RDQS pin
- Entry into and exit from the mode is initiated by programming MR46 OP[1]
 - CAS WS_FS must be issued before MRW command for entry
- RDQS_t/_c behavior follows the definition in MR20 OP[1:0]
 - Disabled, single-ended, differential
- Restrictions on operation during this mode
 - WCK must be toggled for the duration of the mode
 - Change in MRs concerned with output control not allowed

New Features – Channel

2) RDQS toggle



Entry Timing

 DON'T CARE  TIME BREAK

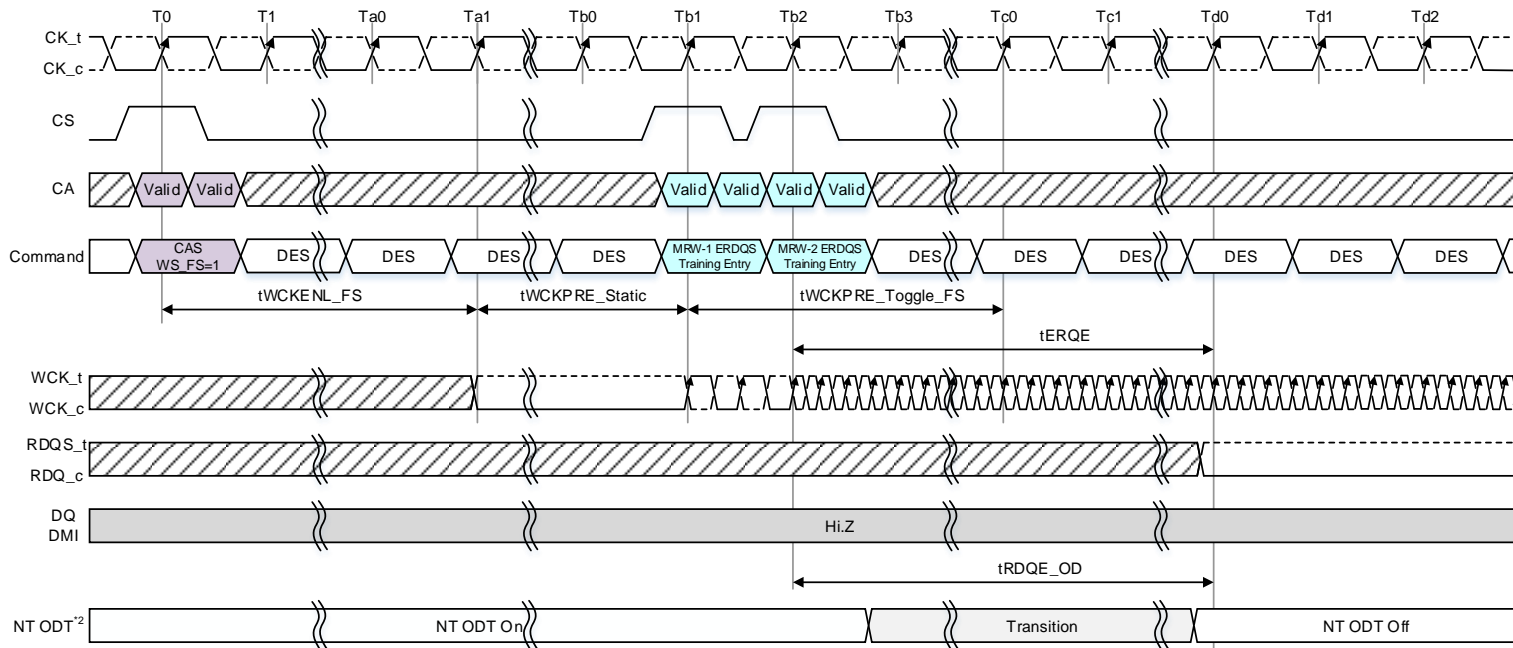
New Features – Channel

3) Enhanced RDQS Training

- Enhanced RDQS training mode keeps RDQS in low-Z state
 - RDQS_t is driven LOW and RDQS_c HIGH
- Entry into and exit from the mode is initiated by programming MR46 OP[0]
 - CAS WS_FS must be issued before MRW command for entry
- Restrictions on operation during this mode
 - WCK must be toggled for the duration of the mode
 - Change in MRs concerned with output control not allowed
- Enhanced RDQS and RDQS toggle modes are mutually exclusive

New Features – Channel

3) Enhanced RDQS Training



NOTE 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

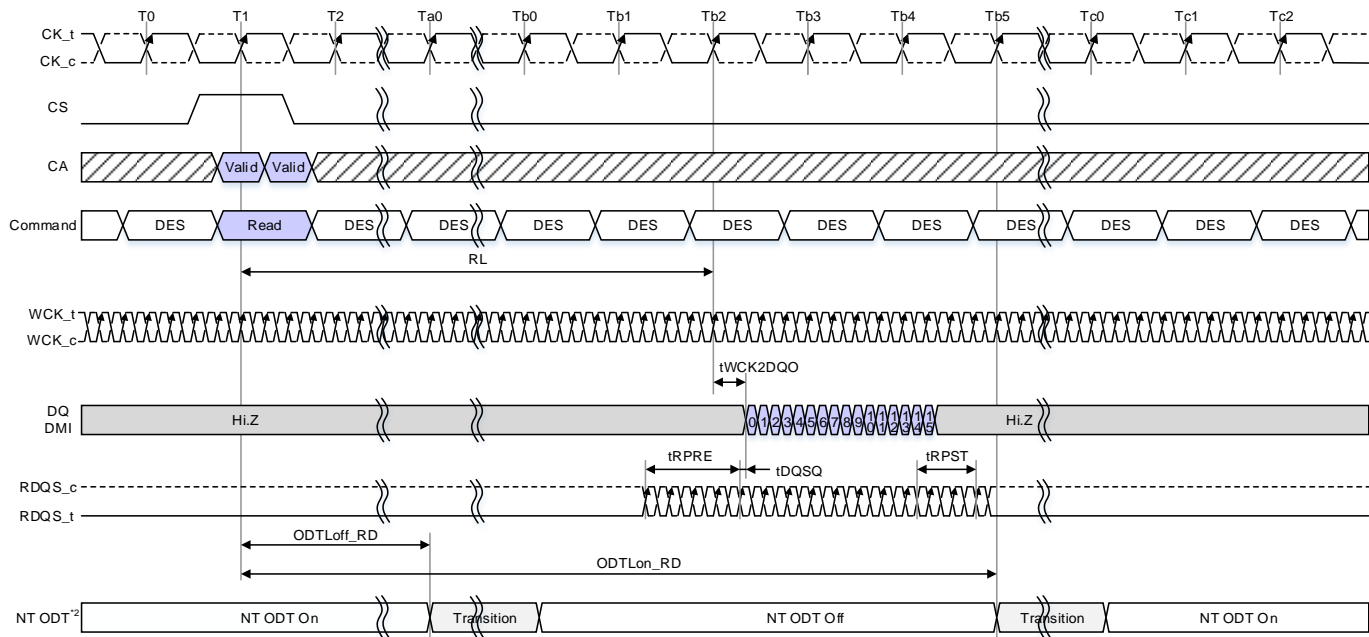
NOTE 2. In case of NT ODT is enable case for RDQS_t/c, DQ and/or DMI

 DON'T CARE  TIME BREAK

Entry Timing

New Features – Channel

3) Enhanced RDQS Training



NOTE 1. DES commands are shown for ease of illustration; other commands may be valid at these times.

NOTE 2. In case of NT ODT is enable case for RDQS_t/c, DQ and/or DMI.

DON'T CARE TIME BREAK

Read During Enhanced RDQS Training

Package Solution Summary

	Ball	Ball pitch	Body Size	Configuration
PoP	496b	0.4mm	14 x 12.4 mm ²	4Ch x64
	436b	0.4mm	14 x 14 mm ²	4Ch x64
Discrete	441b	0.65mm	14 x 14 mm ²	4Ch x64
	315b	0.8(X) / 0.7(Y)	-	2Ch x32
	315b	0.8(X) / 0.7(Y)	-	1Ch x16
uMCP	297b	0.5mm	-	2Ch x32

Package Solution

1) PoP – 496ball

- 4Ch x16 (Total x64)
- Ball Pitch:
 - 0.4 mm
- Body Size:
 - 14.0 mm X 12.4 mm

NC	NC	VDDH	VDD2H	VDD2L	VDDQ	VSS	VDD2H	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD2H	VDD2H	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD2H	VDD1	NC	NC			
NC	DQ3,A	RDG50,T,A	VSS	DQ5,A	VSS	CS1,A	VSS	VSS	DQ13,A	VSS	RDG51,T,A	VSS	DQ9,A	DQ1,C	VSS	RDG50,T,C	VSS	DQ5,C	VSS	CS1,C	VSS	VSS	DQ13,C	VSS	RDG51,T,C	DQ11,C	NC	
DQ1,A	VSS	RDG50,C,A	DM0,A	VDDQ	CA0,A	CS0,A	CA4,A	CA6,A	VDDQ	DM1,A	RDG51,C,A	DQ11,A	VDDQ	VDDQ	DQ3,C	RDG50,C,C	DM0,C	VDDQ	CA0,C	CS0,C	CA4,C	CA6,C	VDDQ	DM1,C	RDG51,C,C	VSS	DQ9,C	
VDDQ	DQ2,A	VDDQ	VSS	DQ6,A	VSS	CA2,A	CA3,A	VSS	DQ14,A	VSS	VDDQ	VSS	DQ8,A	DQ0,C	VSS	VDDQ	VSS	DQ8,C	VSS	CA2,C	CA3,C	VSS	DQ14,C	VSS	VDDQ	DQ10,C	VDDQ	
DQ8,A	VDDQ	WK0,C,A	DQ4,A	VDDQ	CA1,A	VDD2H	VDD2L	CA5,A	VDDQ	DQ12,A	WK1,C,A	DQ10,A	VDDQ	VDDQ	DQ2,C	WK0,C,C	DQ4,C	VDDQ	CA1,C	VDD2H	VDD2L	CA5,C	VDDQ	DQ12,C	WK1,C,C	VDDQ	DQ8,C	
VSS	VSS	WK0,T,A	VSS	DQ7,A	VSS	CK,T,A	CK,C,A	VSS	DQ15,A	VSS	WK1,T,A	VSS	ZQ,A,C	RESET,n	VSS	WK0,T,C	VSS	DQ7,C	VSS	CK,T,C	CK,C,C	VSS	DQ15,C	VSS	WK1,T,C	VSS	VSS	
VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDD2L	VSS	VDD2H	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	
VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VSS	VSS	VSS	VSS																					VSS	VSS	VSS	VSS	
VDD2H	VDD1	VDD2H	VDD2H																					VDD2H	VDD2H	VDD1	VDD2H	
VDD2H	VDD1	VDD2L	VDDQ	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDD2L	VSS	VDD2H	VDD2H	VDD2L	VSS	VSS	VDD2H	VDD2L	VDDQ	VDD2L	VDD1	VDD2H	
VSS	VSS	WK1,T,B	VSS	DQ15,B	VSS	CK,C,B	CK,T,B	VSS	DQ7,B	VSS	WK0,T,B	VSS	RFU	ZQ,B,D	VSS	WK1,T,D	VSS	DQ15,D	VSS	CK,C,D	CK,T,D	VSS	DQ7,D	VSS	WK0,T,D	VSS	VSS	
DQ8,B	VDDQ	WK1,C,B	DQ12,B	VDDQ	CA5,B	VDD2L	VDD2H	CA1,B	VDDQ	DQ4,B	WK0,C,B	DQ2,B	VDDQ	VDDQ	DQ10,D	WK1,C,D	DQ12,D	VDDQ	CA5,D	VDD2L	VDD2H	CA1,D	VDDQ	DQ4,D	WK0,C,D	VDDQ	DQ8,D	
VDDQ	DQ10,B	VDDQ	VSS	DQ14,B	VSS	CA3,B	CA2,B	VSS	DQ6,B	VSS	VDDQ	VSS	DQ8,B	DQ8,D	VSS	VDDQ	VSS	DQ14,D	VSS	CA3,D	CA2,D	VSS	DQ6,D	VSS	VDDQ	DQ2,D	VDDQ	
DQ9,B	VSS	RDG51,C,B	DM1,B	VDDQ	CA6,B	CA4,B	CS0,B	CA0,B	VDDQ	DM0,B	RDG50,C,B	DQ3,B	VDDQ	VDDQ	DQ11,D	RDG51,C,D	DM1,D	VDDQ	CA6,D	CA4,D	CS0,D	CA0,D	VDDQ	DM0,D	RDG50,C,D	VSS	DQ1,D	
NC	DQ11,B	RDG51,T,B	VSS	DQ13,B	VSS	VSS	CS1,B	VSS	DQ5,B	VSS	RDG50,T,B	VSS	DQ1,B	DQ9,D	VSS	RDG50,T,D	VSS	DQ13,D	VSS	VSS	CS1,D	VSS	DQ5,D	VSS	RDG50,T,D	DQ3,D	NC	
NC	NC	VDD1	VDD2H	VDD2L	VDDQ	VDD2H	VSS	VDD2L	VDD2H	VDD2H	VDDQ	VDD1	VDD2L	VDD2L	VDD2H	VDD2H	VSS	VDD2H	VDD2H	VDD2L	VDD2H	VSS	VDDQ	VDD2L	VDD2H	VDD1	NC	NC

Package Solution

- 4Ch x64
- Ball Pitch:
 - 0.65 mm
- Body Size:
 - 14 mm x 14 mm

3) Discrete – 441ball

VSS	VSS	VDD1	VDD2_L	VSS	VDD0_H	VDD1	VSS	VDD2_L	VDD2_H	VDD2_H	VSS	VDD1	VDD2_L	VSS	VDD2_H	VDD1	VSS	VDD2_L	VSS	VSS	
VSS	DQ0_A	VSS	DQ3_A	VDD2_H	VSS	DQ11_A	DQ9_A	DQ8_A	VSS	VDD2_H	DQ0_C	VSS	DQ3_C	VDD2_H	VSS	DQ11_C	DQ9_C	DQ8_C	VSS	VSS	
VDD2_H	VSS	DQ2_A	VDDQ	CA0_A	VDD2_H	VSS	DQ10_A	VDDQ	VSS	VSS	DQ2_C	VDDQ	CA0_C	VDD2_H	VSS	DQ10_C	VDDQ	VDD2_H	VDD2_H	VDD2_H	
VSS	DQ1_A	WCK0_C_A	VSS	CA1_A	VSS	CS0_A	VDDQ	VSS	WCK1_T_A	VDDQ	DQ1_C	WCK0_C_C	VSS	CA1_C	CS0_C	VDDQ	VSS	WCK1_T_C	VDDQ	VSS	
VDDQ	RDQS_0_C_A	VSS	WCK0_T_A	VSS	CS1_A	VSS	WCK1_C_A	DM11_A	VSS	VDDQ	RDQS_0_C_C	VSS	WCK0_T_C	VSS	CS1_C	VSS	WCK1_C_C	VSS	VSS	VDD2_H	
VDDQ	RDQS_0_T_A	VSS	VDDQ	VSS	CA2_A	VSS	RDQS_1_T_A	VSS	VDDQ	VSS	VDDQ	VSS	RDQS_0_T_C	VSS	CA2_C	VSS	RDQS_1_T_C	VSS	VDDQ	VDD2_H	
VSS	DQ4_A	VDDQ	DM10_A	RFU0_A	RFU1_A	CA6_A	VSS	RDQS_1_C_A	VSS	VDDQ	DM10_C	VDDQ	DQ4_C	RFU0_C	RFU1_C	CA6_C	VSS	RDQS_1_C_C	VSS	VSS	
VDD2_L	VSS	DQ5_A	VSS	CK_T_A	VSS	CA5_A	VDDQ	VSS	DQ12_A	VSS	VSS	DQ5_C	VSS	CK_T_C	VSS	CA5_C	VDDQ	VSS	DQ12_C	VDD2_L	
VDD2_H	DQ6_A	DQ7_A	VDD2_H	VSS	CK_G_A	VSS	DQ14_A	DQ13_A	VSS	VDD2_L	DQ6_C	DQ7_C	VDD2_L	ZQ_A_C	CK_G_C	VSS	DQ14_C	DQ13_C	VSS	VDD2_H	
VSS	VDD2_H	VDD2_H	VDD2_H	VSS	CA3_A	CA4_A	VDD2_L	VSS	DQ15_A	VDD2_H	VDD2_H	VDD2_H	VDD2_H	VSS	CA3_C	CA4_C	VDD2_H	VSS	DQ15_C	VSS	
VDD2_H	VDD2_L	VDD2_L	VDD2_L	VDD2_L	VDD2_L	VSS	VDD2_H	VDD2_H	VSS	VSS	VSS	VDD2_H	VDD2_H	VSS	VDD2_H	VDD2_L	VDD2_L	VDD2_L	VDD2_L	VDD2_H	
VSS	DQ15_B	VSS	VDD2_H	CA4_B	CA3_B	VSS	VDD2_H	VDD2_H	VDD2_H	VDD2_H	DQ15_D	VSS	VDD2_L	CA4_D	CA3_D	VSS	VDD2_H	VDD2_H	VDD2_H	VSS	
VDD2_H	VSS	DQ13_B	DQ14_B	VSS	CK_C_B	ZQ_B_D	VDD2_L	DQ7_B	DQ6_B	VDD2_L	VSS	DQ13_D	DQ14_D	VSS	CK_C_D	VSS	VDD2_H	DQ7_D	DQ6_D	VDD2_H	
VDD2_L	DQ12_B	VSS	VDDQ	CA5_B	VSS	CK_T_B	VSS	DQ5_B	VSS	VSS	DQ12_D	VSS	VDDQ	CA5_D	VSS	CK_T_D	VSS	DQ5_D	VSS	VDD2_L	
VSS	VSS	RDQS_1_C_B	VSS	CA6_B	RFU1_B	RFU0_B	DQ4_B	VDDQ	DM10_B	VSS	VSS	RDQS_1_C_D	VSS	CA6_D	RFU1_D	RFU0_D	DM10_D	VDDQ	DQ4_D	VSS	
VDD2_H	VDDQ	VSS	RDQS_1_T_B	VSS	CA2_B	VSS	VDDQ	VSS	VSS	VDDQ	VSS	RDQS_0_T_B	VSS	VDDQ	VSS	RDQS_1_T_D	VSS	CA2_D	VSS	RDQS_0_T_D	VDDQ
VDD2_H	VSS	DM11_B	WCK1_C_B	VSS	CS1_B	VSS	WCK0_T_B	VSS	RDQS_0_C_B	VDDQ	VSS	DM11_D	WCK1_C_D	VSS	CS1_D	VSS	WCK0_T_D	VSS	RDQS_0_C_D	VDDQ	
VSS	VDDQ	WCK1_T_B	VSS	VDDQ	CS0_B	CA1_B	VSS	WCK0_C_B	DQ1_B	VDDQ	VDD2_H	WCK1_T_D	VSS	VDDQ	CS0_D	CA1_D	VSS	WCK0_C_D	DQ1_D	VSS	
VDD2_H	VDD2_H	VDDQ	DQ10_B	VSS	VDD2_H	CA0_B	VDDQ	DQ2_B	VSS	VSS	VDD2_H	VDDQ	DQ10_D	VSS	VDD2_H	CA0_D	VSS	VDD2_H	DQ2_D	VSS	
VSS	RESE_T_N	DQ8_B	DQ9_B	DQ11_B	VSS	VDD2_H	DQ3_B	VSS	DQ0_B	VSS	VSS	DQ8_D	DQ9_D	DQ11_D	VSS	VDD2_H	DQ3_D	DQ0_D	VSS	VSS	
VSS	VSS	VDD2_L	VSS	VDD1	VDD2_H	VSS	VDD2_L	VDD1	VSS	VSS	VDD2_H	VDD2_H	VDD2_L	VSS	VDD1	VDD2_H	VSS	VDD2_L	VDD1	VSS	VSS

Package Solution

- Application:
 - Client & Various Application (like 200b in LPDDR4)
- Ball Pitch
 - 0.8mm(X) , 0.7mm (Y)
- Body Size

4) Discrete – 315ball

NC	NC	VDDQ	DM10_A	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DM11_A	VDDQ	NC	NC
NC	VDDQ	RDG95_T_A	VSS	DQ4_A	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ12_A	VSS	RDG91_T_A	VDDQ	NC
VDD1	DQ1_A	VDDQ	RDG90_C_A	VSS	DQ5_A	VDD2H	VSS	VDD2H	DQ13_A	VSS	RDG91_C_A	VDDQ	DQ9_A	VDD1
DQ8_A	VSS	DQ3_A	VDDQ	WCK0_C_A	VSS	VSS	VDD2H	VSS	VSS	WCK1_C_A	VDDQ	DQ11_A	VSS	DQ8_A
VSS	DQ2_A	VSS	WCK0_T_A	VDDQ	DQ6_A	VDD2H	VSS	VDD2H	DQ14_A	VDDQ	WCK1_T_A	VSS	DQ10_A	VSS
VDDQ	VSS	VDDQ	VDDQ	DQ7_A	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ15_A	VDDQ	VDDQ	VSS	VDDQ
VDDQ	VDDQ	VSS	CA0_A	VSS	CS1_A	VSS	CA2_A	VSS	CA4_A	VSS	CA6_A	VSS	VDDQ	VDDQ
Reset_N	VDD2L	VSS	VSS	CA1_A	VSS	CS0_A	VSS	CK_L_A	VSS	CA3_A	VSS	CA5_A	VDD2L	ZQ_A
VSS	VDD2L	VSS	RFU	VDD2H	RFU	VSS	VSS	CK_C_A	VSS	VDD2H	VSS	VSS	VDD2L	VSS
VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
VSS	VSS	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VSS	VSS	VSS
VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VSS	VSS	VSS	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H	VDD2H
VSS	VDD2L	VSS	VSS	VDD2H	VSS	CK_C_B	VSS	VSS	VSS	VDD2H	VSS	VSS	VDD2L	VSS
RFU	VDD2L	CA5_B	VSS	CA3_B	VSS	CK_L_B	VSS	CS0_B	VSS	CA1_B	VSS	VSS	VDD2L	RFU
VDDQ	VDDQ	VSS	CA6_B	VSS	CA4_B	VSS	CA2_B	VSS	CS1_B	VSS	CA0_B	VSS	VDDQ	VDDQ
VDDQ	VSS	VDDQ	VDDQ	DQ15_B	VDD2H	VDD2H	VSS	VDD2H	VDD2H	DQ7_B	VDDQ	VDDQ	VSS	VDDQ
VSS	DQ10_B	VSS	WCK1_L_B	VDDQ	DQ14_B	VDD2H	VSS	VDD2H	DQ6_B	VDDQ	WCK0_T_B	VSS	DQ2_B	VSS
DQ8_B	VSS	DQ11_B	VDDQ	WCK1_C_B	VSS	VSS	VDD2H	VSS	VSS	WCK0_C_B	VDDQ	DQ3_B	VSS	DQ0_B
VDD1	DQ9_B	VDDQ	RDG91_C_B	VSS	DQ13_B	VDD2H	VSS	VDD2H	DQ5_B	VSS	RDG95_C_B	VDDQ	DQ1_B	VDD1
NC	VDDQ	RDG91_T_B	VSS	DQ12_B	VDD2L	VDD2H	VSS	VDD2H	VDD2L	DQ4_B	VSS	RDG90_T_B	VDDQ	NC
NC	NC	VDDQ	DM11_B	VSS	VDD2L	VDD2H	VDD2H	VDD2H	VDD2L	VSS	DM10_B	VDDQ	NC	NC

Package Solution

- Application:
 - Mobile
- Ball Pitch:
 - 0.5 mm
- Body Size:
 - 11.5 mm X 13.0 mm

5) uMCP – 297ball

DNU	DNU	VDD2H	VDD1	VDD2L	VDD2L	VSS	VDDQ	VDDQ	VSS					VSS	VDD2H	VDD2H	VSS	DNU	DNU
DNU	VSS	VSS	DQ8_A	VSS	DQ8_A	VSS	RDQS1_C_A	RDQS1_T_A	VDD2H				CA5_A	CA6_A	VDD1	VDD1	RFU	DNU	
		DQ10_A	VSS	DQ11_A	VSS	DM11_A	VSS	VSS	VDD2H				CA3_A	VSS	CA4_A	VSS	Z00		
		DQ12_A	VSS	VDDQ	VDDQ	VSS	WCK1_C_A	WCK1_T_A	VSS				VSS	CK_c_A	VSS	VSS	VSS		
	VDDQ	DQ14_A	VSS	DQ13_A	VSS	DQ15_A	VDDQ	VDDQ	VDD2L				VSS	CK_t_A	VSS	CS1_A	VSS		
													CA2_A	VSS	VSS	CS0_A	CS2_A		
							VSS	VSS	VDD2L			VDD2L	CA0_A	CA1_A	VSS	VSS	RFU		
	VSS	DQ5_A	DQ6_A	VSS	DQ7_A	VSS	VDDQ	VDDQ	VDD2L			VDD2H	VDD2H	VSF1	VSSm	VSSm	VDDIQ		
	DM10_A	VSS	VDDQ	VDDQ	WCK0_C_A	WCK0_T_A	VSS	VDD1				VSF3	RST_H	VCCQ	VCCQ	VCCQ	VCCQ		
	DQ0_A	DQ4_A	VSS	DQ3_A	VSS	RDQS0_C_A	RDQS0_T_A	VSS	VDD2H			VSF2	VSSm	VSSm	VSSm	VCCQ	VSSm		
	VDD2H	VSS	DQ1_A	DQ2_A	VDD2L	VDD1	VSS	VSS	VDD2H				DIN1_c	DIN1_t	VSSm	VSSm	VCC		
													VSSm	VSSm	DIN0_c	DIN0_t	VCC		
													DOU11_c	DOU11_t	VSSm	VSSm	VCC		
	VDD2L	VSS	DQ8_B	DQ10_B	VDD2L	VDD1	VSS	VSS	VDD2H				VSSm	VSSm	DOU10_c	DOU10_t	VCC		
	DQ8_B	DQ12_B	VSS	DQ11_B	VSS	RDQS1_C_B	RDQS1_T_B	VDD2H				VSF6	REF_CLK	VSSm	VSSm	VSSm	VSSm		
	DM11_B	VSS	VDDQ	VDDQ	WCK1_C_B	WCK1_T_B	VSS	VDD1				VSF5	VSSm	VCCQ	VCCQ	VCCQ	VCCQ		
	VSS	DQ13_B	DQ14_B	VSS	DQ15_B	VSS	VDDQ	VDDQ	VDD2L			VDD2H	VDD2H	VSF4	VCCQ	VSSm	VDDIQ		
							VSS	VSS	VDD2L				VDD2L	CA6_B	CA5_B	VSS	VSS	VDD1	
													VDDQ	CA4_B	VSS	VSS	VSS	VDDQ	
	VDDQ	DQ6_B	VSS	DQ5_B	VSS	DQ7_B	VDDQ	VDDQ	VDD2L				VSS	CK_c_B	VSS	CS0_B	VDDQ		
		DQ4_B	VSS	VDDQ	VDDQ	VSS	WCK0_C_B	WCK0_T_B	VSS				VSS	CK_t_B	VSS	CS1_B	CS2_B		
		DQ2_B	VSS	DQ3_B	VSS	DM10_B	VSS	VSS	VDD2H				CA3_B	VSS	CA2_B	VSS	RESET		
DNU	VSS	VSS	DQ1_B	VSS	DQ0_B	VSS	RDQS0_C_B	RDQS0_T_B	VDD2H				CA1_B	CA0_B	VDD1	VDD1	VSS	DNU	
DNU	DNU	VDD2H	VDD1	VDD2L	VDD2L	VSS	VDDQ	VDDQ	VSS				VSS	VDD2H	VDD2H	VSS	DNU	DNU	