DUT Connector Definition and Test Environment for HyperTransport

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Version 14

Introduction

HyperTransport has a strong need for compatibility testing. An important enabling element for compatibility testing is to define a standardized connector to use between HT compatibility testing boards. Along with the connector, a mechanical specification is required to allow interoperation.

The Consortium does not make claims of suitability of this connector for production boards as it remains outside the scope of this effort. It will remain up to the individual companies, producer or consumers of HyperTransport devices to determine this connector's applicability for their specific product design.

Requirements:

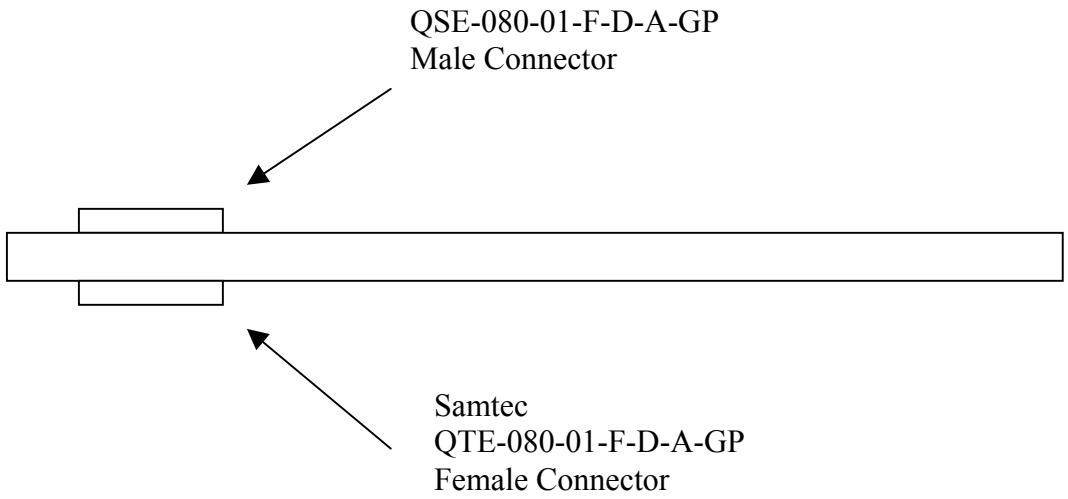
1. Standardized connector
2. Standardized, reliable mechanical arrangement
3. Allows good signal integrity
4. Provides a means of making long HT daisy chains
5. Provides a means of making HT Switch test configurations
6. Mounted horizontally for easy probe access
7. Supports 2, 4, 8, or 16 bit operation

Optional Requirements

1. Useful for Daughter-Card applications
2. Compatible with the HT 2.x proposal
3. Supplies power to board
4. Supports Dual Host Mode
5. Supports 32 bit operation
6. Allows the probing connector to be used

Connector

The specified connectors are the Samtec male connector (QSE) for the top of the board and the Samtec female connector (QTE) for the bottom of the board. The connectors are normally mounted in pairs to give maximum flexibility in connecting HT chains, on HT 2.0 the signal integrity may not allow the stubs caused by the second connector so the configurations are more constrained. The connector on the bottom of the board is always mounted rotated 180 degrees with respect to the one on the top of the board with most of the connector pads sharing vias so that pin n of the topside QSE connector is common with pin 161-n of the bottomside QTE connector (this is not true for a few slow speed signals). The connector pair on the left side of a board is rotated with respect to the connector pair on the right side of the board. These orientations seem strange, but allow a wider range of test configurations, and are best explained using the examples below. Both connectors are not required to be on each board. It may be useful to put connectors on both the top and bottom to al

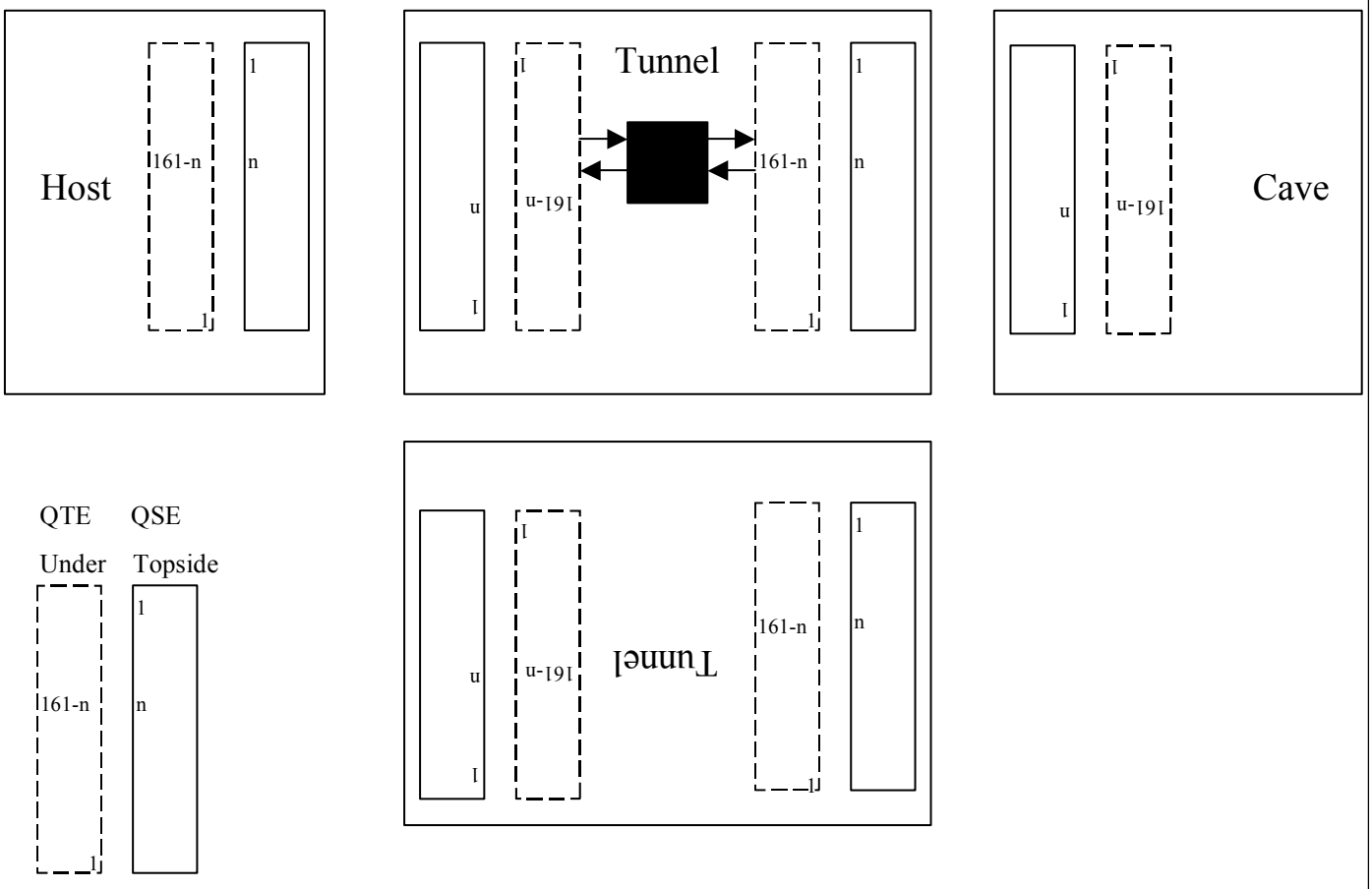


(For reference the SAMTEC QTE-080-01-F-D-EM2-GP is the board edge mounting connector that mates with the topside DUT connector. This part may be useful for evaluation boards for cave devices that want to plug in to a DUT option slot on a host evaluation card that fits in a standard form factor ATX case.)

QSE Series overview:
http://www.samtec.com/signal_integrity/technical_specifications/overview.asp?series=QSE

QSE Electrical characteristics report:
http://www.samtec.com/ftppub/testrpt/qteqsew.pdf

Note: it does not matter if the top of one card plugs to bottom of other or bottom to top, in both cases pin n of a QSE links to pin n of a QTE



Note: connectors are really one above the other, they are shown separated here for clarity.

Example

The example configuration above shows a simple system with a host, tunnel and cave. The Tunnel card shows how the CADOUT and CADIN signals are positioned on the package of a device with the recommended pinout/ballout. The cards are all connected using DUT connectors. In each of the connections the board on the left may be plugged in to the top of the board on the right or the board on the right may be plugged in to the top of the board on the left. In either case the same signals are connected – with the host underneath the signal coming in to pin 21 on the host top connector will connect to pin 21 on the tunnel bottom connector, the other way the host bottom connector pin 140 is to the tunnel pin 140. Since the host topside pin 21 and bottom side pin 140 share a common via, and the same is true for the tunnel, either connection works.

Either HT link on a tunnel should be capable of being connected to the host, and as the figure shows the left-right connector organization allows the tunnel board to be rotated and still be able to plug in on both ends. This is particularly important if the tunnel has

different size links on each port. The DUT allows both to be tested with the host and both with the cave.

HT 2.x Operation
For HT 2.x applications, it will likely to be necessary to not stuff one of these two connectors to help maintain signal integrity. This connector is quite good electrically, but everything matters at the high frequencies associated with HT 2.x. The diagrams of each board give a recommendation for this.

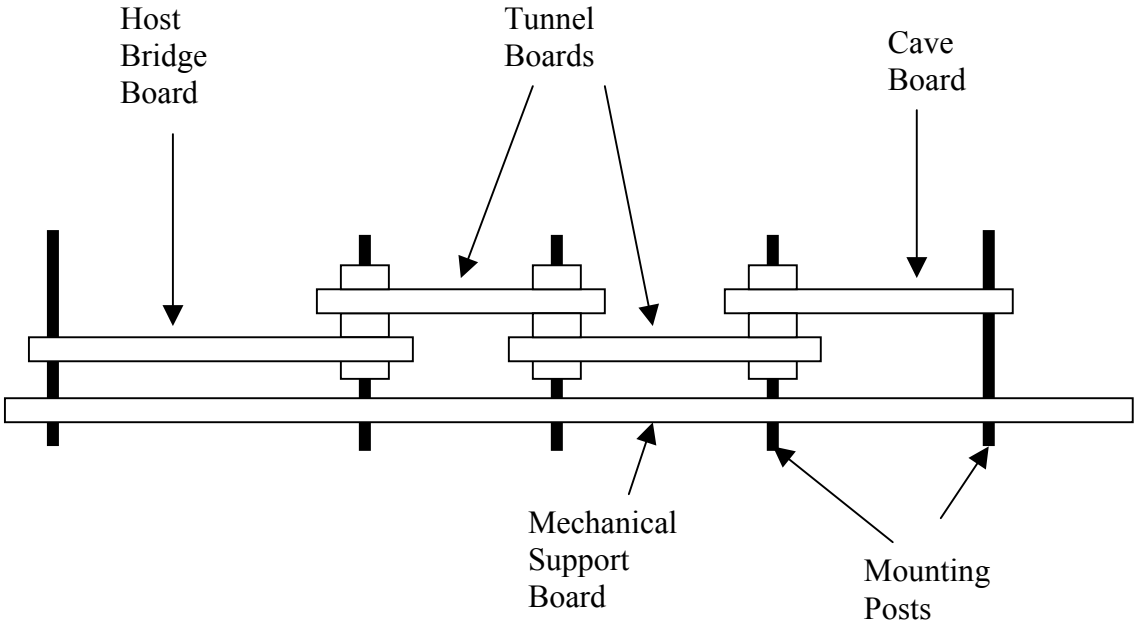
Probing Connector
Users may well want to add a HT Probing Connector to some or all boards to allow attachment of a logic analyzer. It can be found in out the HTC web site under "Technical Documentation". It should be noted that the CTL leads on the probe connector have a less than optimal placement which make its use on 4 layer boards difficult.

Cabled Operation
Cables are available from Precision Interconnect, a Tyco subsidiary. The URL is:
http://www.precisionint.com/tdibrsb/default.asp
These cables support somewhat high frequency operation. They are somewhat expensive (low $hundreds).

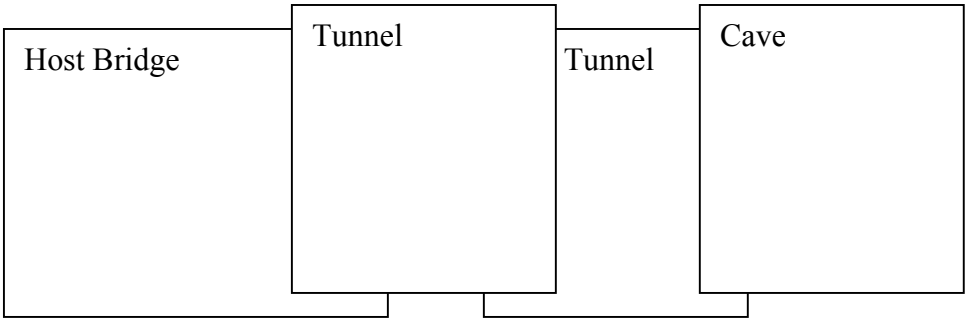
If the cable is to be used to link cards topside QSE to QSE the cable version that links pin 1 and 160 is needed and it will require modifications for the slow speed signals. The QTE to QSE pin 1 to pin 1 cable will work without modifications.

Connected Daisy Chain Configuration

The following is a side view of a daisy chain of HT boards:

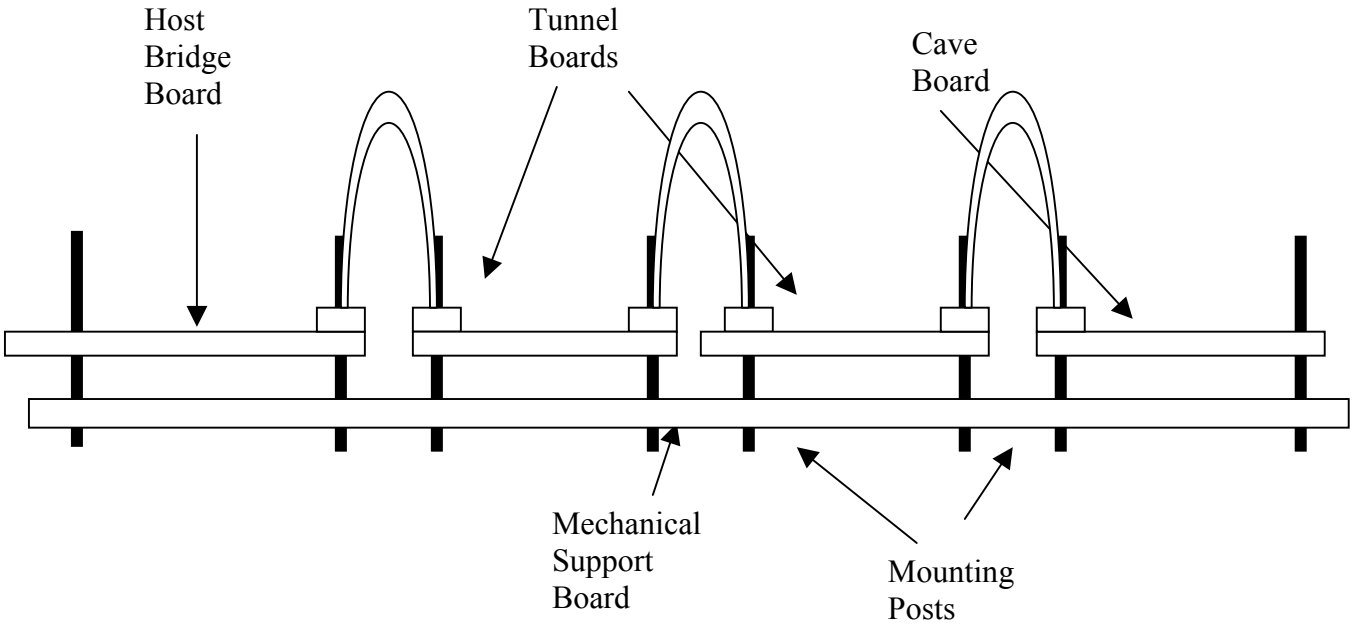


Oblique View

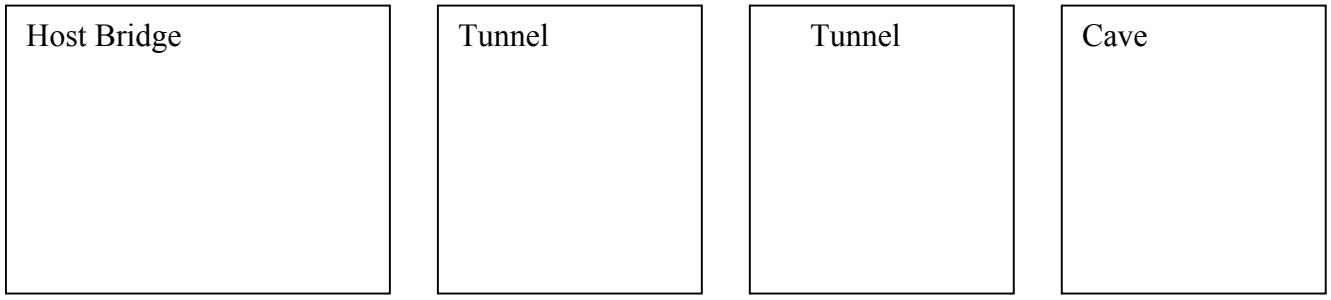


Cabled Daisy Chain Configuration

The following is a side view of a daisy chain of HT boards. There is some risk in this configuration for HT 2.0 operation.

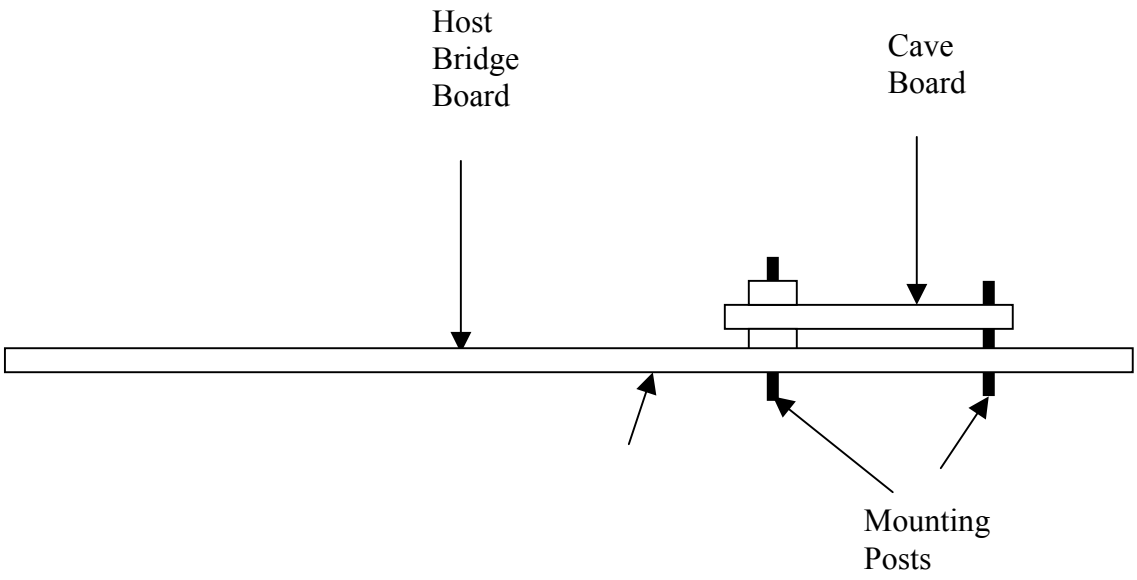


Oblique View

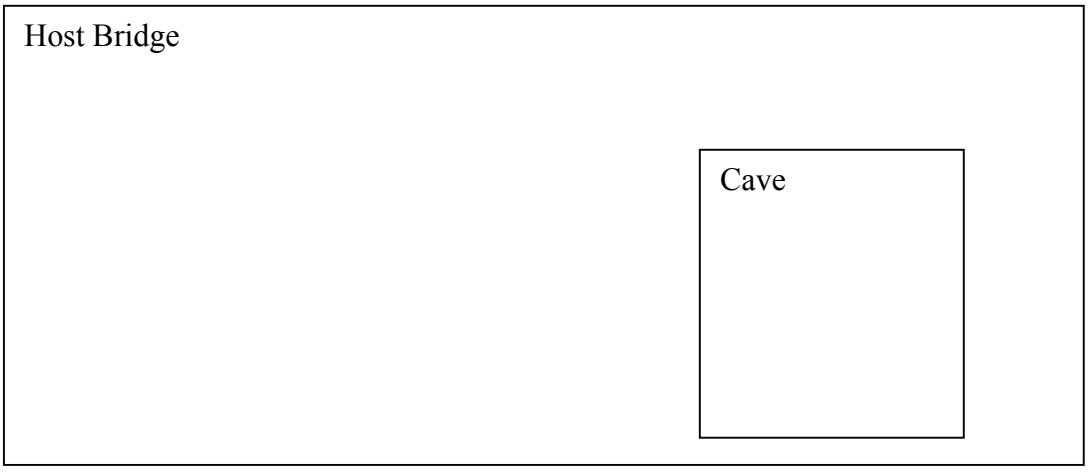


Daughter Card Configuration

The following is a side view of a daughter card application of this connector:

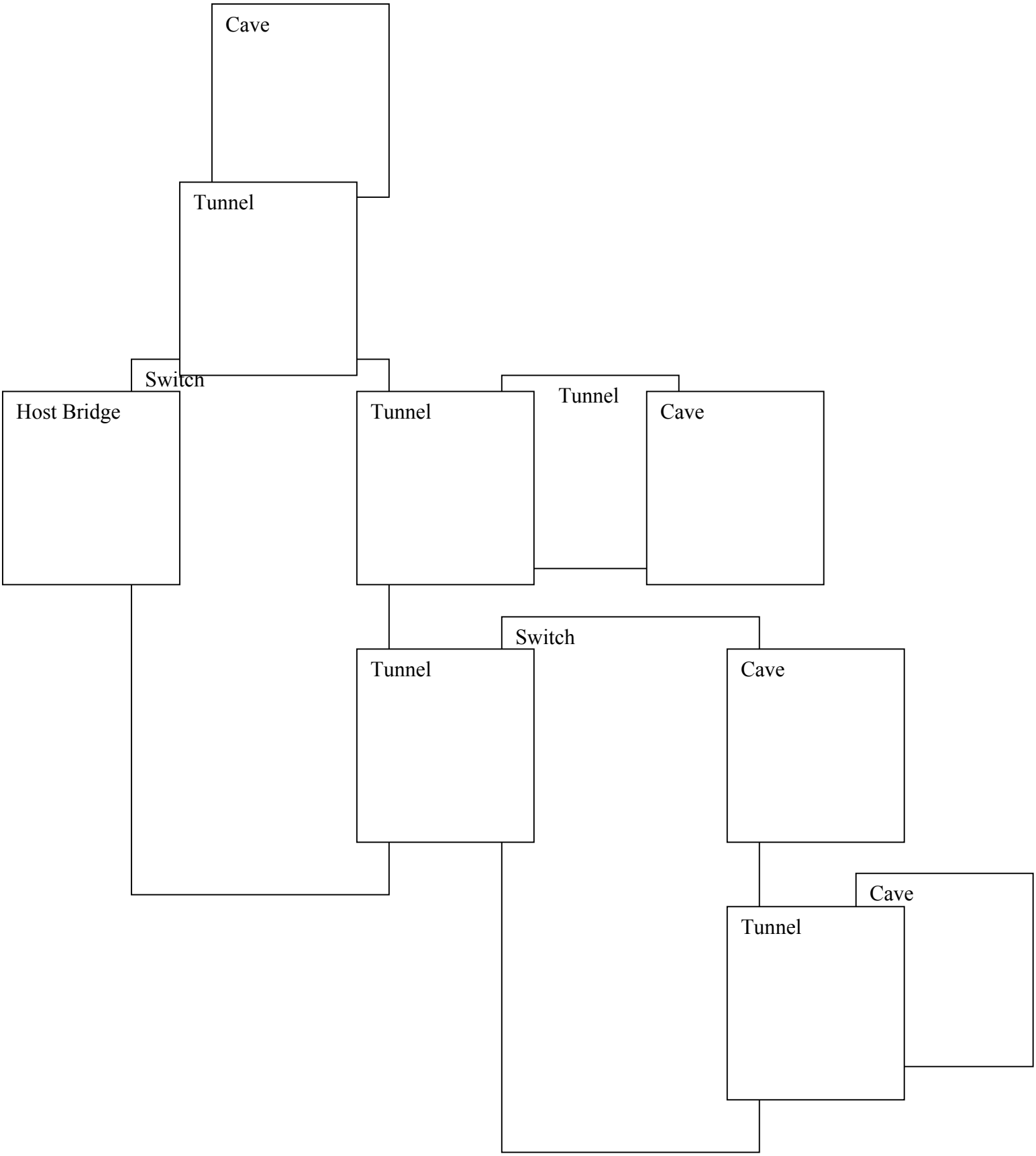


Oblique View



Switch DUT Board Mechanical Configuration

Oblique View



Pinout

Nomenclature: There is potential for confusion in the signal direction because of the choice between connecting the QSE of one board to the QTE of the second or the QTE of the first to the QSE of the second. The direction is shown as an OUTPUT if it is driven by the HT part that is on the board the QSE connector used in the connection is mounted on. If a host board is connected to a cave, then the host will drive HT_TX_CADp8 (from the chip HT_CADOUTp8) on pin QSE23/QTE138; the cave will receive this on QSE138/QTE23 and connect to HT_CADINp8. Because of the connector rotations this always lines up with the recommended pinout/ballout for an HT chip.

See the section entitled "BIDIR pin: HT control pins and SMBus" for a description of pins 10, 14, 16, 17, 19, 142, 144, 145, 147, and 151.

The proposed pin-out of the DUT connector is as follows:

Table 1
HT DUT Connector

SIGNAL	DIR	QSE pin	QTE pin	QTE pin	QSE pin	DIR	SIGNAL
3.3V	POWER	**1**	**160**	**159**	**2**	POWER	3.3V
3.3V	POWER	**3**	**158**	**157**	**4**	POWER	3.3V
3.3V	POWER	**5**	**156**	**155**	**6**	POWER	3.3V
TDI	INPUT	**7**	**154**	**153**	**8**	OUTPUT	HT_REFCLK100
USERA0/A0'		**9**	**152**	**10**	**10**	JTAG	TMS
USERB0/B0'		**11**	**150**	**149**	**12**		USERC0/C0'
USERD0/D0'		**13**	**148**	**14**	**14**	BIDIR	SMBCLK
USERE0/E0'		**15**	**146**	**16**	**16**	BIDIR	SMBDAT
TRST	JTAG	**17**	**17**	**143**	**18**	GROUND	GND
TCK	JTAG	**19**	**19**	**141**	**20**	OUTPUT	HT_TX_CADp0
GND	GROUND	**21**	**140**	**139**	**22**	OUTPUT	HT_TX_CADn0
HT_TX_CADp8	OUTPUT	**23**	**138**	**137**	**24**	GROUND	GND
HT_TX_CADn8	OUTPUT	**25**	**136**	**135**	**26**	OUTPUT	HT_TX_CADp1
GND	GROUND	**27**	**134**	**133**	**28**	OUTPUT	HT_TX_CADn1
HT_TX_CADp9	OUTPUT	**29**	**132**	**131**	**30**	GROUND	GND
HT_TX_CADn9	OUTPUT	**31**	**130**	**129**	**32**	OUTPUT	HT_TX_CADp2
GND	GROUND	**33**	**128**	**127**	**34**	OUTPUT	HT_TX_CADn2
HT_TX_CADp10	OUTPUT	**35**	**126**	**125**	**36**	GROUND	GND
HT_TX_CADn10	OUTPUT	**37**	**124**	**123**	**38**	OUTPUT	HT_TX_CADp3
GND	GROUND	**39**	**122**	**121**	**40**	OUTPUT	HT_TX_CADn3
HT_TX_CADp11	OUTPUT	**41**	**120**	**119**	**42**	GROUND	GND
HT_TX_CADn11	OUTPUT	**43**	**118**	**117**	**44**	OUTPUT	HT_TX_CLK0p
GND	GROUND	**45**	**116**	**115**	**46**	OUTPUT	HT_TX_CLK0n
HT_TX_CLK1p	OUTPUT	**47**	**114**	**113**	**48**	GROUND	GND
HT_TX_CLK1n	OUTPUT	**49**	**112**	**111**	**50**	GROUND	GND

GND	GROUND	**51**	**110**	**109**	**52**	OUTPUT	HT_TX_CADp4
HT_TX_CADp12	OUTPUT	**53**	**108**	**107**	**54**	OUTPUT	HT_TX_CADn4
HT_TX_CADn12	OUTPUT	**55**	**106**	**105**	**56**	GROUND	GND
GND	GROUND	**57**	**104**	**103**	**58**	OUTPUT	HT_TX_CADp5
HT_TX_CADp13	OUTPUT	**59**	**102**	**101**	**60**	OUTPUT	HT_TX_CADn5
HT_TX_CADn13	OUTPUT	**61**	**100**	**99**	**62**	GROUND	GND
GND	GROUND	**63**	**98**	**97**	**64**	OUTPUT	HT_TX_CADp6
HT_TX_CADp14	OUTPUT	**65**	**96**	**95**	**66**	OUTPUT	HT_TX_CADn6
HT_TX_CADn14	OUTPUT	**67**	**94**	**93**	**68**	GROUND	GND
GND	GROUND	**69**	**92**	**91**	**70**	OUTPUT	HT_TX_CADp7
HT_TX_CADp15	OUTPUT	**71**	**90**	**89**	**72**	OUTPUT	HT_TX_CADn7
HT_TX_CADn15	OUTPUT	**73**	**88**	**87**	**74**	GROUND	GND
GND	GROUND	**75**	**86**	**85**	**76**	OUTPUT	HT_TX_CTL0p
USER_TCTL1p	OUTPUT	**77**	**84**	**83**	**78**	OUTPUT	HT_TX_CTL0n
USER_TCTL1n	OUTPUT	**79**	**82**	**81**	**80**	GROUND	GND
GND	GROUND	**81**	**80**	**79**	**82**	INPUT	USER_RCTL1n
HT_RX_CTL0n	INPUT	**83**	**78**	**77**	**84**	INPUT	USER_RCTL1p
HT_RX_CTL0p	INPUT	**85**	**76**	**75**	**86**	GROUND	GND
GND	GROUND	**87**	**74**	**73**	**88**	INPUT	HT_RX_CADn15
HT_RX_CADn7	INPUT	**89**	**72**	**71**	**90**	INPUT	HT_RX_CADp15
HT_RX_CADp7	INPUT	**91**	**70**	**69**	**92**	GROUND	GND
GND	GROUND	**93**	**68**	**67**	**94**	INPUT	HT_RX_CADn14
HT_RX_CADn6	INPUT	**95**	**66**	**65**	**96**	INPUT	HT_RX_CADp14
HT_RX_CADp6	INPUT	**97**	**64**	**63**	**98**	GROUND	GND
GND	GROUND	**99**	**62**	**61**	**100**	INPUT	HT_RX_CADn13
HT_RX_CADn5	INPUT	**101**	**60**	**59**	**102**	INPUT	HT_RX_CADp13
HT_RX_CADp5	INPUT	**103**	**58**	**57**	**104**	GROUND	GND
GND	GROUND	**105**	**56**	**55**	**106**	INPUT	HT_RX_CADn12
HT_RX_CADn4	INPUT	**107**	**54**	**53**	**108**	INPUT	HT_RX_CADp12
HT_RX_CADp4	INPUT	**109**	**52**	**51**	**110**	GROUND	GND
GND	GROUND	**111**	**50**	**49**	**112**	OUTPUT	HT_RX_CLK1n
GND	GROUND	**113**	**48**	**47**	**114**	OUTPUT	HT_RX_CLK1p
HT_RX_CLK0n	OUTPUT	**115**	**46**	**45**	**116**	GROUND	GND
HT_RX_CLK0p	OUTPUT	**117**	**44**	**43**	**118**	INPUT	HT_RX_CADn11
GND	GROUND	**119**	**42**	**41**	**120**	INPUT	HT_RX_CADp11
HT_RX_CADn3	INPUT	**121**	**40**	**39**	**122**	GROUND	GND
HT_RX_CADp3	INPUT	**123**	**38**	**37**	**124**	INPUT	HT_RX_CADn10
GND	GROUND	**125**	**36**	**35**	**126**	INPUT	HT_RX_CADp10
HT_RX_CADn2	INPUT	**127**	**34**	**33**	**128**	GROUND	GND
HT_RX_CADp2	INPUT	**129**	**32**	**31**	**130**	INPUT	HT_RX_CADn9
GND	GROUND	**131**	**30**	**29**	**132**	INPUT	HT_RX_CADp9
HT_RX_CADn1	INPUT	**133**	**28**	**27**	**134**	GROUND	GND
HT_RX_CADp1	INPUT	**135**	**26**	**25**	**136**	INPUT	HT_RX_CADn8
GND	GROUND	**137**	**24**	**23**	**138**	INPUT	HT_RX_CADp8

HT_RX_CADn0	INPUT	**139**	**22**	**21**	**140**	GROUND	GND
HT_RX_CADp0	INPUT	**141**	**20**	**142**	**142**	BIDIR	LDT_STOP#
GND	GROUND	**143**	**18**	**144**	**144**	BIDIR	PWROK
LDT_REQ#	BIDIR	**145**	**145**	**15**	**146**		USERE1/E1'
RESET#	BIDIR	**147**	**147**	**13**	**148**		USERD1/D1'
USERC1/C1'		**149**	**12**	**11**	**150**		USERB1/B1'
SystemReset#	BIDIR	**151**	**151**	**9**	**152**		USERA1/A1'
HT_REFCLK100I	INPUT	**153**	**8**	**7**	**154**	OUTPUT	TDO
3.3V	POWER	**155**	**6**	**5**	**156**	POWER	3.3V
3.3V	POWER	**157**	**4**	**3**	**158**	POWER	3.3V
3.3V	POWER	**159**	**2**	**1**	**160**	POWER	3.3V

Pin Definitions

BIDIR pins: HT control pins and SMBus

The pins that are marked BIDIR in the table are bi-directional and low speed. These do not share vias between the QSE and QTE connectors. Instead they are put on the same pin number of each, requiring a pcb trace (on each board) between them. (The '161-n' partner of a BIDIR pin is a different BIDIR or JTAG signal.) The host card provides the required pull-ups.

To the first time reader, pins 10, 14, 16, 17, 19, 142, 144, 145, 147, and 151 may appear to be incorrect. They are in fact the optimal way of connecting these seven bi-directional signals and three mis-matched unidirectional signals. It would have possible for these 10 signals to follow the pattern of the other signals by assigning two pins to each of these 10 signals. This would have allowed them to share the vias between the QSE and QTE connectors. This would have reduced the number of USER signals from 20 to 10. It was felt that this was too large of a price to pay.

A useful way to understand the connector system in general and this aspect in particular is to make little paper models. Fold a Post-It note in half and write "Host" on it. Draw a box on the right side and write QSE near it and draw a "1" for pin 1 as per the drawing on page 3. Draw a box on the bottom underneath the QTE and draw a "1" for its pin one as well as shown on page 3. Note that the pin 1's are opposite. Do the same for the Tunnel, Cave, and Switch boards. By playing with these boards, you can get a sense of the mechanical arraignment.

JTAG pins

The pins that are marked JTAG as their direction in the table are driven by the host and received by other boards (in a dual host system one host must be nominated as the master host that drives these, the other host should receive them and act as a cave). Each card may place no more than one load on the signal. Tunnels will connect the signals from one connector to the same on the other connector in addition to putting no more than a single load.

The JTAG TDI/TDO pins follow the normal pattern. A host board will drive its TDO on pin QSE154/QTE7 and receive back on TDI.

A tunnel card will receive TDI on QSE7/QTE154 of one connector-pair will pass the data through its JTAG chain (or part of the chain) and from the last output drive the TDO on the other connector pair. In the other direction the other connector TDI may either be routed directly to the TDO on the first or can go through the rest of the chain. Note that this breaks the symmetry of the tunnel, but since a different JTAG chain description will be needed for every configuration this is not a problem in practice. It is recommended that a tunnel card that may be tested with one of the DUT connector-pairs not connected provide a jumper that can be used to loop the JTAG chain back.

A cave card will receive the JTAG data on TDI on QSE7/QTE154 should connect it to the JTAG chain and the last device drive back on TDO QSE154/QTE7. A cave board that does not use JTAG should loop the TDI directly back to the TDO. Note that implies that the HT link to the cave device under test does not support JTAG connectivity testing, so the tester should take additional care to ensure that there is no mechanical break in the link (e.g. due to a damaged connector).

SMBus Interface

Optionally, the System Management Bus 2.0 (SMBus) may be implemented on the board. This specification can be found at http://www.smbus.org/specs/index.html . This is a two wire control interface. The SMBus pins are BIDIR, so follow the connection rules given above.

SystemReset#

The SystemReset# is an active low reset signal using LVTTL levels. It is bi-directional and has a pullup on the host.

HT_REFCLK100 and HT_REFCLK100I

This is a 100 MHz LVTTL reference clock. This is used as the reference for synchronous HT links. Since the synchronous mode is required by the HT specification it

is recommended that DUT cards make use of this reference. Cards using their own reference should be tagged for asynchronous operation only (which may be acceptable if the final system is using the more convenient asynchronous clocking). At first sight the reference clock is similar to the pins tagged JTAG, in that there is one master signal generated by the host. However given the higher frequency and need for reliable edges, the reference clock needs to be regenerated on each card, thus it is looped through the system.
A host must drive the 100MHz reference derived from the same source as its HT interface clock on the HT_REFCLK100 pin QSE8/QTE153. The HT_REFCLK100I pin is left unconnected. (In a double host configuration that uses synchronous clocking the host that is the master will drive the clock and the host that is the slave will receive the reference on HT_REFCLK100I and must buffer it and drive it to HT_REFCLK100.)

A cave will receive the reference clock on HT_REFCLK100I pin QSE153/QTE8 and should use it as the HT clock reference (alternatively the cave card can be reported as only supporting asynchronous links). The clock should always be buffered and driven out on the HT_REFCLK100 pin QSE8/QTE153.

A tunnel will receive the reference clock on HT_REFCLK100I of one connector and must buffer it and drive to the HT_REFCLK100 of the other connector. And the same in the reverse direction. One of the clocks will also be used as the HT clock reference for synchronous devices. Since it is a frequency (not phase) reference and will be looped back by an end node it does not matter which copy is used. If a tunnel may be tested with one connector-pair unconnected then it is recommended that a jumper be provided to loop back the clock reference.

User Defined Pins
The four User Defined USER_xCTLx1 pins may be used for any purpose that does not affect interoperability. The names were chose to make the operation clear in the optional dual 8 bit mode. An example use would be for a clocking option where there is an alternative which does not use this pin for compliance testing. All outputs must be tri-stated or otherwise disconnected when used for multi-vendor compliance testing.

The other USER defined pairs can either be used to carry BIDIR/JTAG signals, or the directional versions. In high speed directional use USERA0 should share a via to connect to USERA0’ as the OUTPUT and USERA1 should share a via to connect to USERA1’ as the INPUT. In slow speed use USERA0 connects to USERA1’ as one signal, and USERA0’ connects to USERA1 to provide another signal. Similarly for USERB, C and D.

Dual Host Chains

The connector configuration is such that a host card can be rotated 180 degrees and matches with a cave board. This allows double host chains to be constructed. However, some care is needed with the reference clock and signals tagged JTAG. As outlined in the

sections above, one host must be nominated a slave and will receive these signals rather than driving them. A jumper can be used to make this selection (and maybe also to signal to software which is the master host for the configuration algorithm). Clearly, inappropriate setting of this jumper will result in an unstable system so care must be taken when setting up cards for a double-hosted test.

Switch Connections

In general a switch primary port behaves like a cave, and a switch secondary port behaves like a host. JTAG and synchronous clocking is tricky on systems with multiple primary ports because the hosts on all but one primary port must be put for slave operation as far as these signals are concerned but will be a master for the link configuration algorithm.

32 Bit Operation

A 32 bit interface may be supported through the use of two pairs of 16 bit interfaces. Care will have to be taken to minimize the PCB skew between the leads.

Dual 8-Bit Operation

Optionally, it is possible to support two 8 bit interfaces on the connector. The following mapping is used.

1. The 1st 8 bit interface uses xCTL0x, xCAD0-7x, and xCLK0x as normal
2. The 1st 8 bit interface uses the low speed signals as defined in the pinout.
3. The 2nd 8 bit interface uses USER_RCTL1x and USER_RCLT1x as the 2nd CTL leads
4. The 2nd 8 bit interface uses xCAD8-15x as the 2nd xCAD0-7x
5. The 2nd 8 bit interface uses xCLK1 as the 2nd xCLKx
6. The 2nd 8 bit interface uses the USERC0/USERC1' for PWROK, USERC0'/USERC1 for RESET#, USERD0/USERD1' for HT_STOP# and USERD0'/USERD1 for HT_REQ#.
7. The burden of making sure that a 16 bit HT interface is not confused on initialization lies with the interface implementing the dual 8 bit interface. A 16 bit interface that is designed for use with dual 8 bit cards can ground the USERC0/C0'/C1/C1' pins to hold the second link in reset.

Skew

The PCBs should be defined so that the signals that connect to the pins furthest from the pcb edge (i.e. those on odd numbered pins of the QSE connector) have 6.17mm less trace length than those that go to the pins closest to the pcb edge. Thus the signals that are longer on one board will compensate by being shorter on the other For example:

Example 1 - on a Host Bridge board QSE pin 21 will have a 6.17mm shorter trace from it to the Host device than pin 22 does.

Example 2 - on a Cave board, pin 21 on the QTE with which the host QSE mates (i.e.pin 160 of the cave board QSE) will have a 6.17mm longer trace from it to the Cave device than pin 22 does.

The number 6.17mm comes from the distance between the pads specified in the QTE recommended PCB layout in the lower left hand corner of:
http://www.samtec.com/ftppub/pdf/QTE.PDF
The skew of the board with the QSE should be made to match the wider QTE. The QSE width is 5.74mm.

Test Control Interface

Control Interface

10/100 Ethernet is a universal and interoperable control interface. A reasonable choice may be to provide a given DUT board with its own 10/100 port to allow the interface to be configured and simulated from the outside. In addition, the HT interface may be also of course be used for configuration.

Interoperability of test software is outside the scope of this document, but is of course important.

Power Supply Issues

It is assumed that the power supplies are laboratory type, high quality supplies with current capacity sufficient for powering all boards in a given chain. Tunnel boards should connect the power pins between its HT connectors well.

It may be desirable to provide additional power connections to the individual boards, but these are assumed to come from the same power source.

The power supplies should be well decoupled with large and small capacitors distributed within each board.

A recommended connector for bringing additional power to a board is the 4-pin ATX hard drive connector.

There may be power supply sequencing requirements, but these are outside the scope of this document.

It is estimated that each power pin can support 500ma for a total of 6A. This leads to a board power budget of 20W. This figure is rough and should be independently verified.

Mechanical Arrangement

Dimensions

The board shall be no deeper than 110mm when it is desired to use a switch board without cables. The QTE-DP-80 is 93.15 mm long, so this is the minimum sized board.

Keep Out Area

No components should be mounted on either side of the board for the full depth of the board from a distance of 9mm inside of the edge of the board.

Positioning

Pin 1 of the QSE is always toward the top of the board for connectors on the right side of the board and towards the bottom of the board for connectors on the left side of the board. The QTE connector under the board is aligned with the QSE but is rotated 180 degrees so that pin 1 of the QTE is under pin 160 of the QSE.

For Host Bridge boards, the HT connector pair shall be on the right side of the board.

For Tunnel boards, there shall be an HT connector pair on both sides of the board (rotated with respect to each other to obey the rule above).

For Cave boards, the HT connector pair shall be on the left side of the board.

Mounting Holes

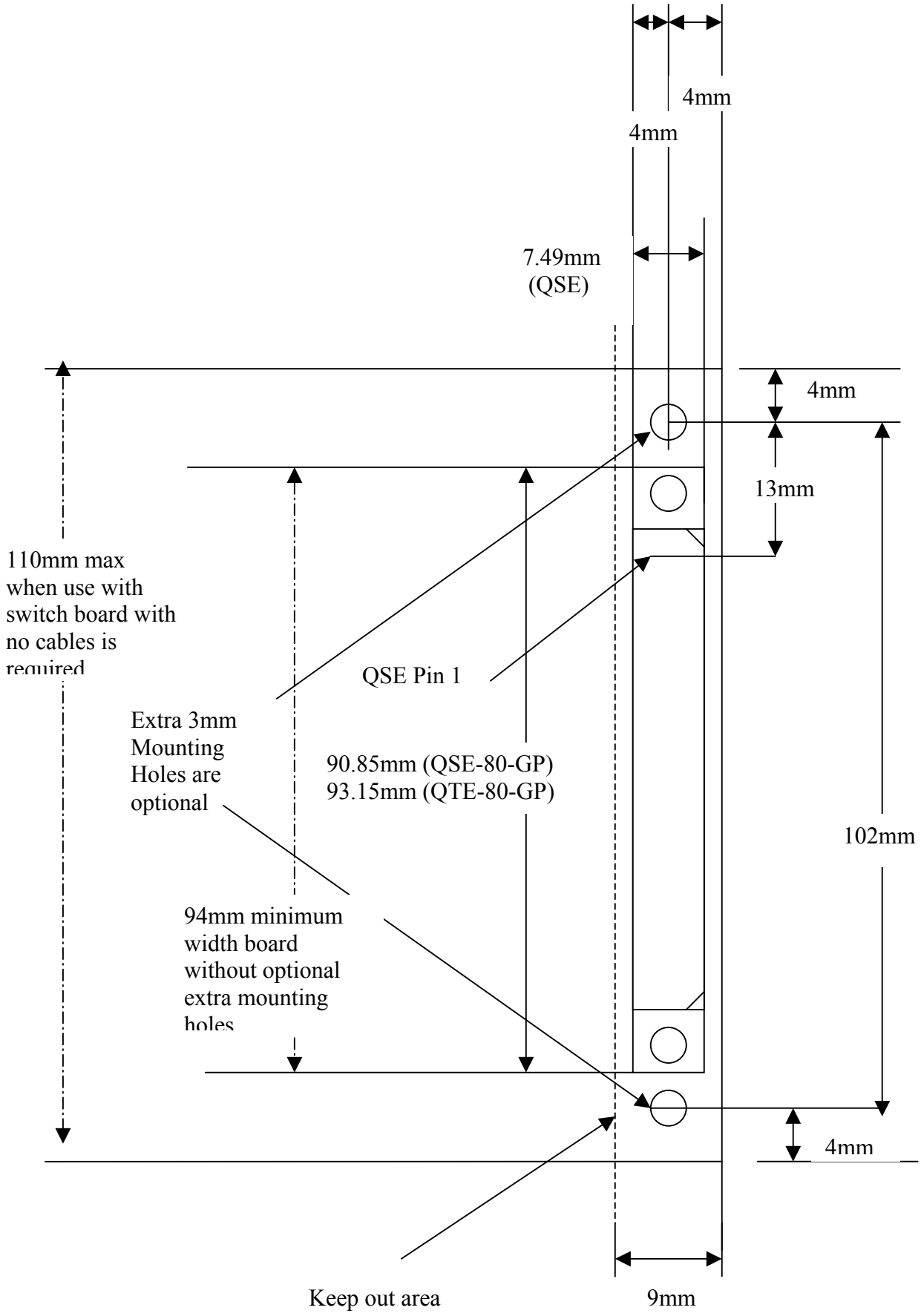
Mounting holes shall be placed at the position shown in the diagrams. These can be used with standoffs and screws to securely fasten the boards to one another.

Width between Mounting Holes

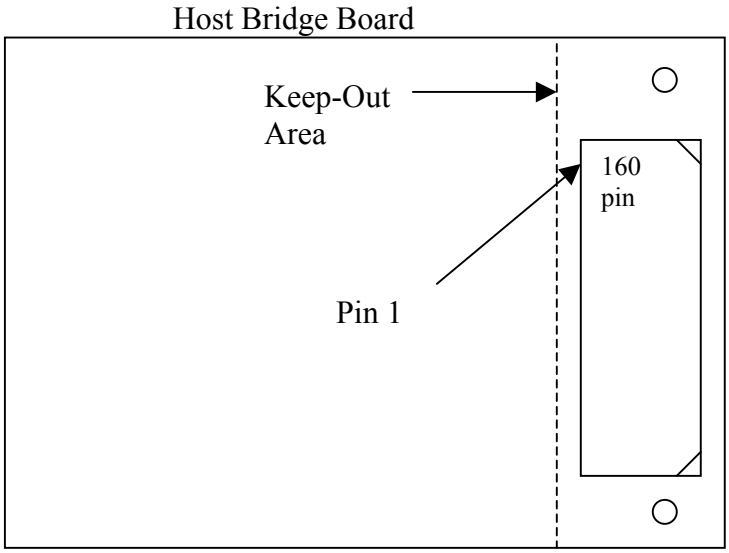
Optionally, the horizontal distance between the mounting holes can be made to be at multiples of 50mm so that a support board can be made to reliably support different width boards.

Use of Non -GP connector

Samtec makes a version of this connector pair without the Guide Posts. This is the QSE/QTE without the –GP suffix. If this connector is used for any reason, a hole or cutout for the post must be provided to allow interoperability. A reason why someone might choose this is to make a board which was slightly narrower than the 93.15 mm length of the QTE-GP allowed to fit into a given form factor.

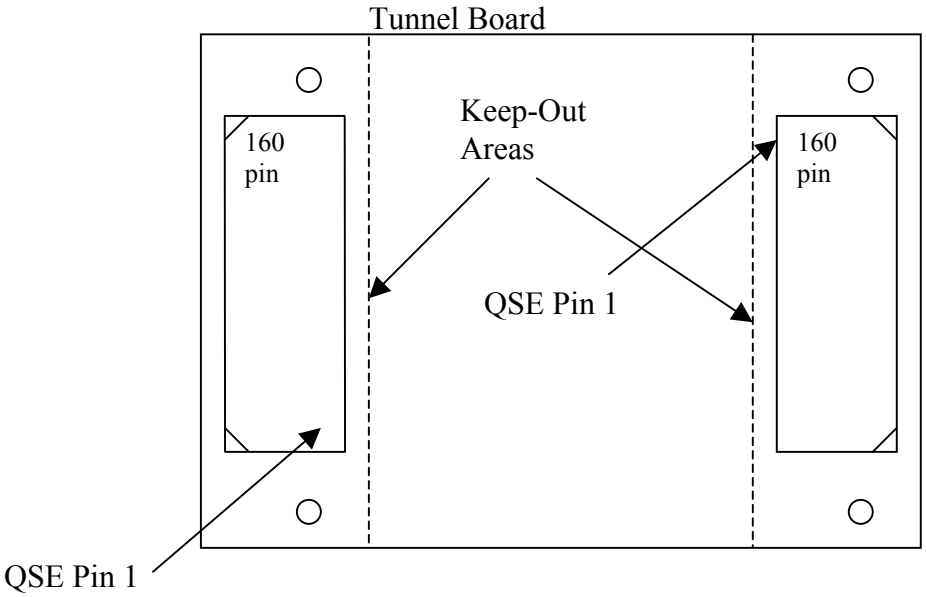

4mm
4mm
7.49mm
(QSE)
4mm
13mm
110mm max
when use with
switch board with
no cables is
required
QSE Pin 1
Extra 3mm
Mounting
Holes are
optional
90.85mm (QSE-80-GP)
93.15mm (QTE-80-GP)
102mm
94mm minimum
width board
without optional
extra mounting
holes
4mm
Keep out area
9mm

Host Bridge Board Diagrams



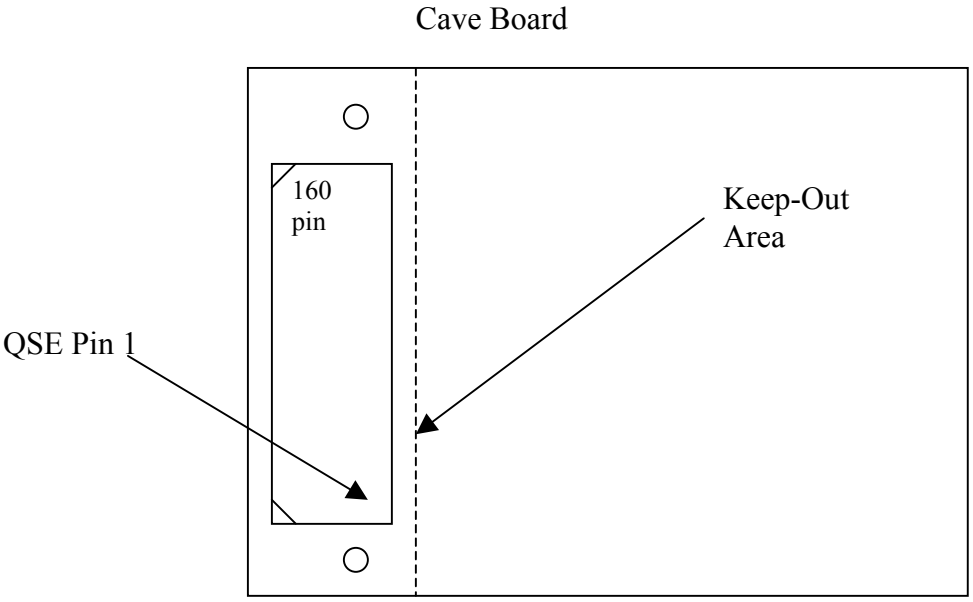
For HT 2.0 operation, only populate the connectors on the top of a normal host bridge board.

Tunnel Board Diagram



For HT 2.0 operation, only populate the connector on the bottom of the tunnel on the side that will connect to a host, and on the top of the side that will connect to a cave or another tunnel. (Note that for full testing of the tunnel two boards must be made to ensure both ports work correctly when towards the host.)

Cave Board Diagrams

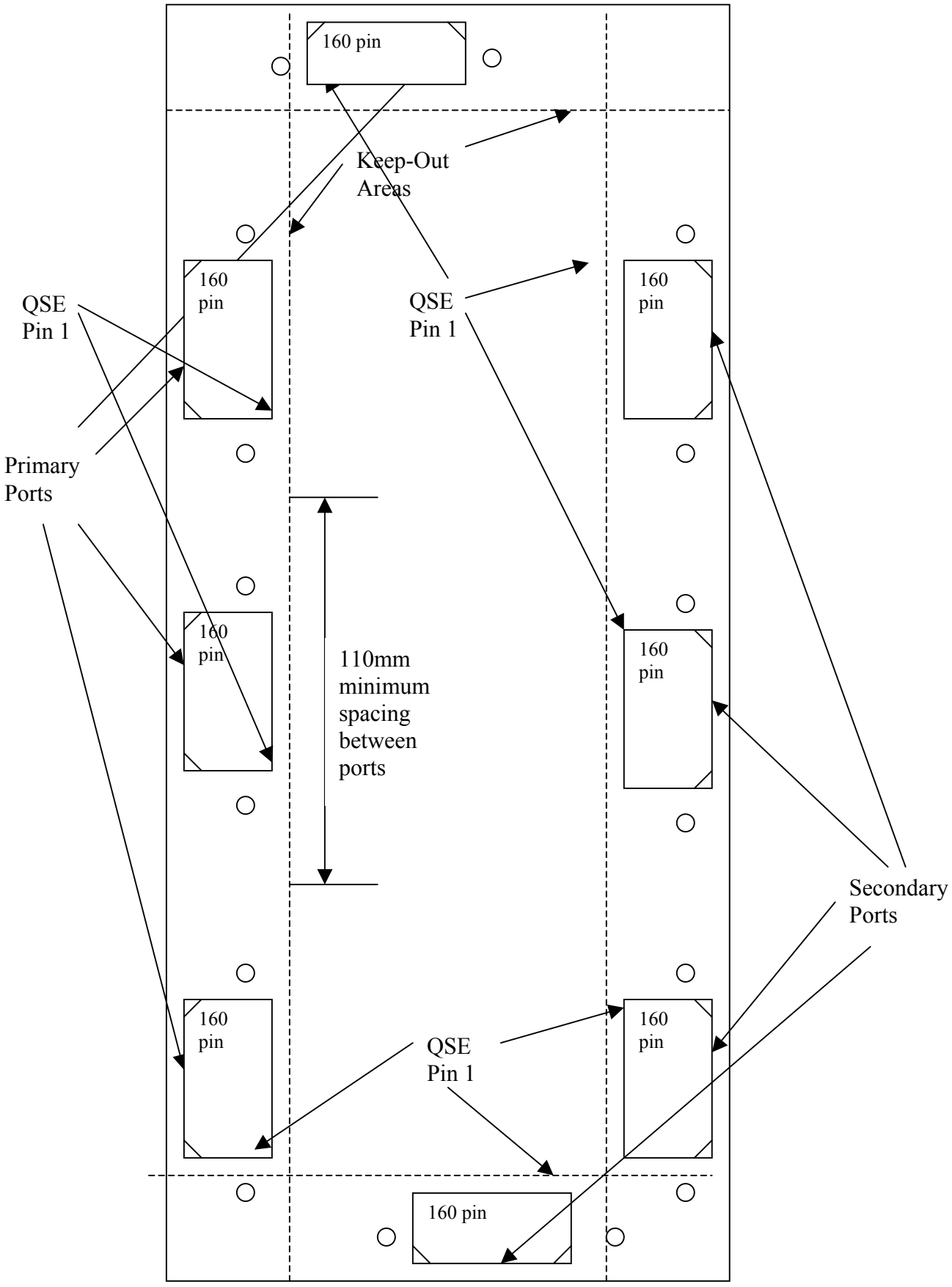


For HT 2.0 operation, only populate the connectors on the bottom of a normal cave board.

Switch Board Diagrams

Switch configurations are more complicated than the other boards because they must allow for different mixes of primary and secondary ports. However, the connector configuration can be the same in either case (a cave is in some sense a rotated host).

For HT 2.0 operation this beautiful symmetry has to be broken, only populate the connectors on the top of a secondary port and the bottom of a primary port.


160 pin
Keep-Out Areas
160 pin
160 pin
QSE Pin 1
QSE Pin 1
Primary Ports
160 pin
160 pin
110mm minimum spacing between ports
Secondary Ports
160 pin
160 pin
QSE Pin 1
160 pin