Principles of the 1-T DRAM Concept on SOI

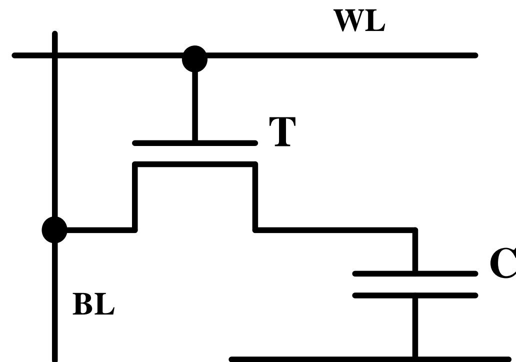
Jean-Michel Sallese, Serguei Okhonin, Pierre Fazan
Mikhail Nagoga

LEG Laboratory, Swiss Federal Institute of Technology, EPFL,
1015 Lausanne, Switzerland

MIXDES 02

Introduction

- **1T/1C DRAM** cell area : $8F^2$ (F: min. feat. size)

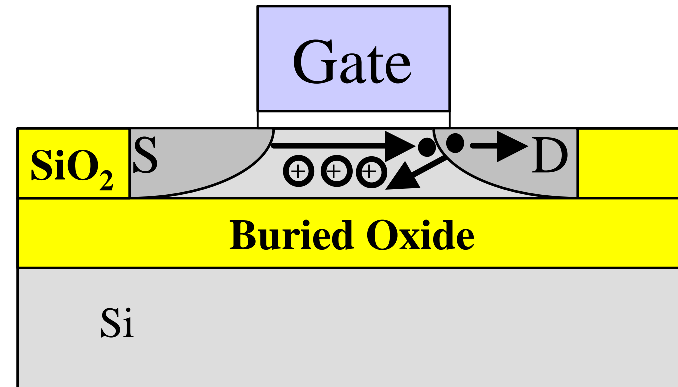


- **Capacitor does not scale** below 100 nm (30 fF)
- **Alternate Memory Solutions**: exotic materials, large cells and complex:
  - **FERAM: 1T / 1 FeCap - MRAM: 1T / 1 MTJ - OUM: 1T / 1 R**
- **Capacitor-less DRAM Cells**: some attempts, still complex:
  - **2T cell on bulk Si or SOI, Tunnel diode.**
- **Objective of this work: a 1T cell**
  - **Use SOI MOSFET's**
  - **Scales with CMOS < 100 nm**

Introduction

- **PD SOI-Mosfet Floating Body Effects:**
  Floating Body Device operation instabilities:
  - ***Kink effect***
  - ***Self heating***
  - Transient effects:
    - **Current overshooting**
    - **Current undershooting**

PD-SOI Nmosfet

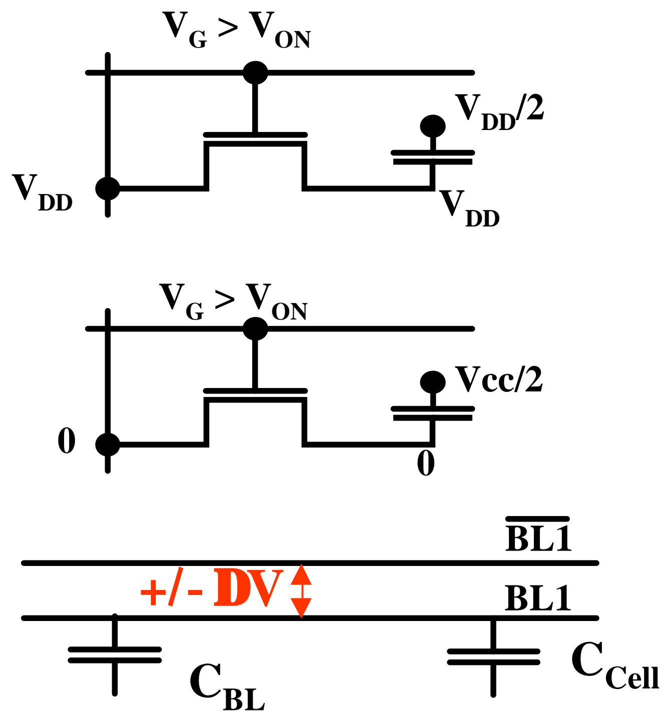


- **1T DRAM**: exploits such effects:
  - **Use SOI body charging to store information.**
  - **Use SOI transistor to read stored information.**

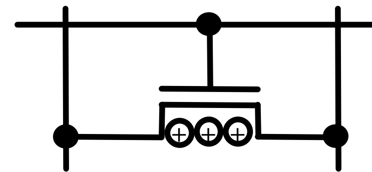
1T-DRAM Concept

- **Store excess of + or - charges in the Body of PD SOI-MOSFETs**
- Use the transistor amplifying mode: **1T Gain Cell**

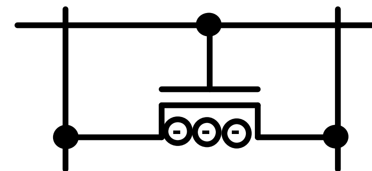
1T/1C-DRAM ***True 1T-DRAM***



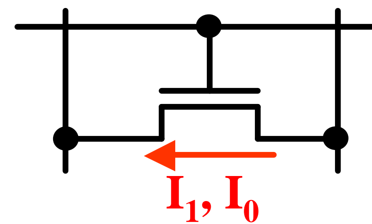
Store “1”



Store “0”



Read by charge sharing



Read by current sensing

1T-DRAM Operation Modes

- ***Samples :***

  0.25 µm PD-SOI N&P MOSFETs from LETI

  0.13 µm PD-SOI N&P MOSFETs from IMEC

- **Data Writing (PD N-mosfet):**

  Write a **“1”** :

  - Channel impact ionization : **excess of holes**

  Write a **“0”** :

  - Forward biasing body junction: **default of holes**

- **Data Reading:**

  Read the information stored by **current sensing**

  Non destructive read

- **Data Refreshing:**

  DRAM= data loss with time

  Refresh operations needed

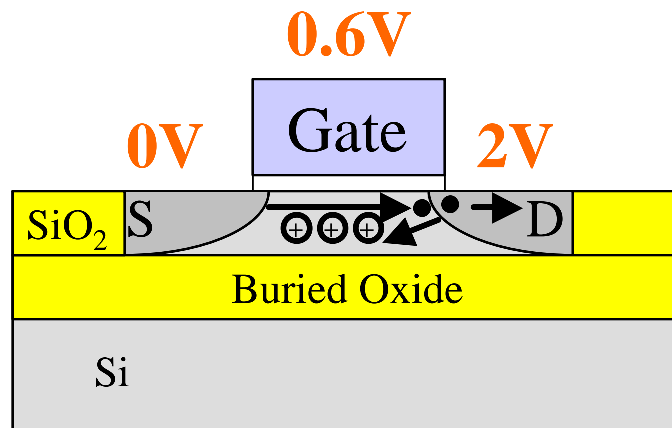
1T-DRAM Operation Modes

- **Writing “1”**
- Use impact ionization mechanism:

Example of voltage for 0.25mm NMOS devices

for writing “1” in 3 ns

PD-SOI NMOS



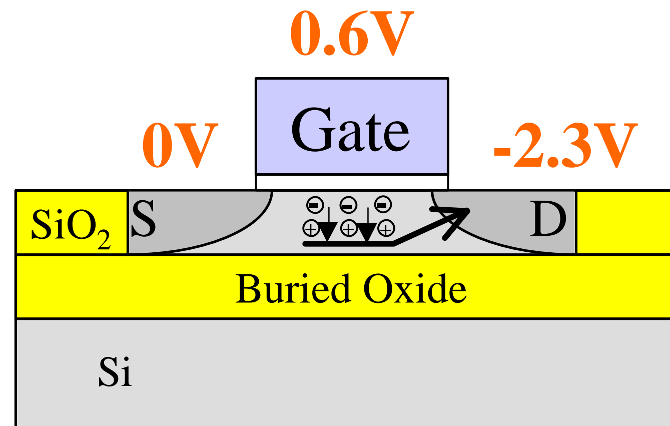
1T-DRAM Operation Modes

- **Writing "0"**
- Use hole removal mechanism:

Example of voltage for 0.25 mm NMOS devices

for writing "0" in 3 ns

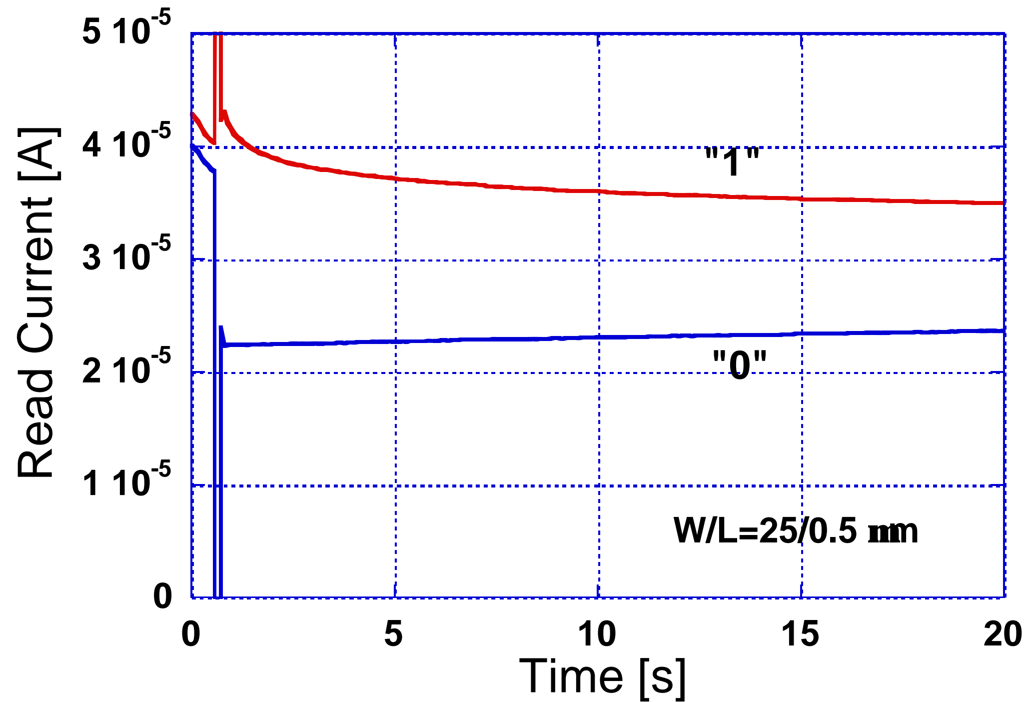
PD-SOI NMOS



1T-DRAM Operation Modes

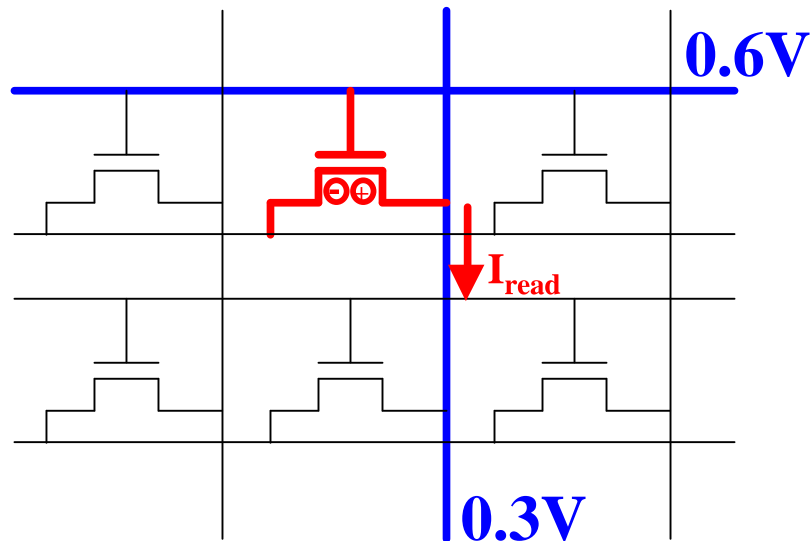
- **Writing "1" & Writing "0"**

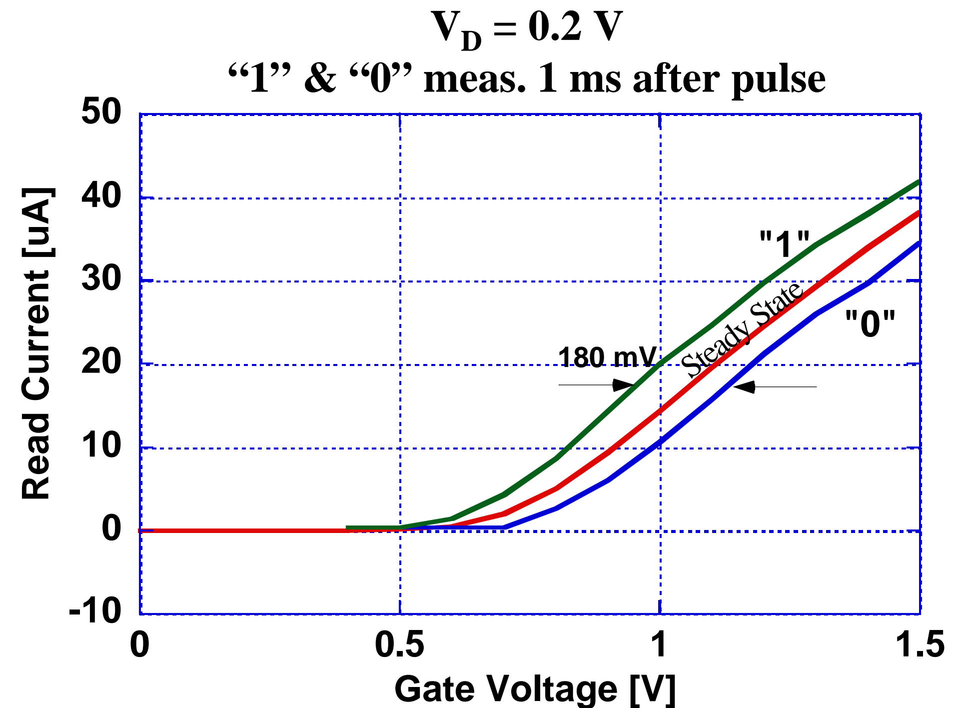
(0.25 μm PD N-mosfet, W/L = 25/0.5 μm)



1T-DRAM Operation Modes

- **Data reading: current sensing**





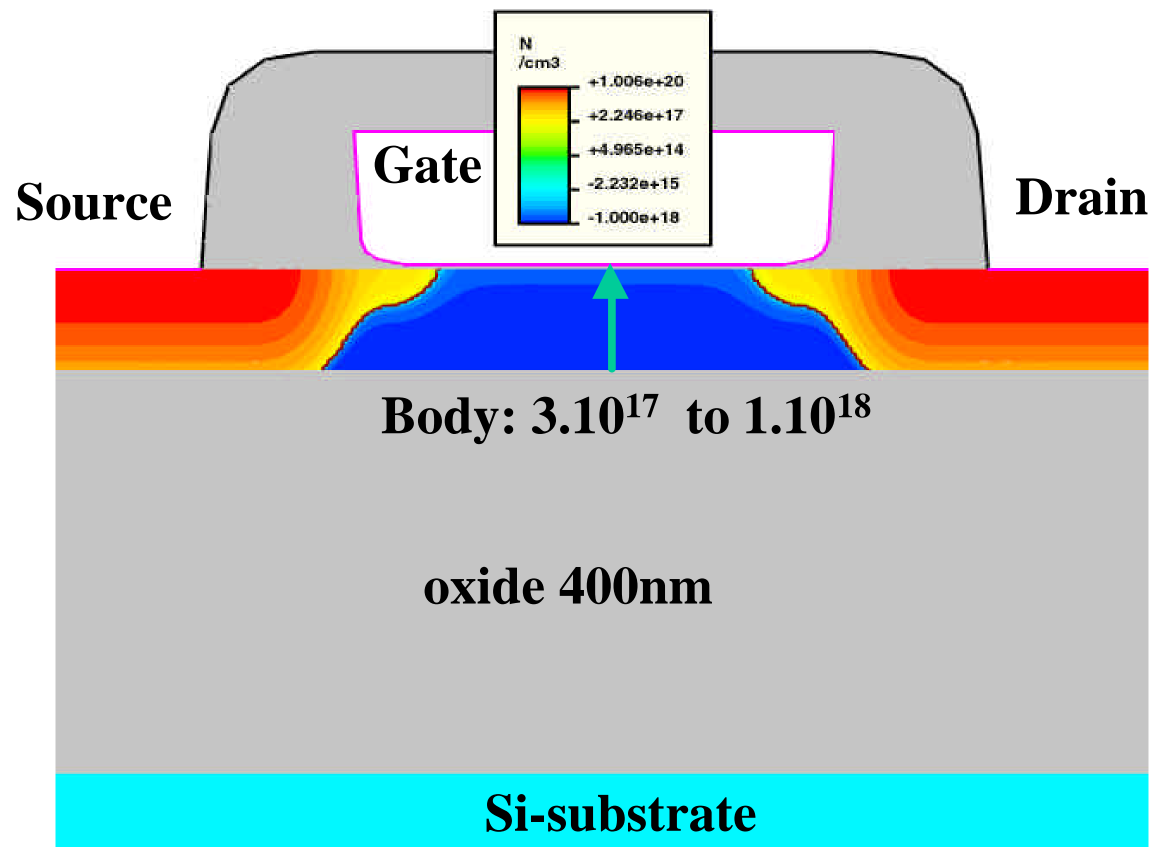
- **Key difference** vs 1T/1C-DRAM:
  - **Non destructive read**
- **But refresh needed:** charge loss due to generations & recombinations

2D Simulation & Mechanisms

Device structure

N-channel FET on SOI (0.3mm)

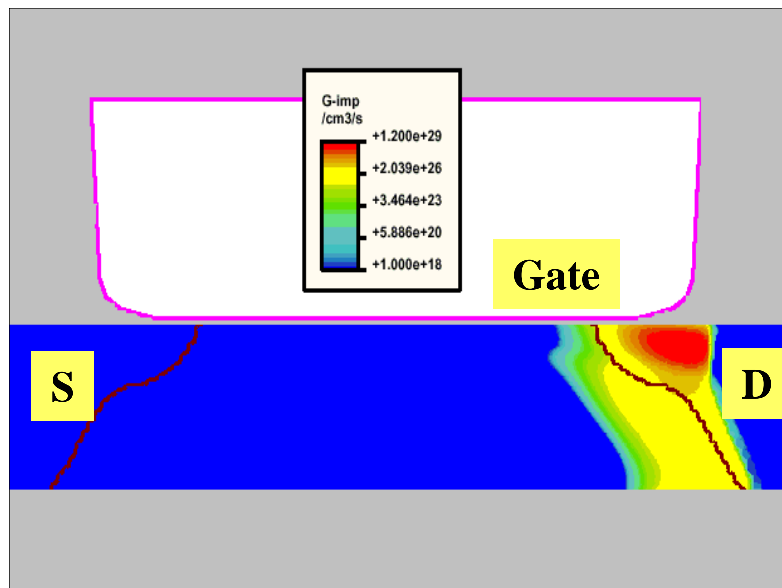
Gate oxide: 4.5nm



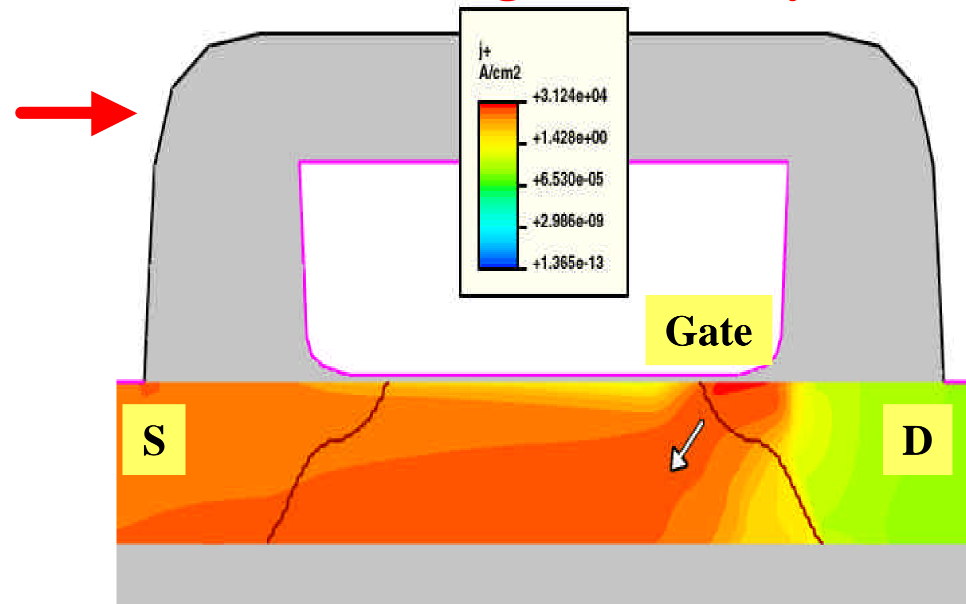
2D Simulation & Mechanisms

During Writing "1" V_G= 0.6V V_S= 0V V_D= 2V

Holes generated by Impact Ionization at high V_D (2V)



Hole Flux due to Impact Ionization: Positive charge in the body



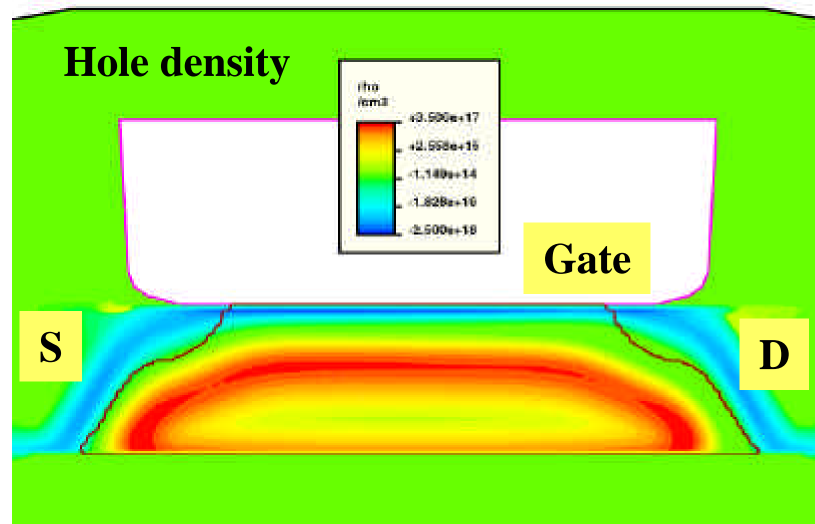
2D Simulation & Mechanisms

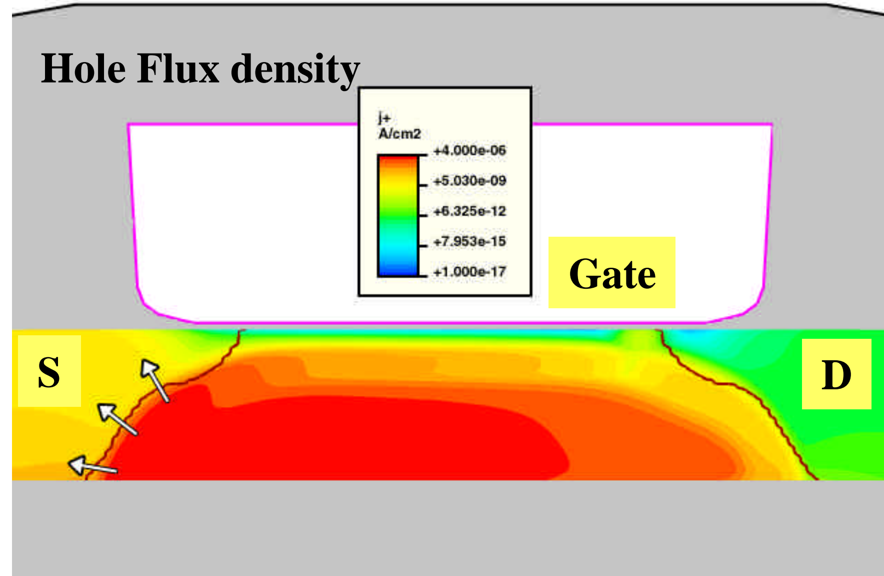
After Writing "1" $V_G = 0.6V$ $V_S = 0V$ $V_D = 0.3V$

Excess of holes in the body

Excess of channel electrons: Drain current increases

…until holes are evacuated through forward junction leakage

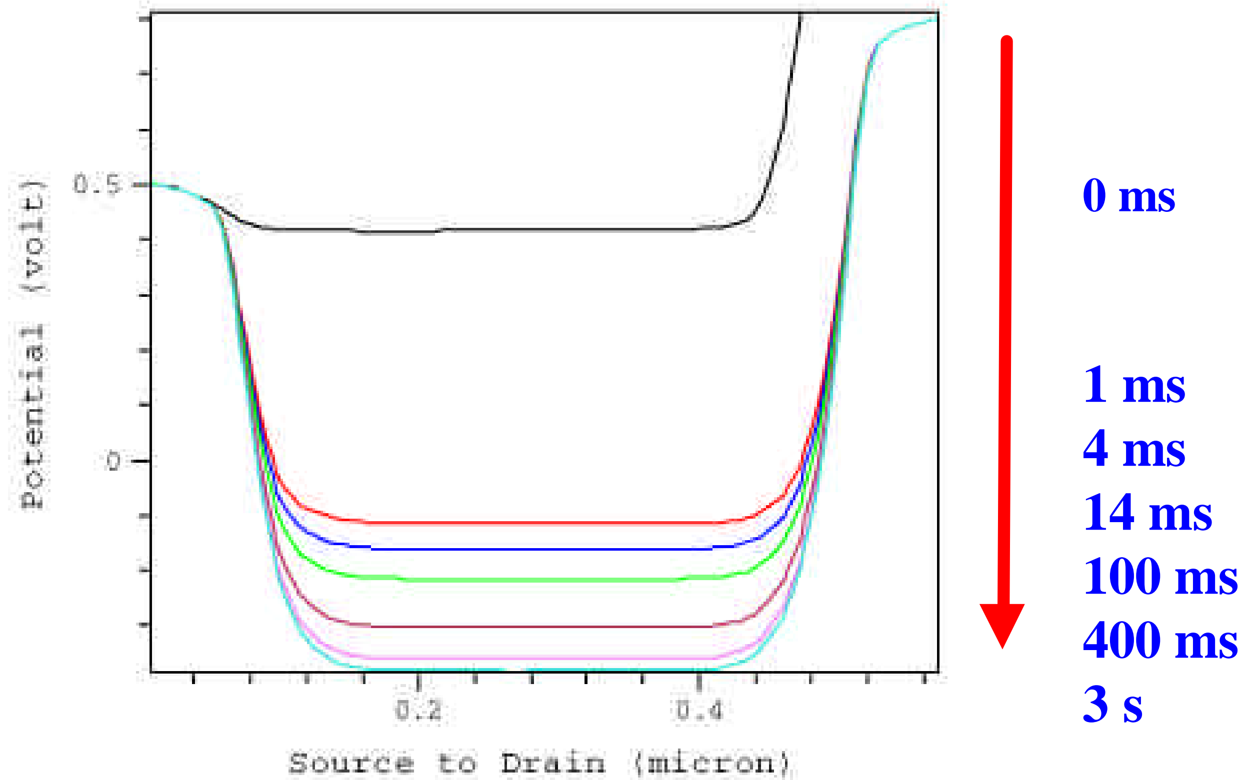




2D Simulation & Mechanisms

After Writing “1”

Decay of the body potential as a function of time after Writing ‘1’

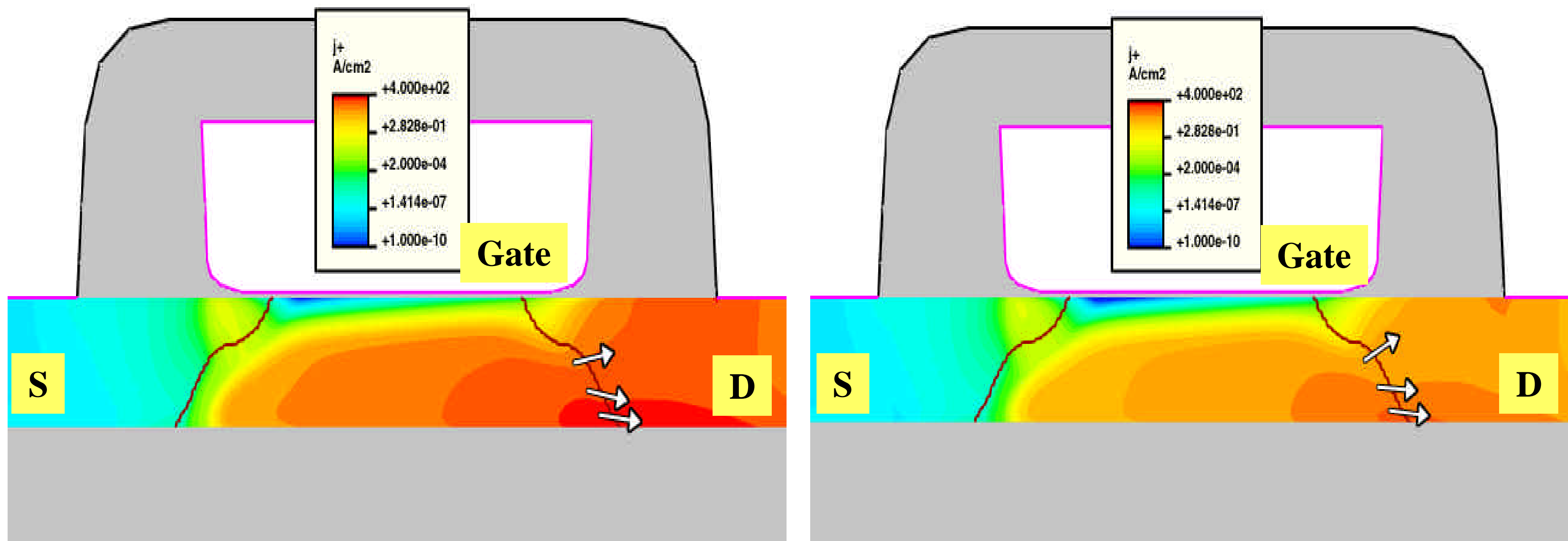


2D Simulation & Mechanisms

During Writing "0" V_G= 0.6V V_S= 0V V_D= -1V

Holes are removed after a few *ns*

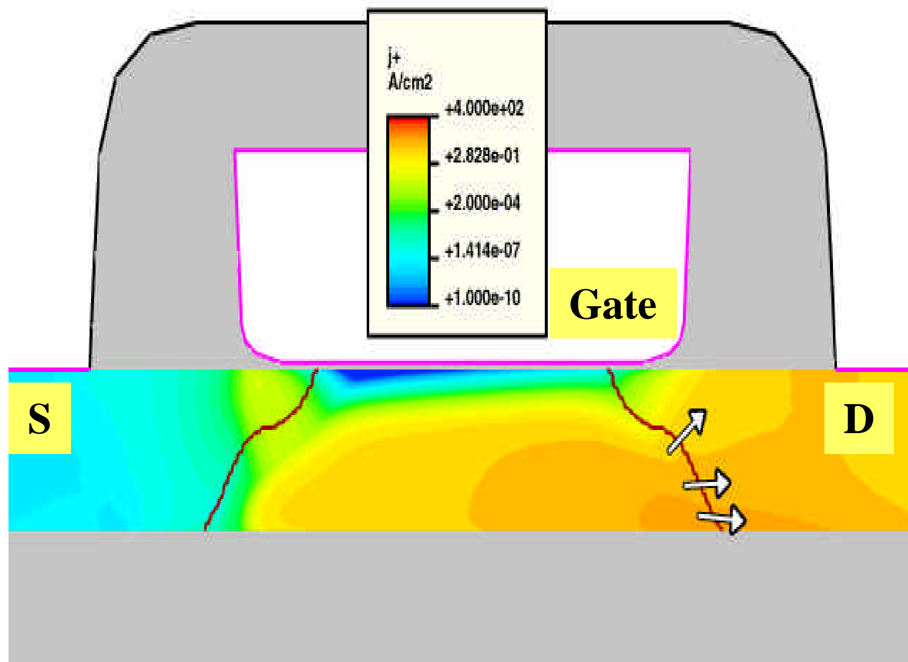
Hole current density after 1 ns **…after 3 ns**



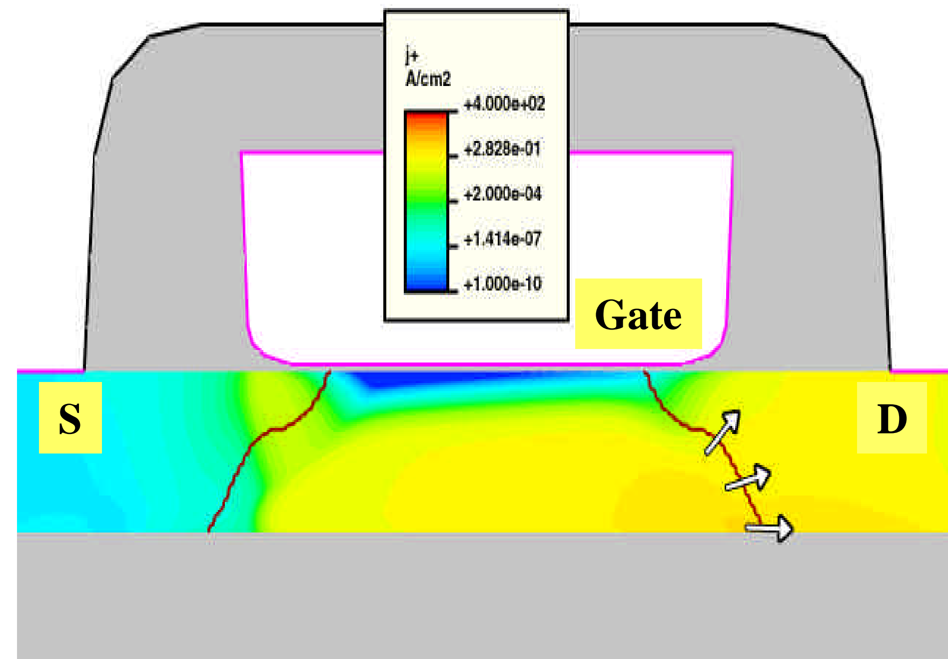
2D Simulation & Mechanisms

During Writing "0"

…after 10 ns



…after 100 ns: *steady state*



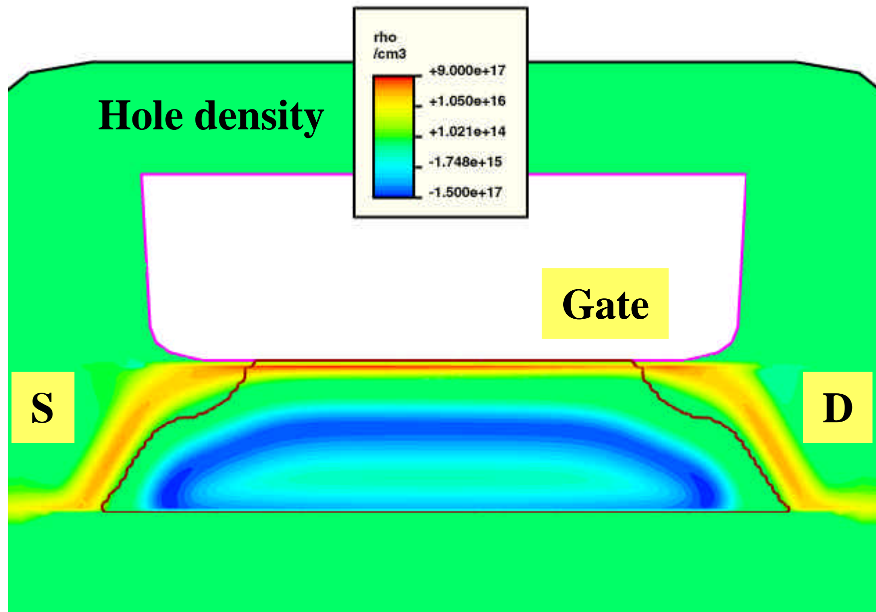
2D Simulation & Mechanisms

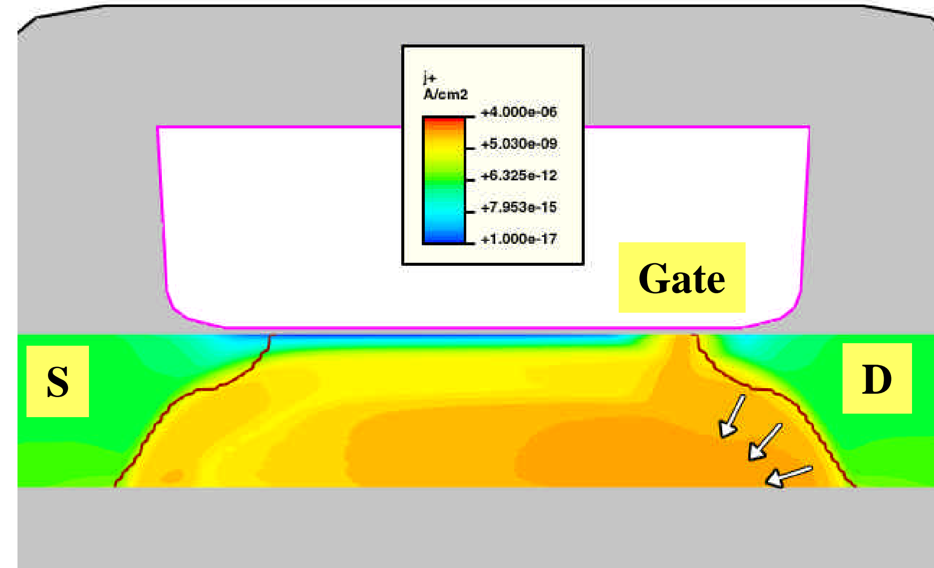
After Writing "0" $V_G = 0.6V$ $V_S = 0V$ $V_D = 0.3V$

Default of holes in the body

Default of channel electrons: Drain current decreases

Reverse junction leakage generates holes in the body

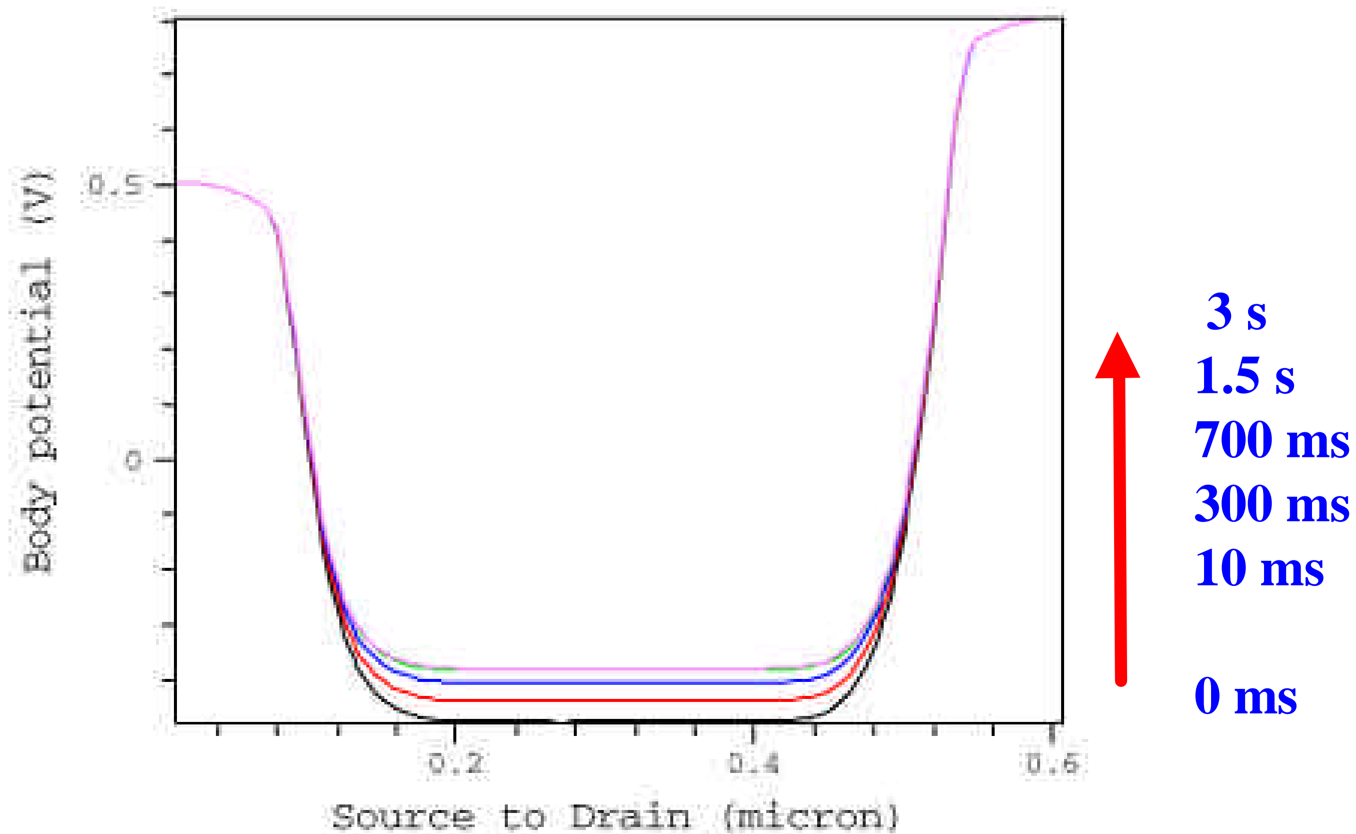




2D Simulation & Mechanisms

After Writing “0”

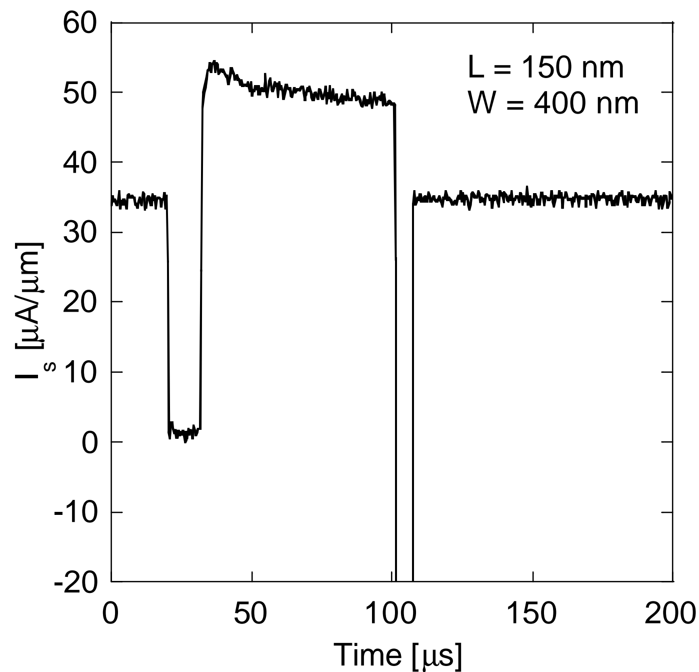
Decay of the body potential as a function of time after Writing ‘0’

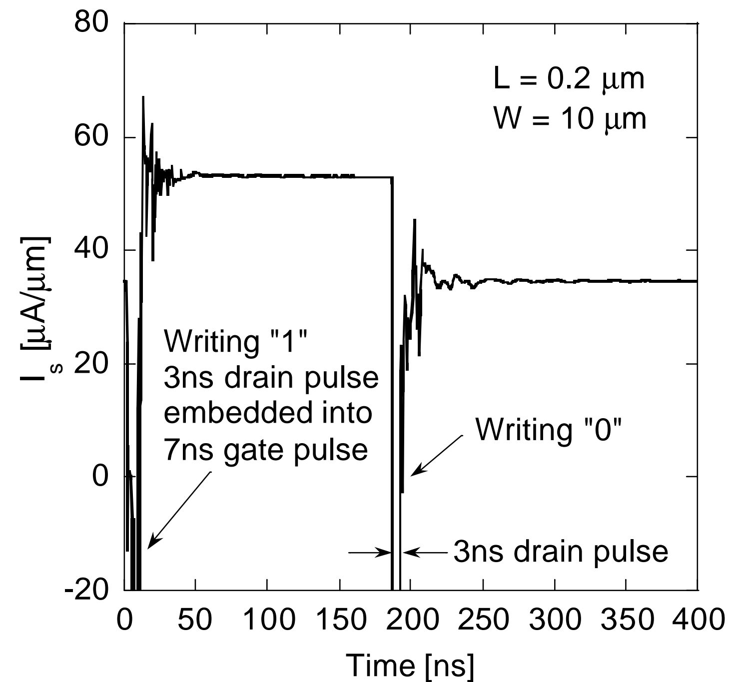


3 s
1.5 s
700 ms
300 ms
10 ms
0 ms

1T-DRAM Cell Scaling

- **Demonstration for small *W/L* and 3 ns operation**
  - High endurance: >10^{15} extrapolated





Conclusion

- 1T/1C-DRAM cells: does not scale below 100 nm
- SOI DRAM = true 1T-DRAM = $4F^2$ cell
- Exploits Floating Body charging of PD SOI-MOSFETs
- No capacitor, no new materials, no additional masks
- Standard CMOS logic or memory process
- Ideal for merged logic/memory SOC applications
- Non destructive read in a refresh interval
- High switching speed: 3 ns demonstrated
- Scalable