Video Electronics Standards Association

TV Panels Standard

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VESA TV Panels Standard

Version 1
March 10, 2006

Purpose

This specification defines the requirements for the standardization of mechanical dimensions and selected electrical interface requirements for 23-, 26-, 32- and 37-inch (wide format) TV panels. The intent of this standard is to help LCD manufacturers and panel consumers to better control panel supply and demand cycles. Panels built to this specification will be able to be used interchangeably without requiring alterations in product tooling for the display module.

Summary

This standard specifies selected mechanical dimensions, electrical interfaces and data formats for 23-, 26-, 32- and 37-inch (wide format) TV panels.

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Preface

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Other Documents Referenced

Note: Versions identified here are current, but users of this standard are advised to ensure they have the latest versions of referenced standards and documents.

Source	Name	Version / Date
TIA/EIA-644	Electrical Characteristics of Low-Voltage Differential Signaling (LVDS) Interface Circuits	March 1, 1996

Table 1 - Reference Documents

Support for this Standard

Clarifications and application notes to support this standard may be written. To obtain the latest standard and any support documentation, contact VESA.

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Acknowledgements

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Table 2 - Acknowledgements

Revision History

March 10, 2006 --- Initial release of the standard

1 Overview

1.1 Summary

This document defines the electrical interface requirements and mechanical dimensions for industry compatible 23-, 26-, 32- and 37-inch (wide format) TV panels.

1.2 Standard Objectives

To define selected electrical interface requirements and mechanical dimensions for industrial compatible TV panels (wide format) in sizes 23-, 26-, 32- and 37-inches. Target pixel formats are 1366 x 768 and 1920 x 1080.

2 Selected Electrical Interface Requirements

The panel interface to the system includes two different physical interfaces: LVDS for data and the inverter interface for backlight.

a. Pixel formatting
b. LVDS signal interface
c. LVDS data/color mapping
d. Power sequencing
e. Backlight electrical interface

These requirements are described in the following sections.

3 Pixel Formatting

Figure 3-1 shows pixel formatting for the active display area.

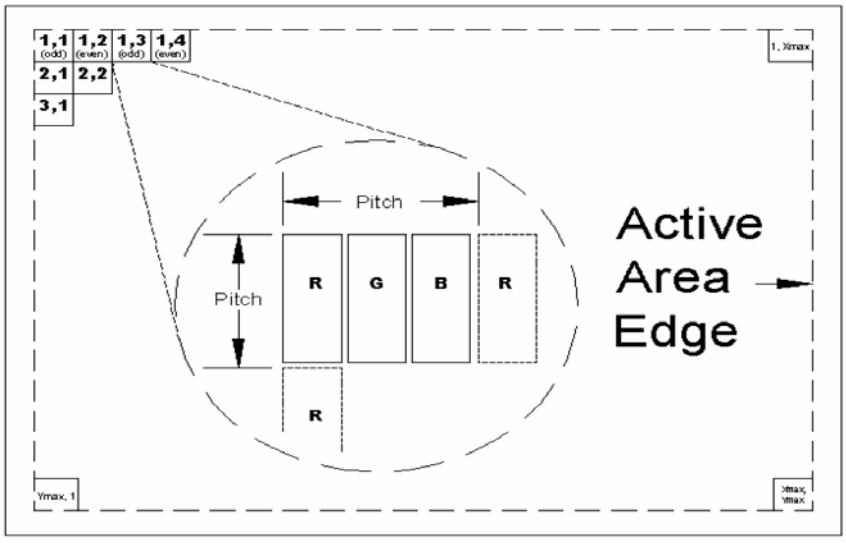


Figure 3-1 - Pixel Formatting

4 LVDS signal interface

The connector keep-out area shall be designed to support insertion of either a wire-crimp style connector or the wider flex-cable style connector. All connectors need to have locking mechanism.

The LVDS differential signal line-to-line termination, Z_T, shall be 100±10 ohm.

There are two different sets of standardized pin-outs for 5V and 12V panels.

Pin 1 location of the LVDS connector is at the left hand side (bottom view of panel). Refer to mechanical drawing for details.

The interface is listed in Table 3 for 5V panels and in Table 4 for 12V panels.

Table 3 - LVDS interface pinout and connector for 5V panels

	WXGA 8-bit	WXGA 10-bit (or 8bit)	F-HD 8-bit	F-HD 10-bit
Format →	1366 x 768	1366 x 768	1920 x 1080	1920 x 1080
Connector →	FI-E30S	FI-RE41S-HF	FI-RE51S-HF	FI-RE51S-HF
Pins →	30	41	51	51
Pin #				
1	Reserved	VDD (5V)	VDD (5V)	VDD (5V)
2	Reserved	VDD	VDD	VDD
3	Reserved	VDD	VDD	VDD
4	GND	VDD	VDD	VDD
5	Rx0-	VDD	VDD	VDD
6	Rx0+	GND	GND	GND
7	GND	GND	GND	GND
8	Rx1-	GND	GND	GND
9	Rx1+	GND	GND	GND
10	GND	GND	RO0-	RO0-
11	Rx2-	RO0-	RO0+	RO0+
12	Rx2+	RO0+	RO1-	RO1-
13	GND	GND	RO1+	RO1+
14	RxCLK-	RO1-	RO2-	RO2-
15	RxCLK+	RO1+	RO2+	RO2+
16	GND	GND	GND	GND
17	Rx3-	RO2-	ROCLKIN-	ROCLKIN-
18	Rx3+	RO2+	ROCLKIN+	ROCLKIN+
19	GND	GND	GND	GND
20	Reserved	ROCLKIN-	RO3-	RO3-
21	LVDS_SEL	ROCLKIN+	RO3+	RO3+
22	Reserved	GND	NC	RO4-
23	GND	RO3-	NC	RO4+
24	GND	RO3+	GND	GND
25	GND	GND	RE0-	RE0-
26	VLCD (5V)	RO4- (NC for	RE0+	RE0+
27	VLCD	RO4+ (NC for	RE1-	RE1-
28	VLCD	GND	RE1+	RE1+
29	VLCD	Reserved	RE2-	RE2-
30	VLCD	Reserved	RE2+	RE2+
31		Reserved	GND	GND
32		Reserved	RECLKIN-	RECLKIN-
33		Reserved	RECLKIN+	RECLKIN+
34		Reserved	GND	GND
35		Reserved	RE3-	RE3-
36		Reserved	RE3+	RE3+

37	Reserved	NC	RE4-
38	Reserved	NC	RE4+
39	Reserved	GND	GND
40	Reserved	Reserved	Reserved
41	Reserved	Reserved	Reserved
42		Reserved	Reserved
43		Reserved	Reserved
44		Reserved	Reserved
45		Reserved	Reserved
46		Reserved	Reserved
47		Reserved	Reserved
48		Reserved	Reserved
49		Reserved	Reserved
50		Reserved	Reserved
51		Reserved	Reserved

Notes:
LVDS_SEL : N.C. – Normal (NS) color mapping
LVDS_SEL and other control: 3.3V CMOS logic level.
Reserved pins usage is manufacturer dependent; default N.C. when not used.

Table 4 - LVDS interface pinout and connector for 12V panels

	WXGA 8-bit	WXGA 10-bit	F-HD 8-bit	F-HD 10-bit
Format →	1366 x 768	1366 x 768	1920 x 1080	1920 x 1080
Connector	FI-X*30SSL-HF**	FI-RE51S-HF	FI-RE51S-HF	FI-RE51S-HF
Pins →	30	51	51	51
Pin #				
1	VLCD (+12V)	GND	GND	GND
2	VLCD (+12V)	Reserved	Reserved	Reserved
3	VLCD (+12V)	Reserved	Reserved	Reserved
4	VLCD (+12V)	Reserved	Reserved	Reserved
5	GND	Reserved	Reserved	Reserved
6	GND	Reserved	Reserved	Reserved
7	GND	LVDS_SEL	LVDS_SEL	LVDS_SEL
8	GND	Reserved	Reserved	Reserved
9	LVDS_SEL	Reserved	Reserved	Reserved
10	Reserved	Reserved	Reserved	Reserved
11	GND	GND	GND	GND
12	RO0-	RO0-	RO0-	RO0-
13	RO0+	RO0+	RO0+	RO0+
14	GND	RO1-	RO1-	RO1-
15	RO1-	RO1+	RO1+	RO1+
16	RO1+	RO2-	RO2-	RO2-
17	GND	RO2+	RO2+	RO2+

18	RO2-	GND	GND	GND
19	RO2+	ROCLKIN-	ROCLKIN-	ROCLKIN-
20	GND	ROCLKIN+	ROCLKIN+	ROCLKIN+
21	ROCLK-	GND	GND	GND
22	ROCLK+	RO3-	RO3-	RO3-
23	GND	RO3+	RO3+	RO3+
24	RO3-	RO4-	N.C.	RO4-
25	RO3+	RO4+	N.C.	RO4+
26	GND	GND	GND	GND
27	Reserved	GND	GND	GND
28	Reserved	N.C.	RE0-	RE0-
29	GND	N.C.	RE0+	RE0+
30	Reserved	N.C.	RE1-	RE1-
31		N.C.	RE1+	RE1+
32		N.C.	RE2-	RE2-
33		N.C.	RE2+	RE2+
34		GND	GND	GND
35		N.C.	RECLKIN-	RECLKIN-
36		N.C.	RECLKIN+	RECLKIN+
37		GND	GND	GND
38		N.C.	RE3-	RE3-
39		N.C.	RE3+	RE3+
40		N.C.	N.C.	RE4-
41		N.C.	N.C.	RE4+
42		GND	GND	GND
43		GND	GND	GND
44		GND	GND	GND
45		GND	GND	GND
46		GND	GND	GND
47		N.C.	N.C.	N.C.
48		VLCD (+12V)	VLCD (+12V)	VLCD (+12V)
49		VLCD	VLCD	VLCD
50		VLCD	VLCD	VLCD
51		VLCD	VLCD	VLCD

5 LVDS Data/Color Mapping

- The default color mapping is NS (Normal) mode for both 8 bit and 10 bit panels.
- Figure 5-1 shows the LVDS Data Color Mapping for a 8-bit 1080p panel. Dual LVDS channels are used to support 1080p mode.
- For WXGA (1366x768) panels, a single LVDS channel is used with only the ODD channel and the mapping shown in Figure 5-2
- Figure 5-3 shows the LVDS Data Color Mapping for a 10-bit 1080p (dual channel) panel.
- Figure 5-4 shows the LVDS Data Color Mapping for a 10-bit WXGA (single channel) panel.
- Figure 5-5 shows the timing diagram for DE, HS and VS.

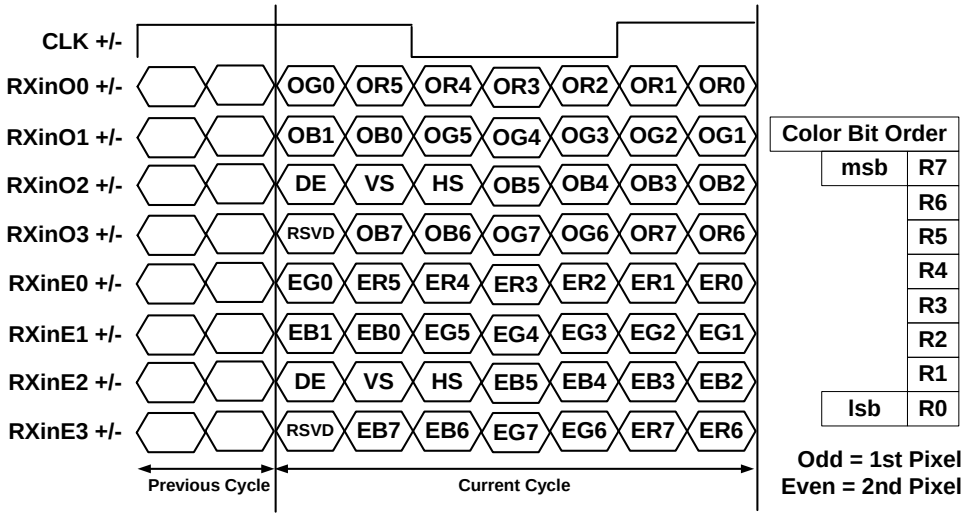


Figure 5-1 - LVDS Data/Color Mapping for Dual Channel, 8-bit panel

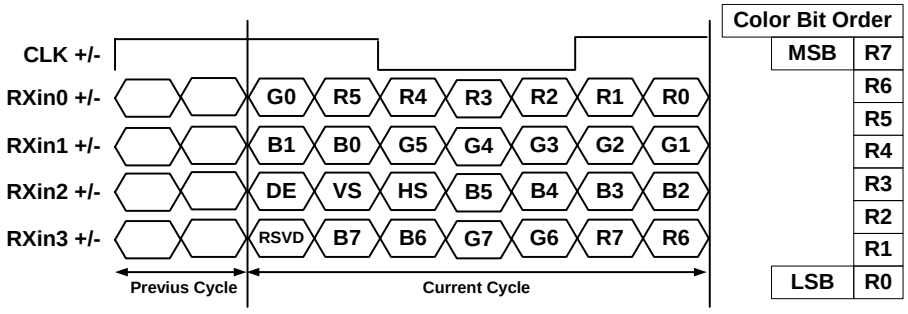


Figure 5-2 - LVDS Data/Color Mapping for Single Channel, 8-bit panel

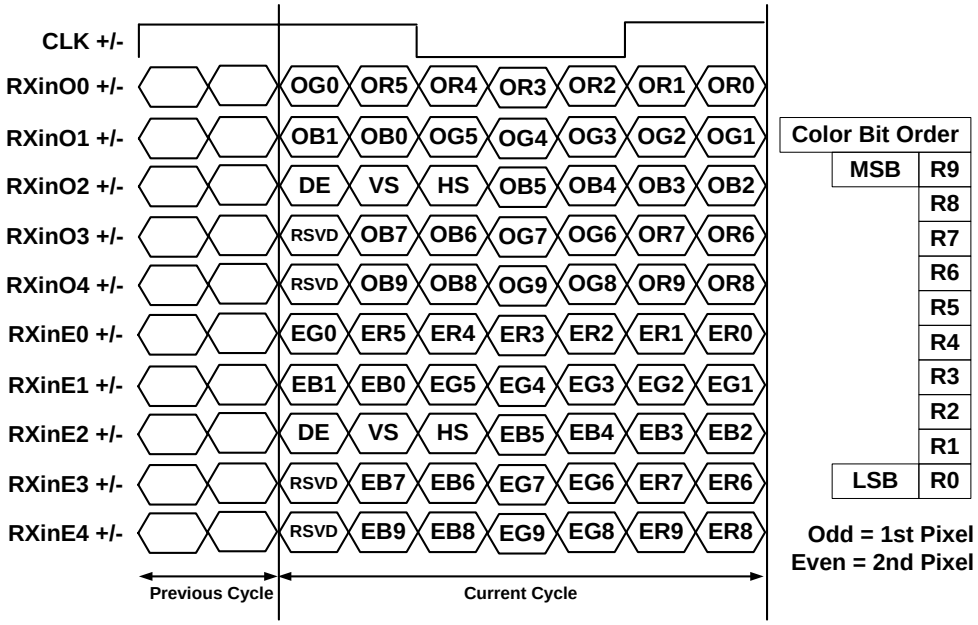


Figure 5-3 - LVDS Data/Color Mapping for Dual Channel, 10-bit panel

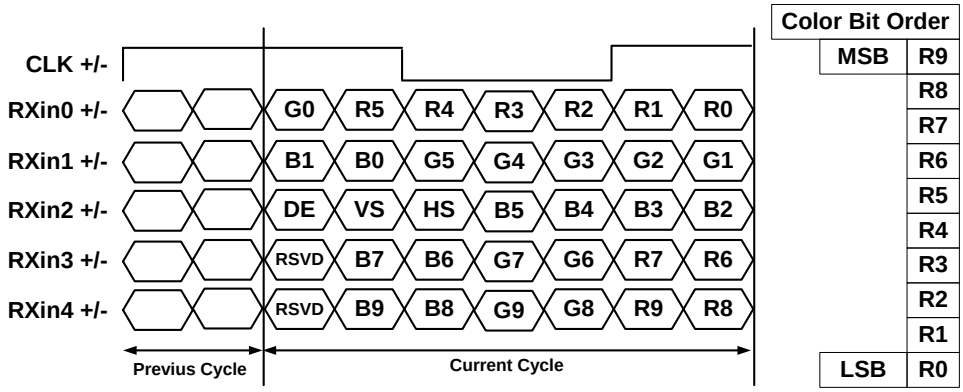


Figure 5-4 - LVDS Data/Color Mapping for Single Channel, 10-bit panel

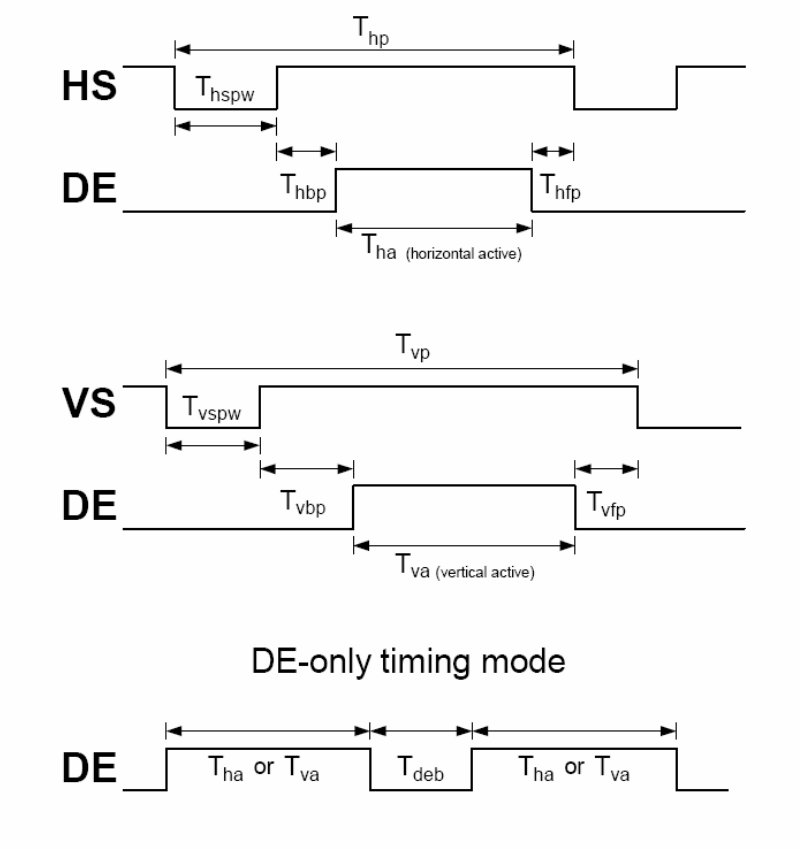


Figure 5-5 - Timing Diagram for DE, HS and VS

6 Power Sequencing

Power sequencing is shown below

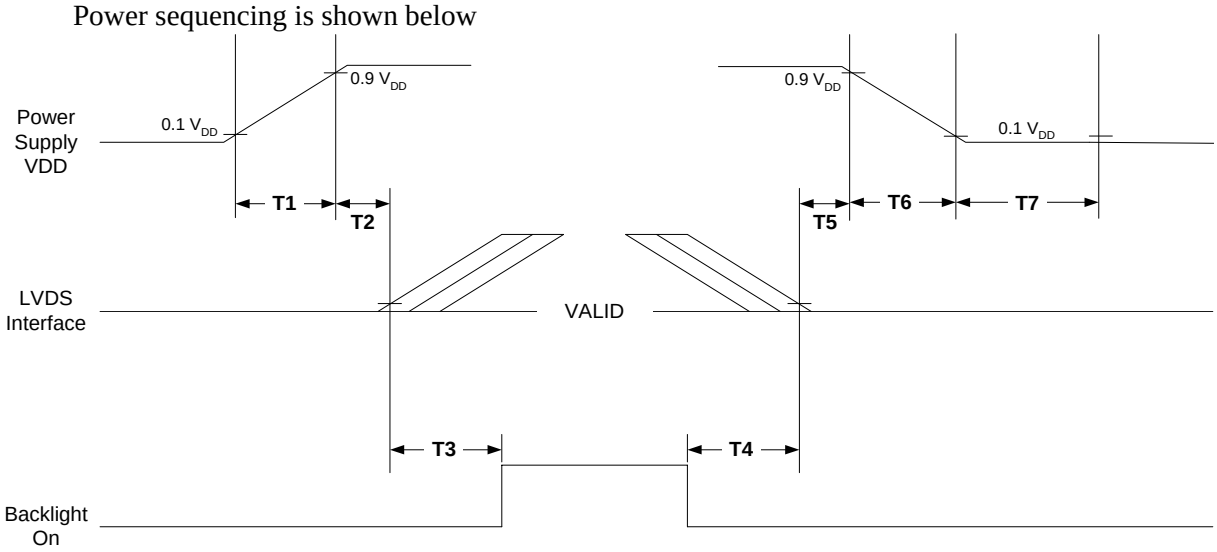


Figure 6-1 – TV Power-Up Sequence Timing

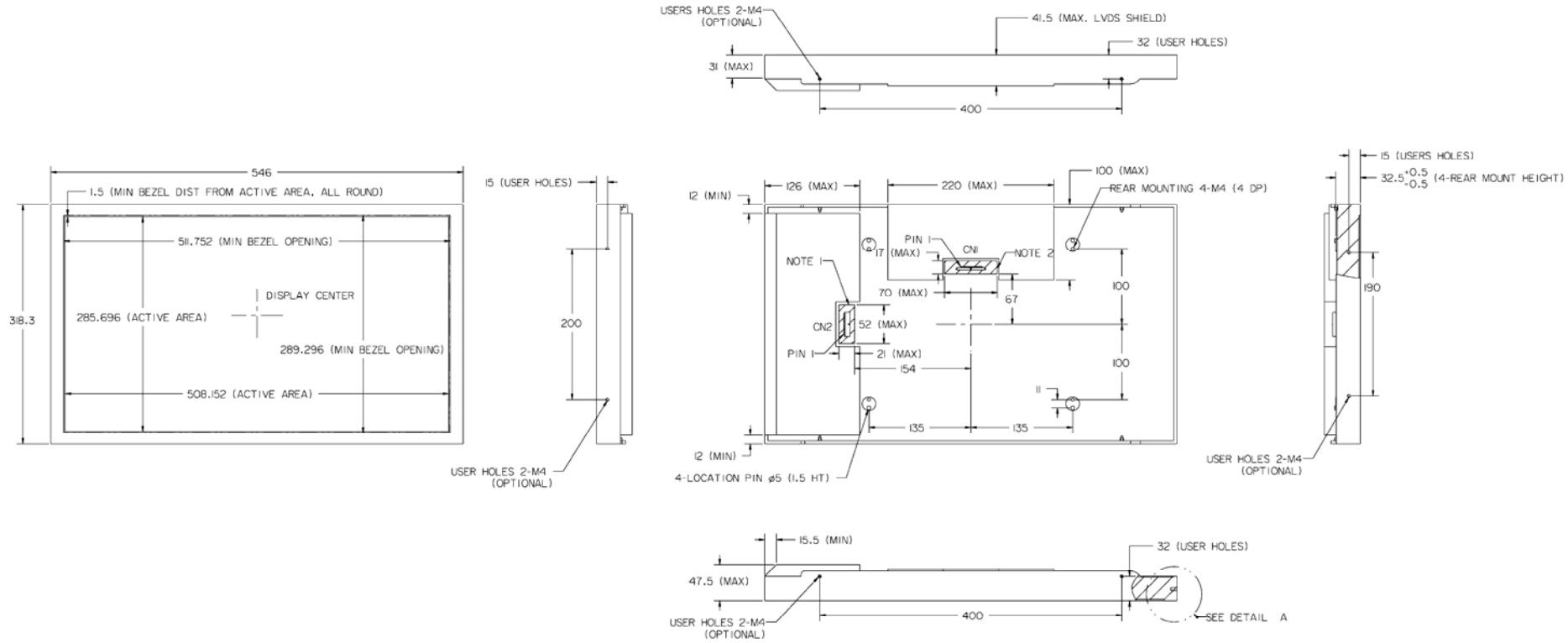
Table 5 - TV Power-Up Timing Parameters

	Minimum time (ms)	Maximum time (ms)
T1	0.5	10
T2	0.5	50
T3	1000	-
T4	200	-
T5	0.5	50
T6	0.01	10
T7	1000	-

Note: T7 is measured after module is fully discharged.

7 Mechanical Drawings[1]

7.1 23" Mechanical Drawing

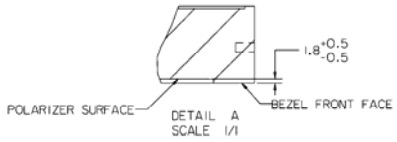


DIAGONAL : 23"
ACTIVE AREA : 508.15 (H) x 285.69 (V)
RESOLUTION : 1366 x 768
PIXEL SIZE : 0.372(h) x 0.372(w)

5 VOLTS PANEL
CN1: FI-E30S (JAE OR EQUIVALENT)
CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)

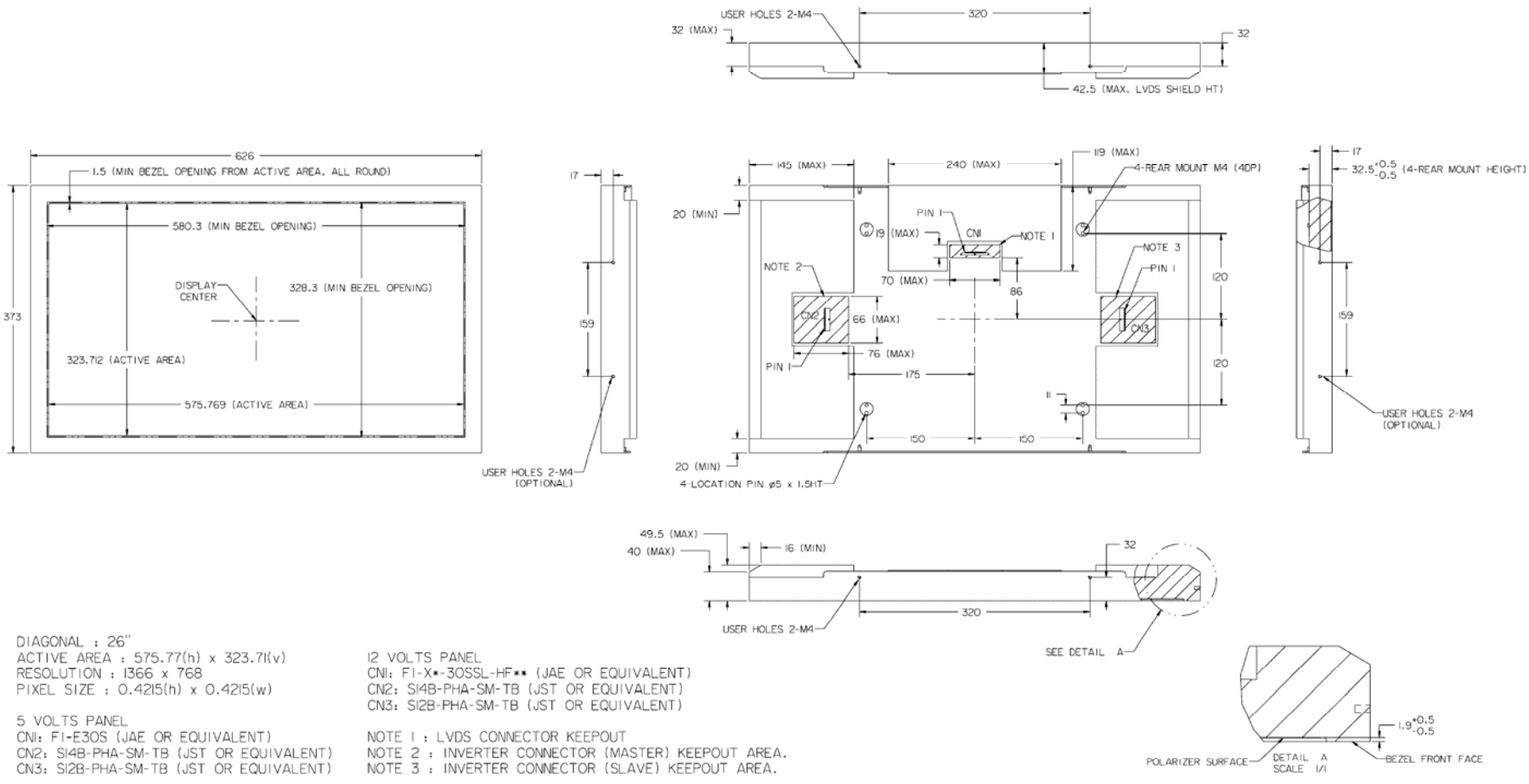
12 VOLTS PANEL
CN1: FI-X**-30SSL-HF** (JAE OR EQUIVALENT)
CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)

NOTE 1 : LVDS CONNECTOR KEEPOUT AREA
NOTE 2 : INVERTER CONNECTOR KEEPOUT AREA.



[1] All dimensions in mm.

7.2 26” Mechanical Drawing



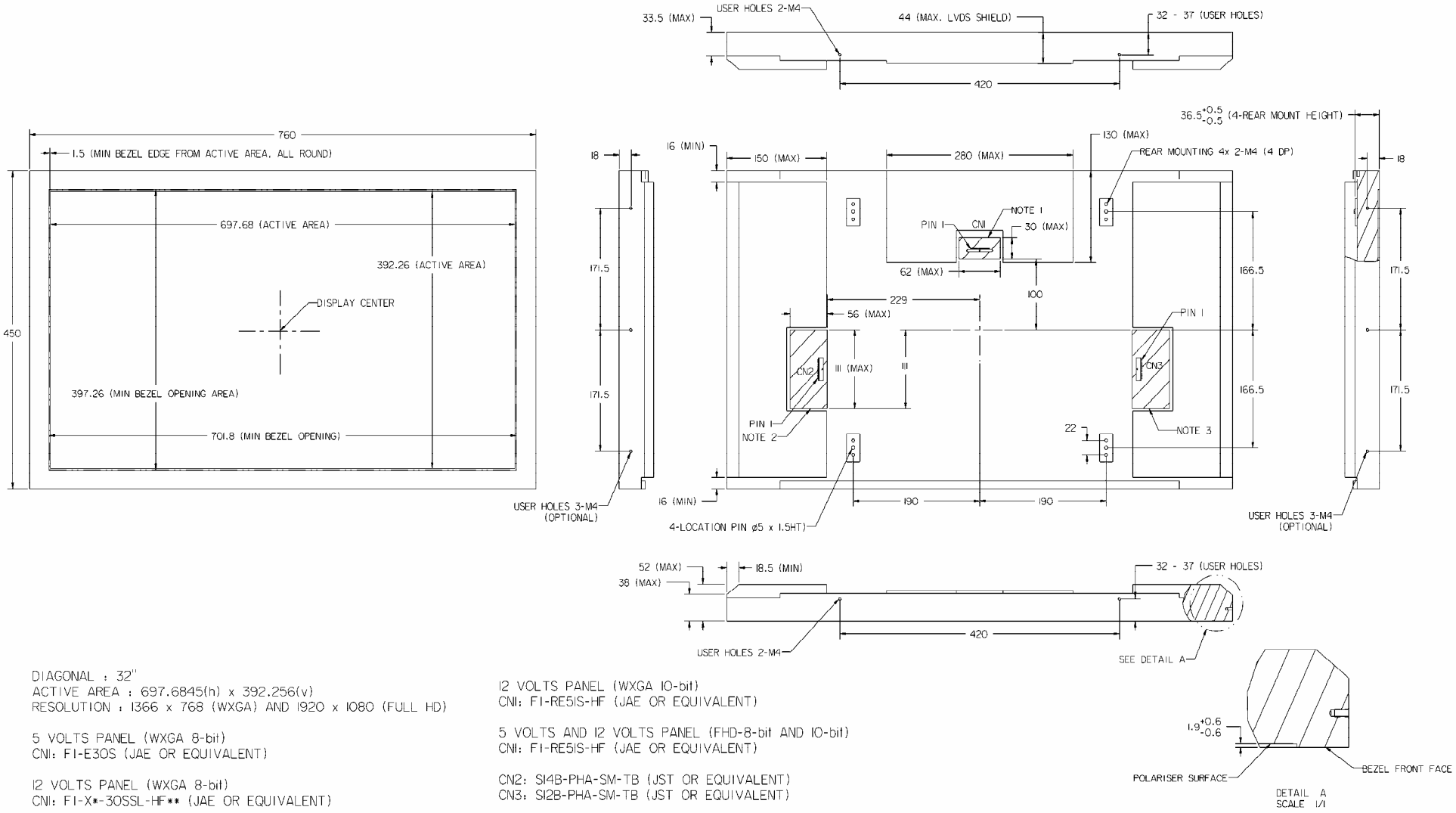
DIAGONAL : 26"
ACTIVE AREA : 575.77(h) x 323.71(v)
RESOLUTION : 1366 x 768
PIXEL SIZE : 0.4215(h) x 0.4215(w)

5 VOLTS PANEL
CN1: FI-E30S (JAE OR EQUIVALENT)
CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)
CN3: SI2B-PHA-SM-TB (JST OR EQUIVALENT)

12 VOLTS PANEL
CN1: FI-X*-30SSL-HF** (JAE OR EQUIVALENT)
CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)
CN3: SI2B-PHA-SM-TB (JST OR EQUIVALENT)

NOTE 1 : LVDS CONNECTOR KEEPOUT
NOTE 2 : INVERTER CONNECTOR (MASTER) KEEPOUT AREA.
NOTE 3 : INVERTER CONNECTOR (SLAVE) KEEPOUT AREA.

7.3 32” Mechanical Drawing



DIAGONAL : 32"
ACTIVE AREA : 697.6845(h) x 392.256(v)
RESOLUTION : 1366 x 768 (WXGA) AND 1920 x 1080 (FULL HD)

5 VOLTS PANEL (WXGA 8-bit)
CN1: FI-E30S (JAE OR EQUIVALENT)

12 VOLTS PANEL (WXGA 8-bit)
CN1: FI-X*-30SSL-HF** (JAE OR EQUIVALENT)

5 VOLTS PANEL (WXGA 10-bit)
CN1: FI-RE41S-HF (JAE OR EQUIVALENT)

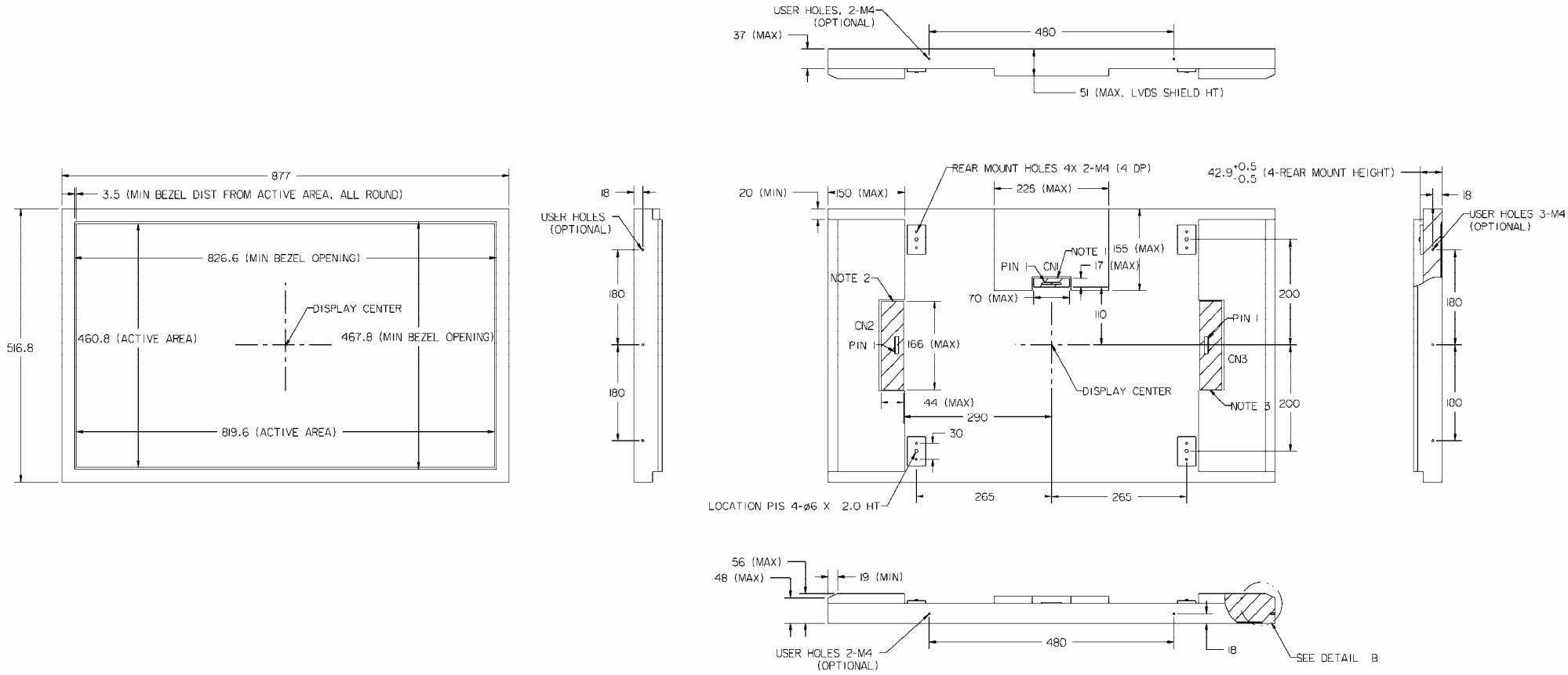
12 VOLTS PANEL (WXGA 10-bit)
CN1: FI-RE51S-HF (JAE OR EQUIVALENT)

5 VOLTS AND 12 VOLTS PANEL (FHD-8-bit AND 10-bit)
CN1: FI-RE51S-HF (JAE OR EQUIVALENT)

CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)
CN3: SI2B-PHA-SM-TB (JST OR EQUIVALENT)

NOTE 1 : LVDS CONNECTOR KEEPOUT AREA
NOTE 2 : INVERTER CONNECTOR (MASTER) KEEPOUT AREA.
NOTE 3 : INVERTER CONNECTOR (SLAVE) KEEPOUT AREA.

7.4 37” Mechanical Drawing



DIAGONAL : 37"
RESOLUTIONS : 1366 x 768 (WXGA) AND 1920 x 1080 (FULL HD)
ACTIVE AREA : 697.6845(h) x 392.256(v)

5 VOLTS PANEL (WXGA 8-bit)
CN1: FI-E30S (JAE OR EQUIVALENT)

12 VOLTS PANEL (WXGA 8-bit)
CN1: FI-X*-30SSL-HF** (JAE OR EQUIVALENT)

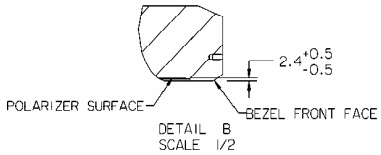
5 VOLTS (WXGA 10-bit)
CN1: FI-RE41S-HF (JAE OR EQUIVALENT)

12 VOLTS PANEL (WXGA 10-bit)
CN1: FI-RE51S-HF (JAE OR EQUIVALENT)

5 VOLTS AND 12 VOLTS PANEL (FHD-8-bit AND 10-bit)
CN1: FI-RE51S-HF (JAE OR EQUIVALENT)

CN2: SI4B-PHA-SM-TB (JST OR EQUIVALENT)
CN3: SI2B-PHA-SM-TB (JST OR EQUIVALENT)

NOTE 1 : LVDS CONNECTOR KEEPOUT AREA
NOTE 2 : INVERTER CONNECTOR (MASTER) KEEPOUT AREA.
NOTE 3 : INVERTER CONNECTOR (SLAVE) KEEPOUT AREA.



8 Backlight Interface

A JST connector S14B-PHA-SM-TB or equivalent connector will be used for the backlight inverter interface. All control signals are 3.3V (analog or CMOS digital). The pinout is shown in Table 6.

Pin 1 of the connector is located at the bottom side of the Connector viewed from the bottom of the panel. Refer to the mechanical drawings for details.

Depending on the implementation, some backlight interfaces have only 1 connector and some have master and slave connectors. The master connector has 14 pins and the slave connector provides 12 pins.

Typical control signals include the following:

- Analog Dimmer – 0V to 3.3V
- PWM Dimmer – 3.3V signal; Duty Cycle 30% to 100%
- BACKLIGHT_ON – HIGH: Backlight ON. 5V VDD logic. 3.3V input is accepted as HIGH.

Table 6 - Backlight Connector Pin-out

Pin#	Master	Slave
1	24.0V	24.0V
2	24.0V	24.0V
3	24.0V	24.0V
4	24.0V	24.0V
5	24.0V	24.0V
6	GND	GND
7	GND	GND
8	GND	GND
9	GND	GND
10	GND	GND
11	Control 1	Don’t Care
12	Control 2	Don’t Care
13	Control 3	
14	Control 4	

9 Glossary of Terms

Abbreviation

CCFL	Cold Cathode Fluorescent Lamp
DE	Display Enable
HS	Horizontal Sync
lsb	Least Significant Bit
LVDS	Low Voltage Differential Signaling: TIA/EIA-644
msb	Most Significant Bit
NC	No Connection
T_{deb}	Time - Display Enable Blanking
T_{ha}	Time - Horizontal Active
T_{hbp}	Time - Horizontal Back Porch
T_{hfp}	Time - Horizontal Front Porch
T_{hp}	Time - Total Horizontal Period
T_{hspw}	Time - Horizontal Sync Pulse Width
T_{va}	Time - Vertical Active
T_{vbp}	Time - Vertical Back Porch
T_{vfp}	Time - Vertical Front Porch
T_{vp}	Time - Total Vertical Period
T_{vspw}	Time - Vertical Sync Pulse Width
VBR	Backlight Brightness
VIN	Backlight Power
VON/OFF	Backlight On / Off
VS	Vertical Sync

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