Charles R. Moore and Russell C. Stanphill

The PowerPC **Alliance**

In September 1991, IBM, Apple and Motorola announced a broad alliance to jointly pursue the development of some of the following emerging technologies. The alliance included five principle initiatives:

- ***Object-oriented technology.*** Apple and IBM agreed to form Taligent, an independent company, to develop and license a future operating system based on object-oriented design principles.
- ***Multimedia technology.*** Apple and IBM agreed to form Kaleida, a joint venture company, to create and license multimedia technologies.
- ***Interconnectivity and networking.*** IBM and Apple agreed to develop hardware and software solutions that allowed their systems to interact more effectively.
- ***Open systems environment.*** Apple, IBM and Motorola agreed to jointly define the PowerOpen™ environment. PowerOpen supports both AIX™ and Macintosh applications, and will be licensed to other vendors.
- ***Microprocessor technology.*** IBM and Motorola agreed to jointly develop a broad family of microprocessors based on a derivative of IBM's POWER™ architecture called the PowerPC architecture.™

Central to this alliance is the commitment to the PowerPC Architecture and a family of microprocessors. Essentially, the companies have agreed to a vision that brings the architecture to the forefront of the computing world, and enables a broad range of PowerPC microprocessor-based systems. This article will primarily focus on the PowerPC microprocessor technology aspects of the alliance.

PowerPC Microprocessors

In addition to a commitment to the PowerPC Architecture, the alliance also calls for the development of a family of single-chip PowerPC microprocessor implementations. This initial family of devices is charged with providing superior solutions for system designers across a very wide range of system design points. As a result, the microprocessors must be general-purpose and offer versatile interfaces. The economics of the computer industry today demand that these designs be relatively inexpensive and allow for inexpensive system-level solutions. In addition, although the various members of the family may require specific optimization trade-offs for particular market segments, they must all exploit the inherent advantages of the PowerPC Architecture to achieve high performance.

To develop these devices, IBM and Motorola have jointly formed a PowerPC design center in Austin called Somerset. This jointly managed center is staffed with approximately 300 experienced microprocessor designers. A design methodology has been established that allows the team to achieve high-quality, aggressive designs on relatively short development cycles. This is achieved by blending tools that enhance designer productivity with tools that allow for full custom design and analysis. The tool set allows the designs to be fabricated by either IBM or Motorola manufacturing facilities using a common half-micron CMOS process.

PowerPC Architecture

The PowerPC Architecture is a third-generation RISC architecture that has been optimized for the diverse computing requirements of the future [3]. It has been jointly adopted by IBM, Motorola and Apple. The collective experience of these companies provided a firm foundation for making appropriate architectural

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trade-offs. The powerful new architecture embraces fundamental concepts of simplicity and general applicability while extending itself to advanced techniques that will carry it into the next decade and beyond.

There were several goals for the PowerPC Architecture. First, it was important that the architecture maintain an application binary interface (ABI) compatible with IBM's POWER architecture. This allows PowerPC microprocessor-based machines to leverage the application base that exists for IBM's RISC System/6000™ machines. To this end, the user-level instruction set and programming model of POWER was selected as a starting point for the PowerPC Architecture. Although some instructions were ultimately added and others deleted, these changes can effectively be managed by compilers and operating systems.

The second goal was to simplify the architecture and ease unnecessary implementation requirements. This flexibility allows implementers to make optimizations that are appropriate for specific market targets. In addition, the simplifications allow for smaller chip sizes, faster cycle times, and more aggressive superscalar implementations.

A third objective of the PowerPC Architecture was to provide support for a wide range of uniprocessor and multiprocessor system configurations. This objective was achieved by recognizing key abstractions of the storage hierarchy and defining the storage control architecture to allow effective management of these abstractions. Furthermore, the architecture allows storage references to follow either a big-endian or a little-endian byte ordering convention.

Finally, the PowerPC Architecture was defined with a set of 64-bit extensions that allow for upward compatibility of 32-bit applications. This was achieved by defining the 64-bit instruction operation as a logical extension to the 32-bit execution model. The memory management architecture was also extended to allow address translation of 64-bit addresses. To allow flexibility, each implementation can be compliant with either the base 32-bit PowerPC Architecture or the extended 64-bit architecture.

The alliance partners agreed to an initial microprocessor roadmap (see Figure 1) that specifies four independent design points. Each of these designs are challenged with bringing industry leadership solutions to their specific segments of the computing market. The initial four design points include the following:

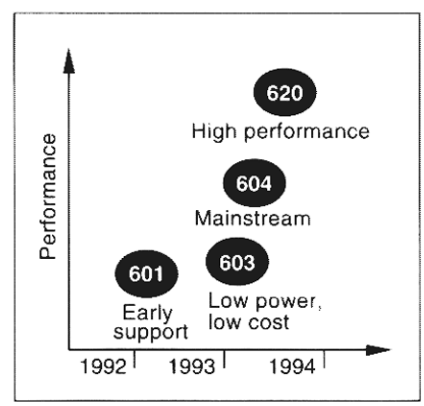

Figure 1. PowerPC roadmap

The **PowerPC 601™ microprocessor** is the first member of the family and is responsible for bringing PowerPC Architecture to the market as early as possible [2]. It is targeted for early PowerPC adopters and is suited for use in desktop computers, portable systems, and low-end multiprocessor systems. The design implements the 32-bit PowerPC Architecture and achieves competitive performance at a relatively low cost. Processor chips have been available since early 1993, and first PowerPC 601 microprocessor-based systems were introduced by IBM in the fall of 1993. The PowerPC 601 is available in 50-, 66-, 80-, and 100MHz versions.

The **PowerPC 603™ processor** is defined to address the low-end and low-cost range of the 32-bit PowerPC microprocessor family [1]. This part packs desktop performance into an 85 square millimeter die, and dissipates less than 3 watts of power at 80MHz. The chip is intended for use in low-end desktop systems and portable systems. This part was announced formally in October 1993, and is slated for production in 3Q94.

The **PowerPC 604™ microprocessor** is designed for mainstream computing environments including personal computers, midrange workstations, and multiprocessor systems. It is organized to offer superior performance over the competition, and outstanding price/performance. The chip is a 32-bit implementation of the PowerPC Architecture, and uses advanced superscalar design techniques to achieve high performance. Samples are expected in the third quarter of 1994.

The **PowerPC 620™ processor** is designed to deliver the maximum performance achievable with the currently available half-micron CMOS process technology. This superscalar design implements the full 64-bit PowerPC Architecture and includes an embedded L2 cache controller that interfaces to standard static random access memory (SRAM) chips. The design is targeted at high-end desktop computers, work-group servers and transaction processing-based systems. Samples are expected in the second half of 1994.

These four microprocessors will be heavily used in future IBM and Apple products, and they will also be independently marketed and sold by both IBM and Motorola for use by other system developers. The extension of the PowerPC microprocessor family to the open market is an important and strategic part of the alliance's plan to make PowerPC Architecture successful.

Future Direction

The four microprocessor designs identified on the current roadmap represent only the start of the PowerPC processor development. As technology continues to advance, new opportunities for higher performance, greater levels of integration, lower power consumption and lower cost will arise. IBM and Motorola are committed to driving these technology advancements into their processor development efforts, and to extend the product roadmap to eventually cover an even greater range of computing requirements.

In addition, over time, the existing design points will become usable as *cores* for more fully integrated and optimized solutions for particular target applications or markets. These cores will also be available for customers to use in development of their own application-specific VLSI solutions. Finally, relevant aspects of the PowerPC Architecture will be driven into other market segment opportunities. For example, in a separate effort, IBM is developing a line of embedded controllers based on portions of the PowerPC Architecture. These controllers will be suitable for environments that are less demanding than the general-purpose computing environment, yet still require high performance at a very low cost. ■

References

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2. Moore, C.R., The PowerPC 601 microprocessor. *IBM RISC System/6000 Technology: Vol. II*, IBM Corp., 1993.
3. Silha, E. PowerPC Architecture: A high-performance architecture with a history. *IBM RISC System/6000 Technology: Vol. II*, IBM Corp. 1993.

In this document, the terms PowerPC 601 microprocessor and 601; PowerPC 603 microprocessor and 603; PowerPC 604 microprocessor and 604; and PowerPC 620 microprocessor and 620 are used to denote the various microprocessors from the PowerPC Architecture family.

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About the Authors:

CHARLES R. MOORE is senior engineer in the RISC System/6000 division of IBM Corp. He is currently working in the high-end processor development group. His research interests include high-performance computer organizations, VLSI design methods and strategic planning. **Author's Present Address:** IBM Corp., 11400 Burnet Rd, M/S 4305, Austin, TX 78758-3493; email: cmoore@ibmoto.com

RUSSELL C. STANPHILL is a Motorola veteran, currently serving as codirector of the Somerset Design Center. In 1991, Stanphill was instrumental in working with Apple and IBM to form what is now the PowerPC alliance. By early 1992 he was elected to manage the resulting Somerset facilities. **Author's Present Address:** Motorola, Semiconductor Products Sector, Microprocessor and Memory Technologies Group, 6501 William Cannon Drive West, Austin, TX 78735-8598.

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