Electrostatic Discharge (ESD) Technology Roadmap – Revised April 2010

Synopsis

This document provides estimates of future ESD device thresholds and their potential impact on ESD control practices. The threshold estimates reflect the prevailing trends in semiconductor technology as viewed by selected industry leaders. These projections are intended to provide a view of future device protection limitations driven by performance requirements and technology scaling. It also provides a common view of expected performance for device suppliers and users. Finally, these trends point to the need for continued improvements in ESD control procedures and compliance.

Introduction

In the late 1970s, electrostatic discharge, or ESD, became a problem in the electronics industry. Low level ESD events from people were causing device failures and yield losses. As the industry learned about this phenomenon, both device design improvements and process changes were made to make the devices more robust and processes more capable of handling these devices.

During the 1980s and early 1990s device engineers, after going through a learning curve, were able to create protection structures that could withstand higher levels of ESD and thus made the devices less sensitive to ESD events. Both device engineers and circuit designers were able to identify key technology parameters that helped them develop more robust devices.

In the mid to late 1990s however, the requirements for increased performance (devices that operate at 1 GHz and higher) and the increase in the density of circuits on a device caused problems for traditional ESD protection circuits. This was exacerbated with the continued scaling of the technologies toward sub-100 nm feature sizes in order to achieve higher density and performance. The situation became worse with the advent of IC chips with sub-50 nm technologies rapidly coming into production. Due to this trend, the ICs became even more sensitive to ESD events in the years between 2005 and 2009. Therefore, the prevailing trend is circuit performance at the expense of ESD protection levels. This is now becoming critical for high speed serial link IOs (HSS) and even more so in the case of RF circuit applications.

Device ESD Threshold Trends

The following graphs show the device ESD design sensitivity trends based on the most relevant and important ESD models used by device manufacturers as part of the device qualification process: Human Body Model (HBM) and Charge Device Model (CDM). The sensitivity limits are a projection by engineers from leading semiconductor manufacturers. First, the projections for HBM design (min and max) are indicated in Figure 1. Also shown is the progression of ESD control capability for HBM during the same time period. Although design improvements were made from 1978 through 1993, the advanced circuit performance effects started to take place around this time, eventually degrading the levels. The max levels represent what is generally possible from technology scaling and min represents the constriction coming from meeting the circuit

performance demands. It is interesting to observe that the gap between the ESD control and sensitive device HBM levels is closing in, and that, at the beginning of this new decade, the control of ESD for HBM is just barely below the minimum expected high sensitivity HBM designs. Therefore, proactive implementation of advanced HBM controls using the limits and qualifications requirements in ANSI/ESD S2020 or IEC 61340-5-1 would become necessary within the next 5 years.

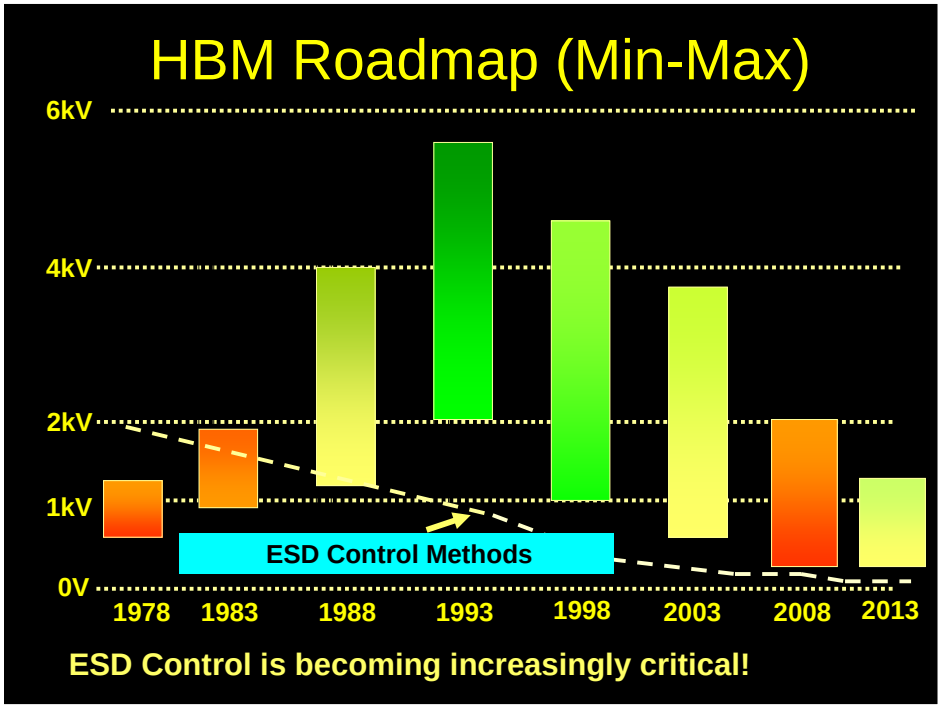

Figure 1 - Human Body Model Sensitivity Limits Projections

The projections for CDM design (min and max) are indicated in Figure 2. Also shown is the progression of ESD control capability for CDM during the same time period. The same general arguments as given above for HBM also apply for CDM. However, the advanced designs will have a larger impact on CDM. This is because the HSS IOs are generally used in high pin-count, hence larger capacitance, IC packages. This higher capacitance leads to relatively higher magnitude discharge peak current levels, and thus greater challenges in CDM protection design. For CDM, a proactive implementation of advanced CDM controls would not only become necessary but would become mandatory within the next 5 years.

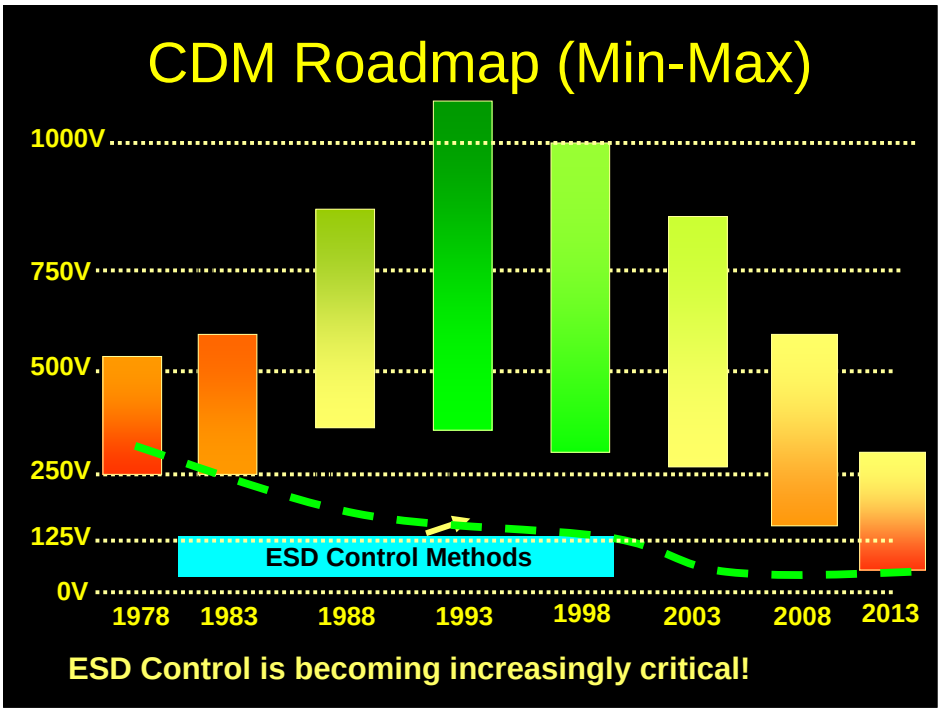

Figure 2 - Charged Device Model Sensitivity Limit Projections

For future device qualification, HBM and CDM should fulfill the necessary requirements. Further, as documented in White Paper I from the Industry Council, Machine Model (MM) protection is intrinsic to HBM and does not need a separate tracking for design purposes [1]. Thus, a separate technology roadmap for MM is not necessary. However, it can be assumed that the MM values are generally a factor of between 10 and 30 times lower than the published HBM qualification numbers for HBM >500V, and approximately 5 times lower for HBM <500 V. It should also be pointed out that conductor-to-device discharges are not well represented by MM. The CDM method gives a better representation of these events. In summary, although machine discharge control is important for a factory environment, the MM device test method levels themselves, per-se, have no relevance. HBM and CDM levels are the important criteria for technology scaling.

Process Capability

These ESD sensitivity trends will have a major impact on manufacturing process yields over the next five years. Companies need to verify that the installed ESD processes are capable of handling these devices.

When designing ESD control processes they must be repeatable and consistent. In addition, there must be a way to evaluate how effective the ESD control items are, based on the sensitivities that are expected to be handled. The following notes provide guidelines on how to evaluate ESD control processes.

Human Body Model (HBM)

It has been shown that for a wrist strap system, the resistance of the person to ground has a direct correlation to the maximum voltage on a person. For wrist straps, Figure 3 may be used.

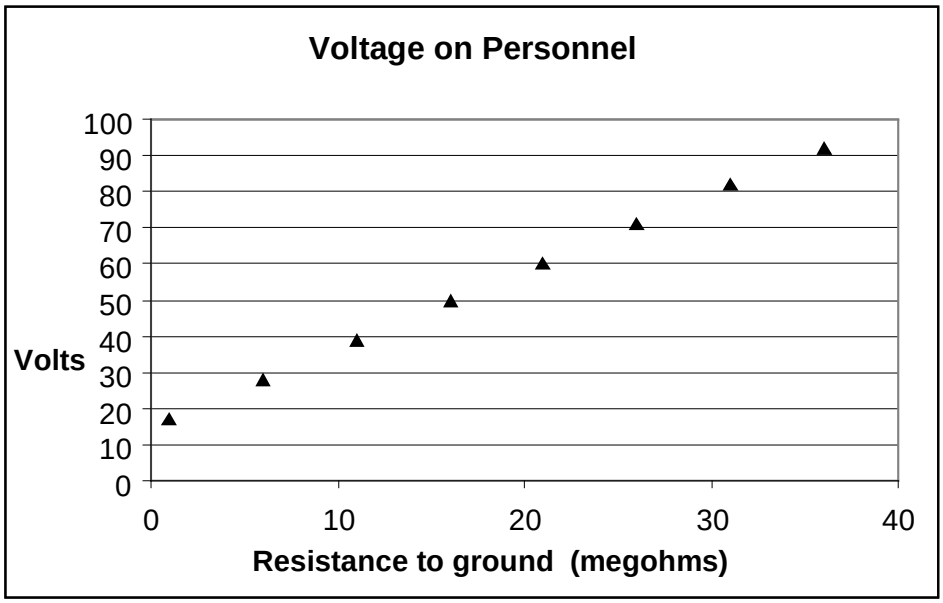

Figure 3 - Resistance in a Wrist Strap System

For an ESD control program that uses ESD footwear and flooring to ground personnel, the situation is more complex. As people walk across an ESD floor while wearing ESD footwear, it is difficult to predict the voltage on a persons' body due to the constantly changing body capacitance and the continuous charging and discharging of the person.

ANSI/ESD STM97.2 can be used to determine the process capability of the footwear flooring system. An example of the type of information provided can be seen below in Figure 4.

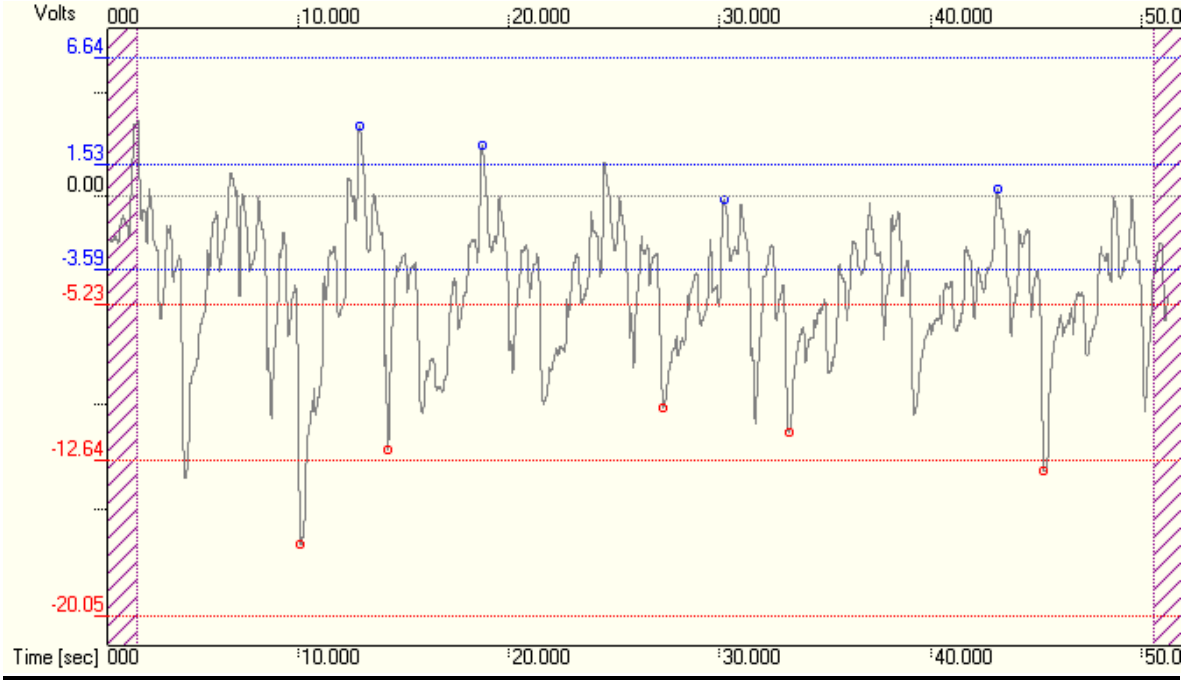

Figure 4 - Determining Process Capability of a Footwear/Flooring System Using ANSI/ESD STM 97.2

Metal Discharge Events

Machine discharges occur when charged, conductive surfaces come into contact with ESD sensitive devices. To minimize machine discharges, ensure that all metal surfaces that come into contact with ESD sensitive devices are grounded. Measurements should be made to ensure that moving parts remain grounded throughout the process.

CDM Events (CDM)

CDM damage occurs when a charged ESD sensitive device is grounded or when a neutral device is grounded in the presence of an electrostatic field. Effective ESD control programs ensure that process required insulators will not induce damaging voltage levels onto the devices being handled, nor allow a device to acquire a charge by triboelectrification and then be subsequently grounded in an uncontrolled fashion.

An example of the impact of decreasing CDM levels on factory practices is illustrated in Figure 5. This chart shows the voltage induced onto a 20 pF parallel plate capacitor from a 2000 volt uniform voltage source at varying distances. Overlaid onto the chart are the minimum CDM levels from the CDM roadmap for the years 2000, 2005, and 2010. Since the devices will become more sensitive over time it will be necessary to either:

A. Increase the distance between the ESD sensitive devices and the charged source or

B. Reduce the charges on surfaces to levels that will limit the induced voltage to levels that will not damage ESD sensitive devices.

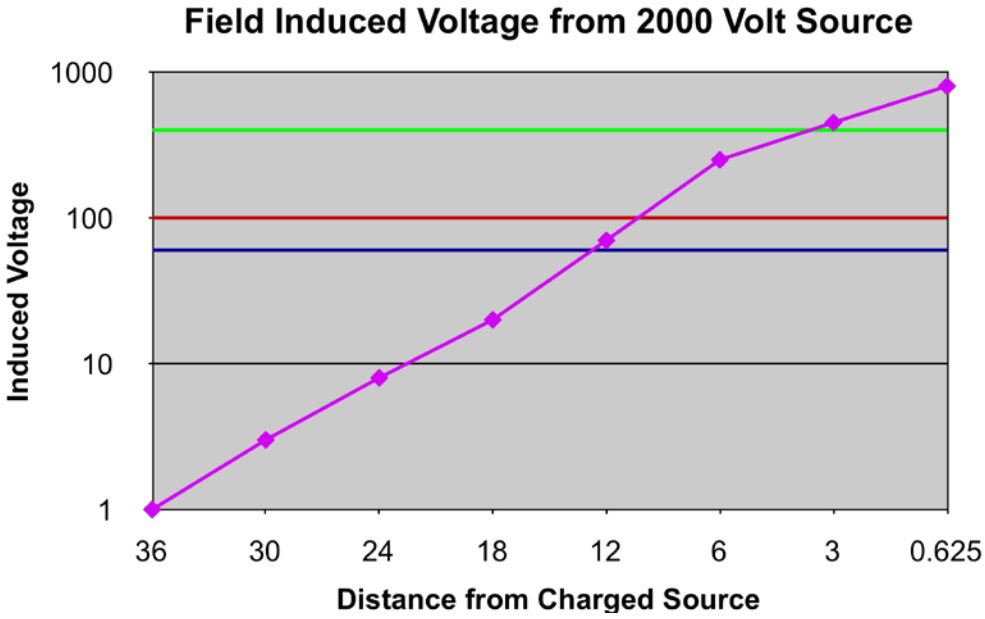

Figure 5 - Voltage Induced onto a 20 pF parallel plate capacitor from a 2000 Volt Uniform Voltage Source at Varying Distances

Conclusions:

With devices becoming more sensitive through 2010-2015 and beyond, it is imperative that companies begin to scrutinize the ESD capabilities of their handling processes. Factory ESD control is expected to play an ever-increasing critical role as the industry is flooded with even more HBM and CDM sensitive designs. For people handling ESD sensitive devices, personnel grounding systems must be designed to limit body voltages to less than 100 volts.

To protect against metal-to-device discharges, all conductive elements that contact ESD sensitive devices must be grounded.

To limit the possibilities of a field induced CDM ESD event, users of ESD sensitive devices should ensure that the maximum voltage induced on their devices is kept below 50 volts.

To limit CDM ESD events, device pins should be contacted with static-dissipative material instead of metal wherever possible.

1. White Paper 1: “A Case for Lowering Component Level HBM/MM ESD Specifications and Requirements,” August 2008, http://www.esda.org/IndustryCouncil.html.

2. White Paper 2: “A Case for Lowering Component Level CDM ESD Specifications and Requirements,” March 2009, http://www.esda.org/IndustryCouncil.html.