HyperTransport™ Consortium

HTX3™ Specification

for

HyperTransport™ 3.0 Daughtercards and ATX/EATX Motherboards

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1. Objective

The HTX3™ Specification for HyperTransport™ Daughtercards and ATX/EATX Motherboards allows developers to deliver HyperTransport™ solutions using standard high-volume platforms such as AMD Opteron™ Processor systems. Standardized HTX3™ -capable motherboards will enable HyperTransport™ silicon and subsystem developers to deliver solutions based on commodity hardware—eliminating the need for custom solutions in most cases.

HTX3™ is intended to be fully backwards compatible with the original HTX™ (HTC2004105-00040-0011) specification while simultaneously allowing designers to take advantage of the new features and capabilities of HyperTransport™ 3.0.

2. Electrical Features of the Specification

The HTX3™ Connector and Form Factor Specification:

- Supports a single 16-bit HyperTransport™ 3.0 interface or one or two 8-bit HyperTransport™ 3 interfaces using link unganging
- Runs at up to a 2.6 GHz clock rate (5.2G transfers/sec)
- Provides all HyperTransport™ 3.0-specific control signals, including synchronous reference clock
- Delivers both 12V and 3.3V power, up to 63 watts combined
- Provides an SMBus interface (3.3V)
- Optionally supports JTAG
- Allows use of 4-layer motherboards and daughtercards with conventional PCB technology

3. Mechanical Features of the Specification

The HyperTransport™ 3.0 EATX Motherboard/Daughtercard Specification:

- Is optionally compatible with the standard ATX (12”x9.6”) and Extended ATX (12x13”) motherboard form factors
- Full height and low-profile form factors as well as short and long cards
- Daughtercard mechanical envelopes are compatible with standard PCI cards to fit in existing chassis designs
- Usable in both riser-based (1U) and pedestal, rack-mount or proprietary applications
- Uses inexpensive commodity connectors available from multiple sources
- Placement of connectors designed to exclude the possibility of accidentally inserting cards built to other known interface specifications

4. Specification Summary

A typical HyperTransport™ 3.0™ dual-processor motherboard layout is illustrated in Figure 1. The slots are numbered from right to left as is the convention for extended ATX. The HTX3™ connectors occupy slot 6, utilizing standard PCI-Express™ 1x and 16x connectors installed in the reverse orientation of normal PCI-Express™. Slot 6 results in a design which is the most easily routable, has the shortest and most direct path for HyperTransport™ 3.0, and which allows the same form factor as PCI-Express™ in a 1U server. Note that the HyperTranspor™t 3.0 signals should route in from the right side so that the signals have the correct routing order on the daughtercard's HyperTransport™ chip. The HyperTransport™ 3.0 host must reside on the motherboard.

The rest of the board's I/O infrastructure is unaffected. The functions of slots 1 through 5 are application-dependent and beyond the scope of this document.

Usage note: Some motherboard vendors may place the HTX3™ connectors in slot 5 so that the same motherboard may support the use of either PCI-Express™ or HTX3™ daughtercards in 1u enclosures. However, doing so requires that the HTX3™ daughtercard be of the low-profile form factor and that it use a unique daughtercard faceplate designed for slot 5 use.

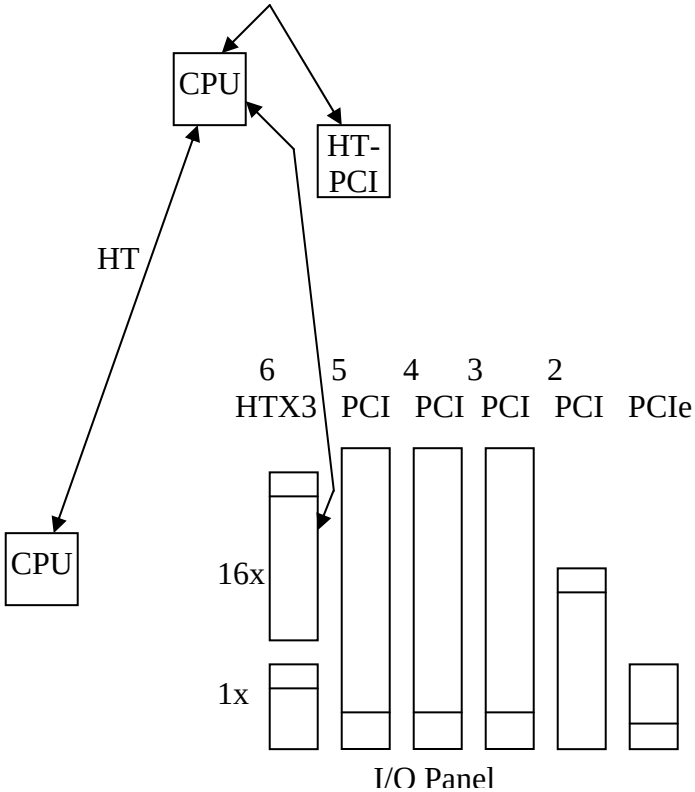
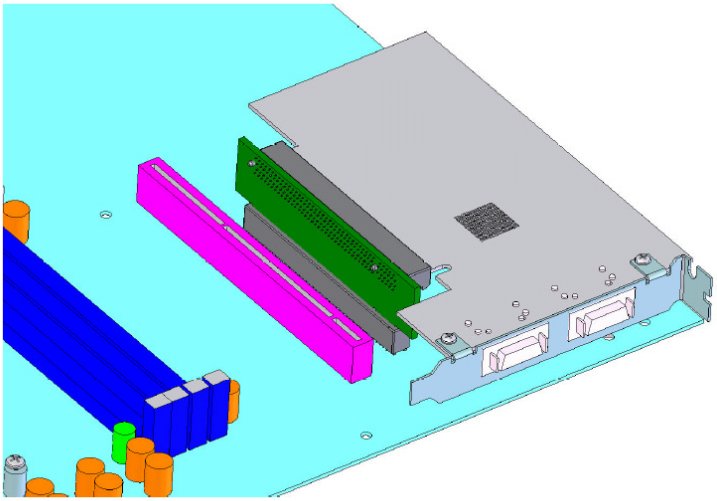


Figure 1. Typical Dual Processor HyperTransport™ 3.0 Motherboard

This specification defines the mechanical locations of the connectors, pinouts, signaling conventions, mechanical specifications for the 1U riser card and HTX3™ daughtercard, and layout rules for motherboard, riser, and daughtercard.

A 1U system, shown in Figure 2, supports a single HTX3™ daughtercard using the HTX3™ riser, and such a HyperTransport™ 3.0-enabled assembly is mechanically 100% compatible with existing 1U chassis designs.



A 3U or greater rack-mount or pedestal server can accommodate the full height card plugged in vertically in conjunction with other PCI and/or PCI Express™ cards, as shown in Figure 3. No change in chassis design is required. The low-profile form factor is suitable for use in 2U chassis.

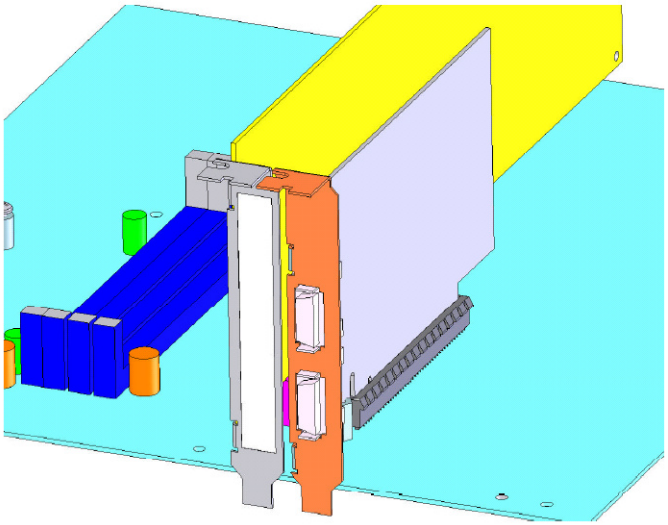


Figure 3. 3U System with Vertically Mounted HTX3™ Daughtercard

5. Connector Pinout

Pinouts for the two HTX3™ motherboard connectors are shown in Table 1. Signal names are from the perspective of the motherboard, e.g. the motherboard drives CADOUT signals and receives CADIN signals, etc.

Table 1. Connector pinouts:

Pin	A	B	Pin
1	VLDT	GND	1
2	VLDT	GND	2
3	GND	CADIN8H	3
4	GND	CADIN8L	4
5	CADIN0H	GND	5
6	CADIN0L	GND	6
7	GND	CADIN9H	7
8	GND	CADIN9L	8
9	CADIN1H	GND	9
10	CADIN1L	GND	10
11	GND	RSVD	11
12	RSVD	GND	12
13	GND	CADIN10H	13
14	GND	CADIN10L	14
15	CADIN2H	GND	15
16	CADIN2L	GND	16
17	GND	CADIN11H	17
18	GND	CADIN11L	18
19	CADIN3H	GND	19
20	CADIN3L	GND	20
21	GND	CLKIN1H	21
22	GND	CLKIN1L	22
23	CLKIN0H	GND	23
24	CLKIN0L	GND	24
25	GND	CADIN12H	25
26	GND	CADIN12L	26
27	CADIN4H	GND	27
28	CADIN4L	GND	28
29	GND	CADIN13H	29
30	GND	CADIN13L	30
31	CADIN5H	GND	31
32	CADIN5L	GND	32
33	GND	CADIN14H	33
34	GND	CADIN14L	34
35	CADIN6H	GND	35
36	CADIN6L	GND	36
37	GND	CADIN15H	37
38	GND	CADIN15L	38
39	CADIN7H	GND	39
40	CADIN7L	GND	40
41	GND	CTLIN0H	41
42	GND	CTLIN0L	42
43	CTLOUT0L	GND	43
44	CTLOUT0H	GND	44
45	GND	CADOUT15L	45
46	GND	CADOUT15H	46
47	CADOUT7L	GND	47
48	CADOUT7H	GND	48
49	GND	CADOUT14L	49
50	GND	CADOUT14H	50
51	CADOUT6L	GND	51

Top of connector (furthest from I/O Panel) as viewed from the solder side of the motherboard.

RSVD and RSVDFS pins should be left *unconnected*, not grounded.

Motherboards that drive or receive USER pins should allow correct operation of daughtercards which leave these pins unconnected.

The “A” side of the daughtercard is the component side.

52	CADOUT6H	GND	52
53	GND	CADOUT13L	53
54	GND	CADOUT13H	54
55	CADOUT5L	GND	55
56	CADOUT5H	GND	56
57	GND	CADOUT12L	57
58	GND	CADOUT12H	58
59	CADOUT4L	GND	59
60	CADOUT4H	GND	60
61	GND	CLKOUT1L	61
62	GND	CLKOUT1H	62
63	CLKOUT0L	GND	63
64	CLKOUT0H	GND	64
65	GND	CADOUT11L	65
66	GND	CADOUT11H	66
67	CADOUT3L	GND	67
68	CADOUT3H	GND	68
69	GND	CADOUT10L	69
70	GND	CADOUT10H	70
71	CADOUT2L	GND	71
72	CADOUT2H	GND	72
73	GND	CADOUT9L	73
74	GND	CADOUT9H	74
75	CADOUT1L	GND	75
76	CADOUT1H	GND	76
77	GND	CADOUT8L	77
78	GND	CADOUT8H	78
79	CADOUT0L	GND	79
80	CADOUT0H	GND	80
81	GND	USER	81
82	RSVD	GND	82

Pin	A	B	Pin
1	GND	USER	1
2	REFCLKL	GND	2
3	REFCLKH	GND	3
4	GND	CTLIN1L	4
5	GND	CTLIN1H	5
6	CTLOUT1L	GND	6
7	CTLOUT1H	PWROK	7
8	LDTSTOP#	RESET#	8
9	+3.3Vaux	+3.3V	9
10	TRST#	+3.3V	10
11	+3.3V	TMS	11
12	GND	TDO	12
13	SMDAT	TDI	13
14	SMCLK	TCK	14
15	GND	GND	15
16	LDTREQ#	+12V	16
17	+12V	+12V	17
18	+12V	RSVDFS	18

Bottom of connector, near I/O panel

Unshaded pins are staggered closer together in the connector than shaded pins.

Pinout considerations include:

- No high-speed signals at connector edge
- Dedicated ground next to every high-speed signal
- HyperTransport™ 3.0-specific control and power signals closer to top of connector
- Ordering of HTX3™ signals matches standard device pinout
- Pinout near I/O panel similar to PCI-Express™ pinout for ease of bussing

6. Power distribution

Power specifications, shown in Table 2, are identical to 16x PCI-Express™ with the addition of VLDT.

Power supply	Voltage	Tolerance	Current
+12V	12V	±8%	4.4A
+3.3V	3.3V	±9%	3A
+3.3Vaux	3.3V	±9%	375ma
VLDT	1.2V	±5%	2A

Table 2. Power specifications

+12V, +3.3V, +3.3Vaux, VLDT and GND signals should be routed to planes or copper pours to ensure low impedance connections.

Although outside the scope of this specification, it is permissible to provide extra power to the daughtercard using a power connector mounted on the daughtercard itself. System designers choosing this method must ensure that the enclosure provides adequate cooling and mechanical clearance and that ground loops are avoided.

7. Signal Description Summary

Table 3 provides a description of the signals on the HyperTransport™ connectors. "MB" refers to motherboard and "DC" refers to daughtercard.

Table 3. Connector Signal Characteristics

Signal name	Count	Direction	Level	Description	Required MB	Required DC
+12V	4	In	Power	12V power	Yes	Yes
+3.3V	3	In	Power	3.3V power	Yes	Yes
+3.3Vaux	1	In	Power	3.3V auxiliary power	Yes	Yes
VLDT	2	In	Power	1.2V HT power	Yes	Yes
GND	91	Common	Ground	Signal ground	Yes	Yes
CADIN[15:8][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	No	No
CADIN[7:0][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	Yes	Yes
CLKIN1[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	No
CLKIN0[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	Yes
CTLIN[1:0][H:L]	2 pairs	DC→MB	LDT diff	HT control	Yes	Yes
CADOUT[15:8][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	No	No
CADOUT[7:0][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	Yes	Yes
CLKOUT1[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	No
CLKOUT0[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	Yes
CTLOUT[1:0][H:L]	2 pairs	MB→DC	LDT diff	HT control	Yes	Yes
LDTSTOP#	1	MB→DC	2.5V CMOS	HT LDTSTOP	Yes	Yes
LDTREQ#	1	DC→MB	2.5V CMOS	HT LDTREQ	Yes	No
PWROK	1	Bidir	2.5V CMOS	HT power OK	Yes	Yes
RESET#	1	Bidir	2.5V CMOS	HT reset	Yes	Yes
REFCLK[H:L]	1 pair	MB→DC	3.3V diff LVPECL	200MHz HT reference clock	Yes	Yes
SMCLK	1	MB→DC	3.3V CMOS	SMBus clock	Yes	No
SMDAT	1	Bidir	3.3V CMOS	SMBus data	Yes	No
TCK	1	MB→DC	3.3V CMOS	JTAG clock	No	No
TMS	1	MB→DC	3.3V CMOS	JTAG mode select	No	No
TRST#	1	MB→DC	3.3V CMOS	JTAG reset	No	No
TDI	1	MB→DC	3.3V CMOS	JTAG data in	No	No
TDO	1	DC→MB	3.3V CMOS	JTAG data out	No	No
USER	2	User	User	User-defined	-	-
RSVD	3	-	-	Reserved, do not connect	-	-
RSVDFS	1	-	-	Reserved, future standardization	-	-

a. Routing Rules

The HyperTransport™ connector should be considered a “zero mismatch boundary” as defined in Section 2.3.6.2 of the HyperTransport™ Interface Design Guide, Rev. 1.07. Motherboard and daughtercard routing should comply with the Interface Design Guide using this assumption. This allows the routing for the motherboard and the daughtercard to be independent and interoperable.

Trace lengths for HyperTransport™ signals on the motherboard should not exceed 9.25 inches. Trace lengths on the daughtercard should not exceed 2.75 inches. This will ensure that the total trace length will not exceed the maximum allowed 12 inches.

Designers should ensure that +12V, +3.3V, +3.3Vaux, VLDT and GND pins are connected to a power plane or copper pour to ensure low impedance connections.

b. RESET# and PWROK

HTX3™ -compliant motherboards and daughtercards must implement RESET# and PWROK using open drain drivers.

RESET# may optionally be driven low (asserted) by the daughtercard. A pullup resistor of value greater than or equal to 1K ohms shall be placed on the motherboard. A minimum of 500 milliseconds should be allotted between the assertion of PWROK and the deassertion of RESET# to allow time for the initialization of any FPGAs on the daughtercard.

PWROK may optionally be driven low (deasserted) by the daughtercard. A pullup resistor of value greater than or equal to 1K ohms shall be placed on the motherboard. HTX3™ daughtercards containing FPGAs with long initialization times may drive PWROK low during the FPGA initialization sequence. Once initialization of the FPGAs completes, driving PWROK high will cause the motherboard to enter the Hypertransport™ 3.0 initialization sequence.

Usage note: FPGA-based daughtercards which deassert PWROK in order to ensure proper completion of FPGA initialization before system startup should drive PWROK with an external component. PWROK must remain low during the entire FPGA initialization operation if this method is used.

c. Single-Ended Signal Level Shifters

HyperTransport™ 3.0 specifies a new VLDT voltage reference for the open drain single ended signals PWROK, RESET#, LDTSTOP# and LDTREQ# (see *HyperTransport™ I/O Link Specification Rev. 3.0*, Section 19). HyperTransport™ 1.0 devices reference these signals to 2.5V. To ensure backwards compatibility with first generation HTX™ daughtercards, the motherboard must provide level shifters to support the 2.5V signal levels at the HTX3™ connector.

8. Signal Integrity

Signal integrity for HyperTransport™ 1.0 devices shall be measured according to the HyperTransport™ Electrical Compatibility Measurements Rev. 0.03, HyperTransport Technology Consortium document number HTC20021219-0018-0001.pdf. HyperTransport™ 3.0 devices shall be compliant with the HyperTransport I/O Link Specification, Rev. 3.0. Settings for TX de-emphasis and RX equalizers are outside the scope of this specification.

9. Higher Speed Operation

Operation at speeds higher than 5.2 GT/sec is outside the scope of this specification. Designers are urged to minimize trace lengths and signal skew to achieve best results at higher speeds. Modeling of system signal integrity using a tool such as Spice is highly recommended to verify an acceptable eye pattern at the receivers. Use of surface mount connectors is recommended to reduce stubs and stray capacitances.

10. 8-bit Link Support

If a first generation HTX™ daughtercard only supports a single 8-bit HyperTransport™ link, then it must tie CADIN[15:8]H and CLKIN1H to GND through 51 ohm resistors and CADIN[15:8]L and CLKIN1L to VLDT through 51 ohm resistors. In addition, both CTLIN1H and CTLIN1L must be tied to GND through 51 ohm resistors to ensure that the Opteron™ processor correctly identifies that the high order link is unused.

HyperTransport™ 3.0 devices can support both 16 bit ganged and 8 bit unganged operation. Link operation and width are determined by the processor's sampling of CTL and CAD lines prior to the deassertion of RESET# as specified in Chapter 12 of the *HyperTransport™ I/O Link Specification, Revision 3.0*. Table 4 summarizes the requirements for driving CTL and CAD prior to the deassertion of RESET#.

Table 4. CTL and CAD Settings Prior to Deassertion of RESET#

Mode	CTLIN1	CTLIN0	CAD[15:00]
16-bit ganged link	Logic 1	Logic 0	0x00FF
8 bit Sublink 0 used, Sublink 1 unused[1]	Logic 0	Logic 0	0x00FF
Both unganged 8 bit sublinks 0 and 1 used	Logic 0	Logic 0	0xFFFF

[1] Motherboards and daughtercards which use only a single 8-bit sublink ***must*** use Sublink 0.

Table 5 summarizes the legal combinations of HTX™ and HTX3™ motherboards and daughtercards.

Table 5. Supported Configurations

	Supported Daughtercards				
Motherboard Slot Type	HTX™ 16-bit[2]	HTX™ 8-bit Link 0	HTX3™ 16-bit ganged[2]	HTX3™ 8-bit Link 0	HTX3™ 2 x 8-bit Links 0 & 1
HTX™	Yes	Yes	Yes (800 MHz Max)	Yes (800 MHz Max)	Link 0 Only (800 MHz Max)
HTX3™ 16-bit link to single cpu	Yes[3]	Yes	Yes[4]	Yes	Yes
HTX3™ 8-bit link to single cpu (Link 0)	Yes, in 8-bit mode	Yes	Yes, in 8-bit mode	Yes	Link 0 Only
HTX3™ - Two 8-bit links to two cpus	Yes, in 8-bit mode	Yes	Yes, in 8-bit mode	Yes	Yes

[2] Device will come up as 8-bits and BIOS must configure it for 16-bit operation.
[3] BIOS must gang the link.
[4] BIOS must detect that both links connect to the same device and gang the link.

11. Unused HyperTransport Slot

In the event that the HTX3™ slot is unused, an optional terminator board of the same form factor as the HTX3™ daughtercard or the same form factor as the HTX3™ riser card may be provided to prevent floating inputs and/or jumper the JTAG chain. This board should tie CADIN[15:0]H, CLKIN[1:0]H and CTLIN[1:0][H:L] to GND through 51 ohm resistors and CADIN[15:0]L and CLKIN[1:0]L to VLDT through 51 ohm resistors. TDI should be jumpered to TDO to complete the JTAG chain. A terminator board is not strictly required, as a floating link will be seen by the processor as not connected. An optional jumper to connect TDI to TDO may be placed on the motherboard to jumper the JTAG chain if the slot is unused. However, this jumper must be removed to ensure proper JTAG operation if a daughtercard is present.

12. Motherboard Dimensions and Connector Placement

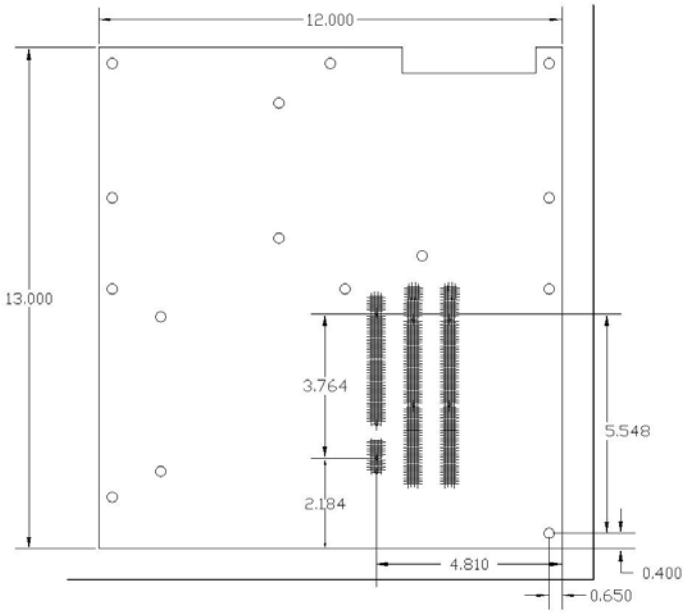


Figure 4. EATX Motherboard with HTX3™ Connector in Slot 6 Position

The example shown in Figure 4 is an EATX motherboard with the HTX3™ connector in the position normally occupied by PCI slot 6. Placing the HTX3™ connector in the slot 6 position permits operation with a riser, allowing the use of a 1u enclosure. Proprietary designs may place the HTX3™ connector in any of the PCI slot positions provided that HyperTransport™ 3.0 layout and signal integrity requirements are met.

13. Riser Dimensions

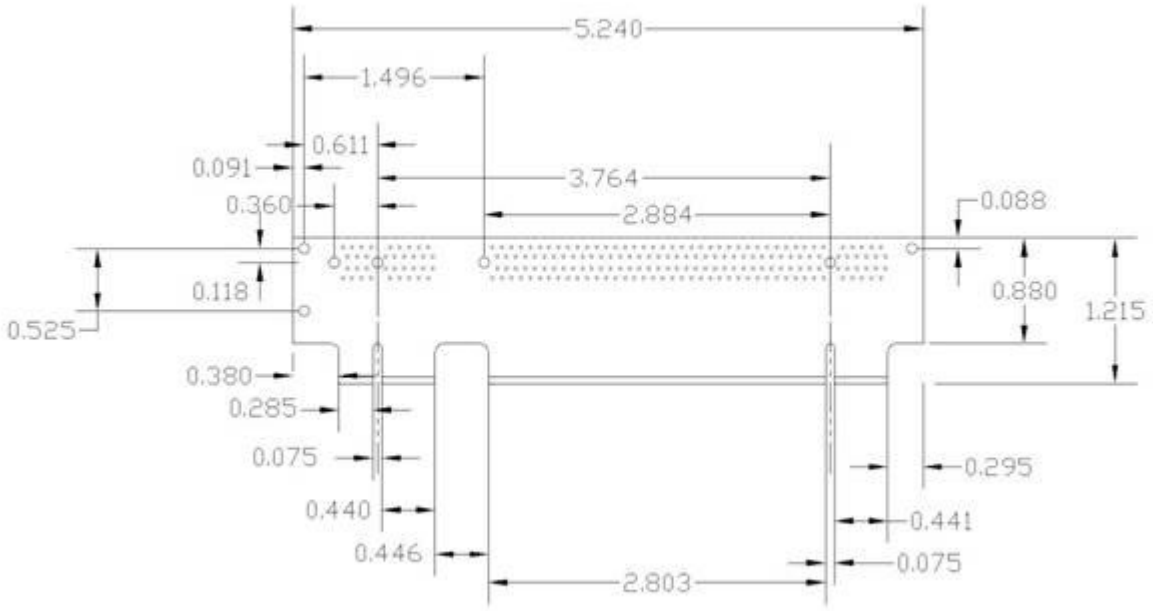


Figure 5. HTX3™ Riser for 1U Systems

The riser card allows operation of the HTX3™ daughtercard in 1U chassis. Care should be taken to ensure that the HyperTransport™ traces on the riser card are of equal length so that the effect of the riser on HyperTransport™ signal-to-signal skew is minimized. Bypass capacitors should be added between the +12V and +3.3V power planes and ground to reduce power supply ripple and noise. It is recommended that two 220uF electrolytic capacitors be used to bypass +12V and two 470uF electrolytic capacitors be used to bypass +3.3V.

a. Proprietary Risers

It is also permissible to use a propietary riser to produce the standardized horizontal HTX3™ connector as illustrated in section 4, Figure 2 from a motherboard with a proprietary connector and/or connector positioning. Designers must ensure that proper signal integrity is maintained when placing additional connectors or longer trace lengths in the signal paths.

14. Full Height Daughtercard Dimensions

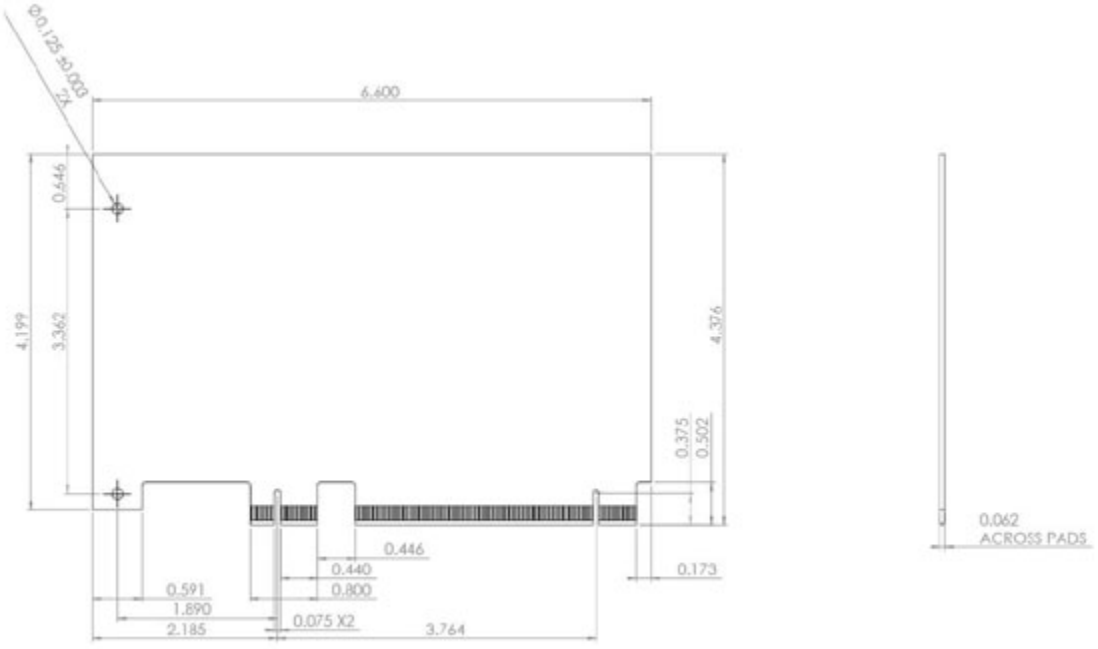


Figure 6. HTX3™ Daughtercard Outline

Figure 6 shows the mechanical outline of the HTX3™ daughtercard. Low profile card outlines are permitted provided that the mechanical integrity and placement of the faceplate mounting and connector fingers are maintained. On daughtercards which do not use the JTAG function, TDI should be jumpered to TDO to complete the JTAG chain.

15. Low Profile Daughtercard Dimensions

Figure 6 shows the mechanical outline of a full-height HTX3™ daughtercard. A low-profile form factor for use in 2U systems (or to save board area) is supported. The dimensions for the low-profile form factor are identical to the dimensions shown in Figure 6 except 1.75 inches is subtracted from the height of the board (e.g. 4.376 inches become 2.626 inches).

16. Long Daughtercard Dimensions

Figure 6 shows the mechanical outline of a full-height HTX3™ daughtercard. When extra room for components is required, a long form factor card may be used in applications where the chassis design will accommodate a long form factor card. The dimensions for the long form factor card are identical to the dimensions shown in Figure 6 except that 5.683 inches is added to the card length dimension and the distance from the edge fingers to the rear of the board (e.g. 6.600 inches and 0.173 inches become 12.283 inches and 6.124 inches, respectively). As commodity chassis generally do not support it, the combination of low-profile and long form factor is not recommended by this specification.

17. Mechanical Compatibility with PCI Express™

For maximum mechanical compatibility with chassis supporting PCI Express™ cards, it is recommended that the daughtercard designer consult the PCI Express Card Electromechanical Specification, Rev. 1.1 for the locations of component keepouts, I/O bracket dimensions, edge finger placement, mounting hole placement, optional card retainer dimensions, etc.

Appendix A - Circuit Design Considerations for FPGA-based HTX™ 3 Daughtercards

The HTX3™ specification requires the motherboard to implement PWROK as an open drain signal that may be driven by the daughtercard. In order to guarantee that an FPGA present on an HTX3™ daughtercard is initialized, the daughtercard may simply deassert PWROK (pull it low) until it has completed the initialization of the FPGA. Once PWROK is released, system initialization will occur normally. FPGA-based daughtercards which deassert PWROK in order to ensure proper completion of FPGA initialization before system startup should drive PWROK with an external component. PWROK must remain low during the entire FPGA initialization operation if this method is used.

The HTX3™ daughtercard must drive CTLIN[1:0] according to values given in Section 10, Table 4 within 100 microseconds of the assertion of PWROK,

All used CADIN lines must be driven to a logical 1 to establish the link width prior to the deassertion of RESET# (e.g. within 500 milliseconds of the assertion of PWROK).

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