HyperTransport™ Consortium

HyperTransport™ ATX/EATX Motherboard/Daughtercard Specification
Including Errata Revision F

HTX™ Connector and Form Factor Specification for HyperTransport™ Daughtercards and ATX/EATX Motherboards

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0010	Vote passed to release Errata E, add long card form factor and improved mechanical specifications		4/11/07
0011	Vote passed to release Errata F – Correction to long board dimension, change PWROK to bi-directional signal, add Appendix A, deprecate REFCLK66, specify REFCLK[H:L] as 3.3V LVPECL only for new designs	7, 16, Appendix A	12/12/2007

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1. Objective

The HTX™ Connector and Form Factor Specification for HyperTransport™ Daughtercards and ATX/EATX Motherboards allows system developers to deliver HyperTransport™ solutions using standard high-volume platforms such as Opteron™ servers. Standardized HTX™-capable motherboards will enable HyperTransport™ silicon and subsystem developers to deliver solutions based on commodity hardware—eliminating the need for custom solutions on most cases.

2. Electrical Features of the Specification

The HTX™ Connector and Form Factor Specification:

- Supports a 16-bit HyperTransport™ interface
- Daughtercards may choose to implement only 8 bits
- Runs at up to an 800MHz clock (1.6G transfers/sec). (Support for higher clock speeds is outside of the scope of this specification.)
- Provides all HyperTransport™-specific control signals, including synchronous reference clock
- Delivers both 12V and 3.3V power, up to 63 watts combined
- Provides an SMBus interface (3.3V)
- Optionally supports JTAG
- Allows use of 4-layer motherboards and daughtercards with conventional PCB technology

3. Mechanical Features of the Specification

The HyperTransport™ EATX Motherboard/Daughtercard Specification:

- Is optionally compatible with the standard ATX (12”x9.6”) and Extended ATX (12x13”) motherboard form factors
- Full height and low-profile form factors as well as short and long cards
- Daughtercard mechanical envelopes are compatible with standard PCI cards to fit in existing chassis designs
- Usable in both riser-based (1U) and pedestal, rack-mount or proprietary applications
- Uses an inexpensive, multiply-sourced commodity connector
- Placement of connectors designed to exclude the possibility of accidentally inserting cards built to other known interface specifications

4. Specification Summary

A typical HyperTransport™ dual-processor motherboard layout is illustrated in Figure 1. The slots are numbered from right to left as is the convention for extended ATX. The HyperTransport™ connectors occupy slot 6, utilizing standard PCI-Express™ 1x and 16x connectors installed in the reverse orientation of normal PCI-Express™. Slot 6 results in a design which is the most easily routable, has the shortest and most direct path for HyperTransport™, and which allows the same form factor as PCI in a 1U server. Note that the HyperTransport™ signals should route in from the right side so that the signals have the correct routing order on the daughtercard's HyperTransport™ chip. The HyperTransport™ host must reside on the motherboard.

The rest of the board's I/O infrastructure is unaffected. The function of slots 1 through 5 is application-dependent and beyond the scope of this document.

Usage note 1: At least one motherboard on the market is known to place the HTX connector in slot 5. This requires a unique daughtercard faceplate design for use in 1u applications.

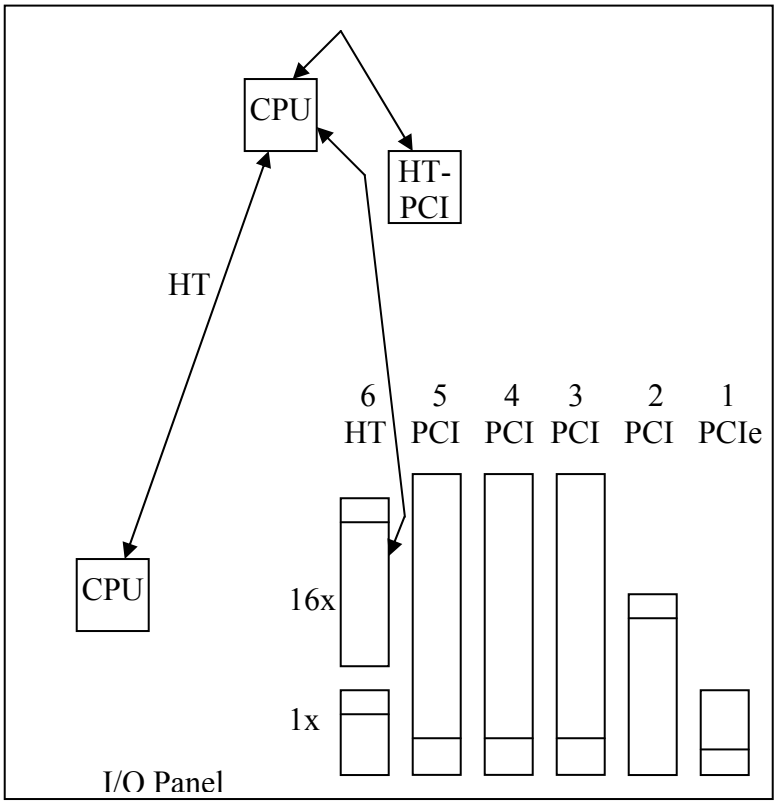

Figure 1. Typical Dual Processor HyperTransport™ Motherboard

This specification defines the mechanical locations of the connectors, pinouts, signaling conventions, mechanical specifications for the 1U riser card and HyperTransport™ daughtercard, and layout rules for motherboard, riser, and daughtercard.

A 1U system, shown in Figure 2, supports a single HyperTransport™ daughtercard using the HyperTransport™ riser, and such a HyperTransport™-enabled assembly is mechanically 100% compatible with existing 1U chassis designs.

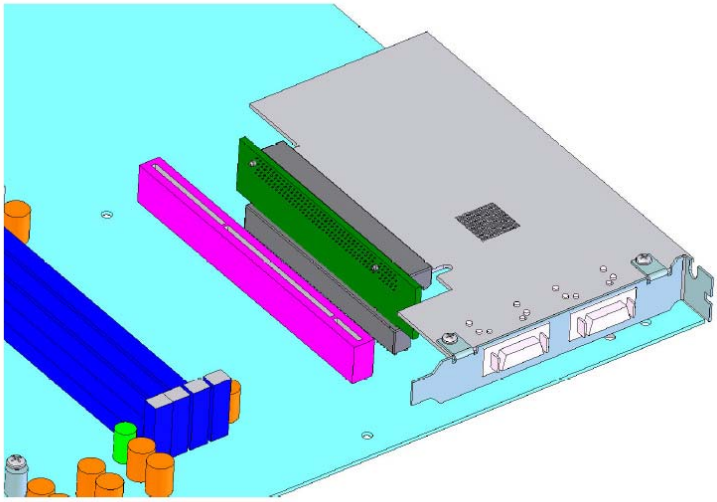

Figure 2. 1U System with Riser

A 3U or greater rack-mount or pedestal server can accommodate the full height card plugged in vertically in conjunction with other PCI and/or PCI Express™ cards, as shown in Figure 3. No change in chassis design is required. The low-profile form factor is suitable for use in 2U chassis.

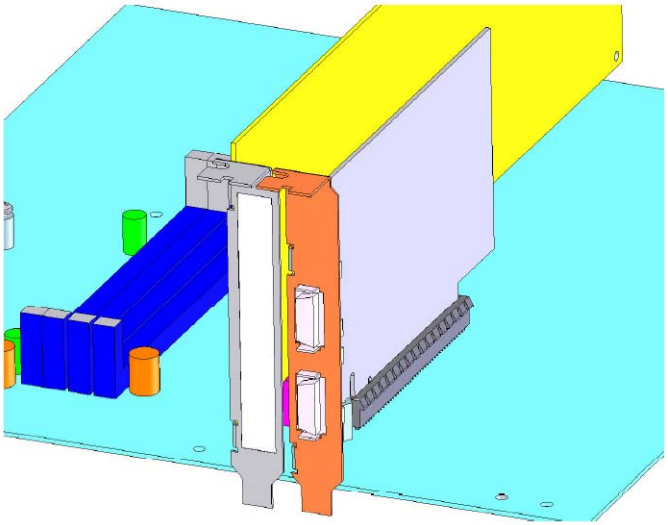

Figure 3. 3U System with Vertically Mounted HT Daughtercard

5. Connector Pinout

Pinouts for the two HyperTransport™ motherboard connectors are shown in Figure 4. Signal names are from the perspective of the motherboard, e.g. the motherboard drives CADOUT signals and receives CADIN signals, etc.

Figure 4. Connector pinouts:

Pin	A	B	Pin
1	RSVD	GND	1
2	VLDT	GND	2
3	GND	CADIN8H	3
4	GND	CADIN8L	4
5	CADIN0H	GND	5
6	CADIN0L	GND	6
7	GND	CADIN9H	7
8	GND	CADIN9L	8
9	CADIN1H	GND	9
10	CADIN1L	GND	10
11	GND	RSVD	11
12	RSVD	GND	12
13	GND	CADIN10H	13
14	GND	CADIN10L	14
15	CADIN2H	GND	15
16	CADIN2L	GND	16
17	GND	CADIN11H	17
18	GND	CADIN11L	18
19	CADIN3H	GND	19
20	CADIN3L	GND	20
21	GND	CLKIN1H	21
22	GND	CLKIN1L	22
23	CLKIN0H	GND	23
24	CLKIN0L	GND	24
25	GND	CADIN12H	25
26	GND	CADIN12L	26
27	CADIN4H	GND	27
28	CADIN4L	GND	28
29	GND	CADIN13H	29
30	GND	CADIN13L	30
31	CADIN5H	GND	31
32	CADIN5L	GND	32
33	GND	CADIN14H	33
34	GND	CADIN14L	34
35	CADIN6H	GND	35
36	CADIN6L	GND	36
37	GND	CADIN15H	37
38	GND	CADIN15L	38
39	CADIN7H	GND	39
40	CADIN7L	GND	40
41	GND	CTLINH	41
42	GND	CTLINL	42
43	CTLOUTL	GND	43
44	CTLOUTH	GND	44
45	GND	CADOUT15L	45
46	GND	CADOUT15H	46
47	CADOUT7L	GND	47
48	CADOUT7H	GND	48
49	GND	CADOUT14L	49
50	GND	CADOUT14H	50
51	CADOUT6L	GND	51

Top of connector, away from I/O Panel as viewed from the solder side of the motherboard.

RSVD and RSVDFS pins should be left *unconnected*, not grounded.

Motherboards that drive or receive USER pins should allow correct operation of daughtercards which leave these pins unconnected.

The “A” side of the daughtercard is the component side.

52	CADOUT6H	GND	52
53	GND	CADOUT13L	53
54	GND	CADOUT13H	54
55	CADOUT5L	GND	55
56	CADOUT5H	GND	56
57	GND	CADOUT12L	57
58	GND	CADOUT12H	58
59	CADOUT4L	GND	59
60	CADOUT4H	GND	60
61	GND	CLKOUT1L	61
62	GND	CLKOUT1H	62
63	CLKOUT0L	GND	63
64	CLKOUT0H	GND	64
65	GND	CADOUT11L	65
66	GND	CADOUT11H	66
67	CADOUT3L	GND	67
68	CADOUT3H	GND	68
69	GND	CADOUT10L	69
70	GND	CADOUT10H	70
71	CADOUT2L	GND	71
72	CADOUT2H	GND	72
73	GND	CADOUT9L	73
74	GND	CADOUT9H	74
75	CADOUT1L	GND	75
76	CADOUT1H	GND	76
77	GND	CADOUT8L	77
78	GND	CADOUT8H	78
79	CADOUT0L	GND	79
80	CADOUT0H	GND	80
81	GND	USER	81
82	RSVD	GND	82

Pin	A	B	Pin
1	GND	USER[2]	1
2	REFCLKL	GND	2
3	REFCLKH	GND	3
4	GND	RSVDFS	4
5	GND	RSVDFS	5
6	RSVDFS	GND	6
7	RSVDFS	PWROK	7
8	LDTSTOP#	RESET#	8
9	+3.3Vaux	+3.3V	9
10	TRST#	+3.3V	10
11	+3.3V	TMS	11
12	GND	TDO	12
13	SMDAT	TDI	13
14	SMCLK	TCK	14
15	GND	GND	15
16	RSVDFS	+12V	16
17	+12V	+12V	17
18	+12V	RSVDFS	18

Bottom of connector, near I/O panel

Note 2: Prior to Revision 11, pin B1 of the small connector was REFCLK66, a 66 MHz reference clock. Use of this signal is now deprecated for new designs.

Unshaded pins are staggered closer together in the connector than shaded pins.

Pinout considerations include:

- No high-speed signals at connector edge
- Dedicated ground next to every high-speed signal
- HyperTransport™-specific control and power signals closer to top of connector

- Ordering of HyperTransport™ interface matches standard device pinout
- Pinout near I/O panel similar to PCI-Express™ pinout for ease of bussing

6. Power distribution

Power specifications, shown in Figure 5, are identical to 16x PCI-Express™ with the addition of VLDT.

Power supply	Voltage	Tolerance	Current
+12V	12V	±8%	4.4A
+3.3V	3.3V	±9%	3A
+3.3Vaux	3.3V	±9%	375ma
VLDT	1.2V	±5%	1A

Figure 5. Power specifications

7. Signal Description Summary

Figure 6 provides a description of the signals on the HyperTransport™ connectors. "MB" refers to motherboard and "DC" refers to daughtercard.

Figure 6. Connector Signal Characteristics

Signal name	Count	Direction	Level	Description	Required MB	Required DC
+12V	4	In	Power	12V power	Yes	Yes
+3.3V	3	In	Power	3.3V power	Yes	Yes
+3.3Vaux	1	In	Power	3.3V auxiliary power	Yes	Yes
VLDT	1	In	Power	1.2V HT power	Yes	Yes
GND	91	Common	Ground	Signal ground	Yes	Yes
CADIN[15:8][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	No	No
CADIN[7:0][H:L]	8 pairs	DC→MB	LDT diff	HT data/command	Yes	Yes
CLKIN1[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	No
CLKIN0[H:L]	1 pair	DC→MB	LDT diff	HT clock	Yes	Yes
CTLIN[H:L]	1 pair	DC→MB	LDT diff	HT control	Yes	Yes
CADOUT[15:8][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	No	No
CADOUT[7:0][H:L]	8 pairs	MB→DC	LDT diff	HT data/command	Yes	Yes
CLKOUT1[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	No
CLKOUT0[H:L]	1 pair	MB→DC	LDT diff	HT clock	Yes	Yes
CTLOUT[H:L]	1 pair	MB→DC	LDT diff	HT control	Yes	Yes
LDTSTOP#	1	MB→DC	2.5V CMOS	HT LDTSTOP	Yes	Yes
PWROK	1	Bidir[5]	2.5V CMOS	HT power OK	Yes	Yes
RESET#	1	Bidir[3]	2.5V CMOS	HT reset	Yes	Yes
REFCLK[H:L]	1 pair	MB→DC	3.3V diff LVPECL[4]	200MHz HT reference clock	Yes	Yes
SMCLK	1	MB→DC	3.3V CMOS	SMBus clock	Yes	No
SMDAT	1	Bidir	3.3V CMOS	SMBus data	Yes	No
TCK	1	MB→DC	3.3V CMOS	JTAG clock	No	No
TMS	1	MB→DC	3.3V CMOS	JTAG mode select	No	No
TRST#	1	MB→DC	3.3V CMOS	JTAG reset	No	No
TDI	1	MB→DC	3.3V CMOS	JTAG data in	No	No
TDO	1	DC→MB	3.3V CMOS	JTAG data out	No	No
USER	2	User	User	User-defined	-	-
RSVD	4	-	-	Reserved, do not connect	-	-
RSVDFS	6	-	-	Reserved, future standardization	-	-

Usage note 3: At least one motherboard on the market is known to drive RESET# with LVTTL instead of an open drain driver.

Usage note 4: Prior to Revision 11, REFCLK[H:L] was optionally driven with 2.5V CMOS. This practice is now deprecated.

Usage note 5: Prior to Revision 11, PWROK was driven only by the motherboard. Older boards might not be able to support daughtercards which drive PWROK.

a. Routing Rules

The HyperTransport™ connector should be considered a “zero mismatch boundary” as defined in Section 2.3.6.2 of the HyperTransport™ Interface Design Guide, Rev. 1.07. Motherboard and daughtercard routing should comply with the Interface Design Guide using this assumption. This allows the routing for the motherboard and the daughtercard to be independent and interoperable.

Trace lengths for HyperTransport™ signals on the motherboard should not exceed 9.25 inches. Trace lengths on the daughtercard should not exceed 2.75 inches. This will ensure that the total trace length will not exceed the maximum allowed 12 inches for 800 MT/sec operation.

b. RESET# and PWROK

RESET# may optionally be driven by the daughtercard. Motherboards and daughtercards should implement RESET# using open drain drivers. A pullup resistor of value greater than or equal to 1K ohms shall be placed on the motherboard. A minimum of 500 milliseconds should be allotted between the assertion of PWROK and the deassertion of RESET# to allow time for the initialization of any FPGAs on the daughtercard.

PWROK may optionally be driven by the daughtercard. Motherboards and daughtercards should implement PWROK using open drain drivers. A pullup resistor of value greater than or equal to 1K ohms shall be placed on the motherboard. (N.B. This is a change to the HTX specification as of Revision 11. For backwards compatibility with previous versions of HTX, see Appendix A.)

8. Signal Integrity

Signal integrity shall be measured according to the HyperTransport™ Electrical Compatibility Measurements Rev. 0.03, HyperTransport Technology Consortium document number HTC20021219-0018-0001.pdf, and shall be compliant with the HyperTransport I/O Link Specification, Rev. 2.0.

9. Higher Speed Operation

Operation at speeds higher than 800 MT/sec is outside the scope of this specification. However, the connectors used are known to work at higher speeds in PCI-Express™ applications. Designers are urged to minimize trace lengths and signal skew to achieve best results at higher speeds.

10. 8-bit Link Support

If a daughtercard only supports an 8-bit HyperTransport link, then it must tie CADIN[15:8]H and CLKIN1H to GND through 51 ohm resistors and CADIN[15:8]L and CLKIN1L to VLDT through 51 ohm resistors.

11. Unused HyperTransport Slot

In the event that the HyperTransport™ slot is unused, an optional terminator board of the same form factor as the HyperTransport™ daughtercard or the same form factor as the HyperTransport™ riser card may be provided to prevent floating inputs and/or jumper the JTAG chain. This board should tie CADIN[15:0]H, CLKIN[1:0]H and CTLINH to GND through 51 ohm resistors and CADIN[15:0]L, CLKIN[1:0]L and CTLINL to VLDT through 51 ohm resistors. TDI should be jumpered to TDO to complete the JTAG chain.

12. Motherboard Dimensions and Connector Placement

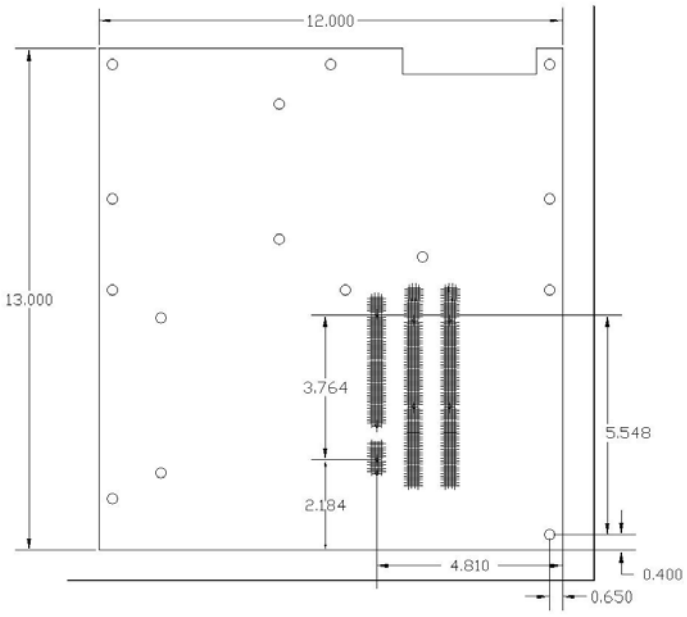

Figure 7. EATX Motherboard with HyperTranport™ Connector in Slot 6 Position

The example shown in Figure 7 is an EATX motherboard with the HyperTransport™ connector in the position normally occupied by PCI slot 6. Placing the HyperTransport™ connector in the slot 6 position permits operation with a riser, allowing the use of a 1u enclosure. Proprietary designs may place the HyperTransport™ connector in any of the PCI slot positions provided that HT layout and signal integrity requirements are met.

13. Riser Dimensions

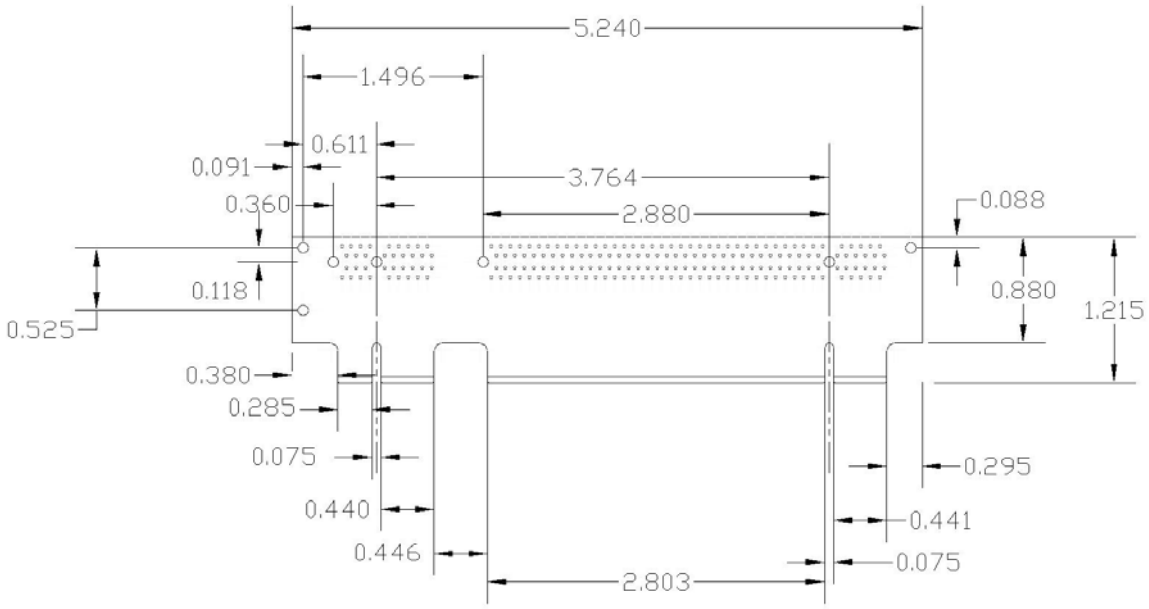

Figure 8. HT Riser for 1U Systems

The riser card allows operation of the HyperTransport daughtercard in 1U chassis. Care should be taken to ensure that the HyperTransport traces on the riser card are of equal length so that the effect of the riser on HyperTransport™ signal-to-signal skew is minimized. Bypass capacitors should be added between the +12V and +3.3V power planes and ground to reduce power supply ripple and noise. It is recommended that two 220uF electrolytic capacitors be used to bypass +12V and two 470uF electrolytic capacitors be used to bypass +3.3V.

a. Proprietary Risers

It is also permissible to use a propietary riser to produce the standardized horizontal HTX connector as illustrated in section 4, Figure 2 from a motherboard with a proprietary connector and/or connector positioning.

Usage note 6: At least one motherboard on the market is known to reproduce the standardized horizontal HTX connector with trace lengths that slightly exceed the recommended length.

14. Full Height Daughtercard Dimensions

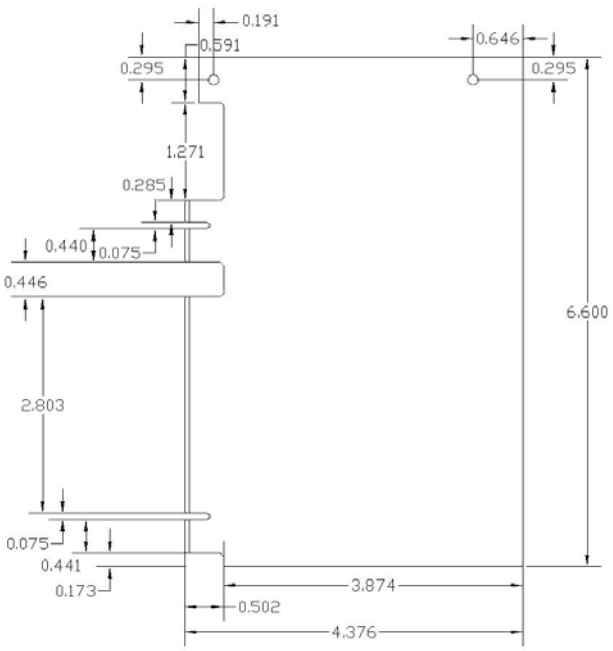

Figure 9. Daughtercard Outline

Figure 9 shows the mechanical outline of the daughtercard. Low profile card outlines are permitted provided that the mechanical integrity and placement of the faceplate mounting and connector fingers are maintained. On daughtercards which do not use the JTAG function, TDI should be jumpered to TDO to complete the JTAG chain.

15. Low Profile Daughtercard Dimensions

Figure 9 shows the mechanical outline of a full-height daughtercard. A low-profile form factor for use in 2U systems (or to save board area) is supported. The dimensions for the low-profile form factor are identical to the dimensions shown in Figure 9 except 1.75 inches is subtracted from the two dimensions shown near the bottom of the drawing (e.g. 3.874 inches and 4.376 inches become 2.124 inches and 2.626 inches, respectively).

16. Long Daughtercard Dimensions

Figure 9 shows the mechanical outline of a full-height daughtercard. When extra room for components is required, a long form factor card may be used in applications where the chassis design will accommodate a long form factor card. The dimensions for the long form factor card are identical to the dimensions shown in Figure 9 except that 5.683 inches is added to the card length dimension and the distance from the edge fingers to the rear of the board (e.g. 6.600 inches and 0.173 inches become 12.283 inches and 6.124 inches, respectively).

Usage note 5: A low-profile long form factor card is not supported.

17. Mechanical Compatibility with PCI Express™

For maximum mechanical compatibility with chassis supporting PCI Express™ cards, it is recommended that the daughtercard designer consult the PCI Express Card Electromechanical Specification, Rev. 1.1 for the locations of component keepouts, I/O bracket dimensions, edge finger placement, mounting hole placement, optional card retainer dimensions, etc.

Appendix A - Circuit Design Considerations for FPGA-based HTX™ Daughtercards

Since the introduction of the HTX™ standard, several companies and at least one university have developed HTX™ daughtercards using FPGA technologies. As FPGAs have grown larger and more complex, their initialization times have increased. Some users have observed problems with HTX™ designs caused by lengthy FPGA initialization times.

The purpose of this appendix is to summarize the problems and present design choices available to developers of FPGA-based HTX™ cards and systems.

a. Problems Caused by Long FPGA Initialization Times

If an FPGA used as a HyperTransport™ interface is not initialized in time to respond to the processor during a cold reset, the HTX™ device may be ignored completely, the system may hang or it may exhibit unpredictable behavior.

The problems may be complicated by:

1) Differences in expected behavior between Gen1 and Gen3 HyperTransport™ devices,

2) New requirements of Family 10h Opteron™ processors, and

3) Vendor-specific implementations of RESET# and PWROK circuits on available HTX™ motherboards

b. Background Information

The HTX™ specification was released in October of 2004. Very early in the specification process, the Technical Working Group decided to redefine the RESET# signal on the HTX™ connector as “bidirectional”, e.g. open drain. It was then thought that making RESET# an open drain signal would provide HTX™ daughtercard devices with a mechanism sufficient to delay system

initialization so that FPGA devices would have time to initialize themselves. The first HTX™ motherboards, developed prior to the approval of the draft specification, did not implement RESET# as an open-drain signal. A footnote was added to the specification notifying developers of this fact.

Prior to Revision 11, the HTX™ specification defined the PWROK signal as a single ended CMOS signal driven from the motherboard to the daughtercard.

Prior to Family 10h, Opteron processors did not sample any of the Hyptertransport™ signals until the deassertion of RESET#. Family 10h processors have been designed to sample the CTL[1:0] lines at approximately 300 microseconds after the assertion of PWROK to determine if a device is present on a given HT port. Unfortunately, Family 10h processors do not wait for the deassertion of RESET#. Therefore, the existing HTX™ mechanism, prior to Revision 11, of extending RESET# until FPGA initialization has completed is inadequate for Opterons of Family 10h and later.

c. HTX™ Cold Reset Sequence

Section 12.2 of the HyperTransport™ 3.0 Specification contains the following paragraph:

"While RESET# is asserted during a cold reset, each device's transmitter drives CLK on all implemented byte lanes, drives its CTL signals to a logical 0, and drives all implemented output CAD signals to a value that is based on the width of its receiver, according to Table 111. Gen1 devices and Gen3 devices that are DC-coupled must hold this value through reset. In Gen1 protocol, CAD must be held until after the device has asserted its own CTL signal and sampled the assertion of the CTL signal driven from the other device. (This assures that each device can sample CAD safely, even if the devices takes considerable time after reset to stabilize clocks and sample CAD.) If the transmitter is narrower than the receiver, all the output CAD signals are driven to a logical 1."

Unfortunately, this requirement does not take into account the fact that the FPGA logic to drive the CTL signals may be uninitialized at the assertion of RESET#. We are forced, then, to examine how the relevant HyperTransport™ devices actually work and design the FPGA circuit accordingly.

The following figure illustrates the sequence of events at the HTX™ connector pins during a cold start:

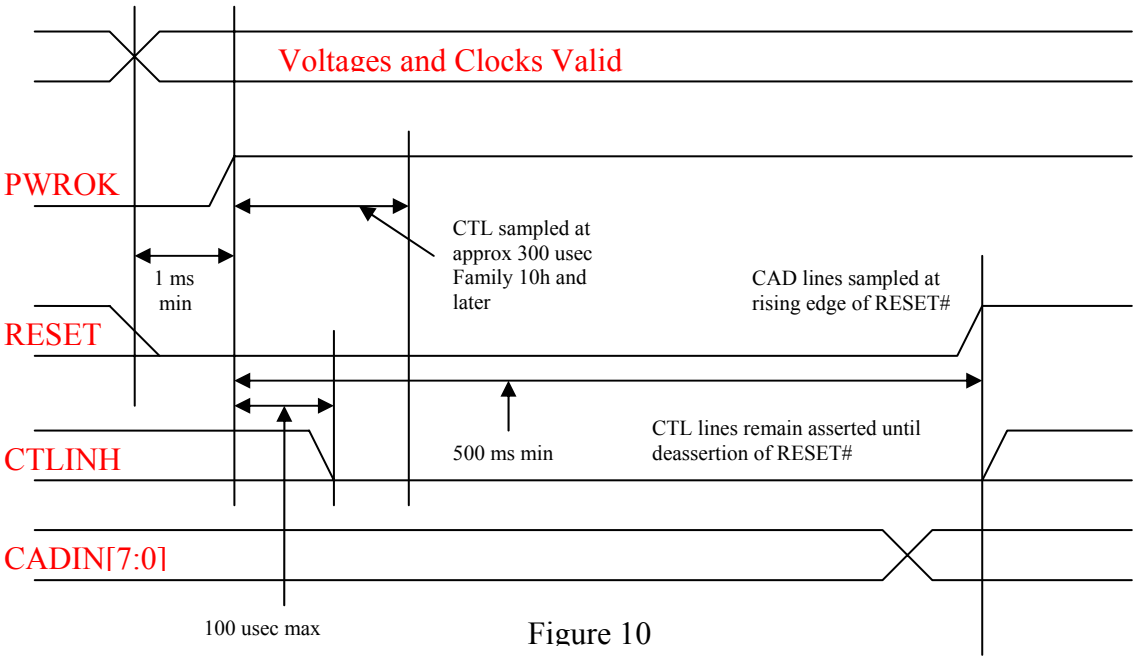

Figure 10

The HTX™ daughtercard must, therefore, meet the following requirements to be operate correctly with all families of Opteron™processors and existing HTX motherboards:

CTLIN must be driven to a logical 0 within 100 microseconds of the assertion of PWROK,

All eight of the CADIN[7:0] lines must be driven to the appropriate value (normally FFh) to establish the link width prior to the deassertion of RESET# (e.g. within 500 milliseconds of the assertion of PWROK).

d. Design Option 1 – Open Drain PWROK

If the motherboard's implementation of PWROK is compliant with Revision 11 of the HTX specification (e.g. it implements open drain PWROK) then the daughtercard may simply deassert PWROK until it has completed the initialization of the FPGA. Once PWROK is released, system initialization will occur normally.

e. Design Option 2 – Delaying PWROK

System designers who have control over the operation of the motherboard may simplify things considerably by increasing the time from "voltages and clocks valid" to the assertion of PWROK from the 1 millisecond specified in the HyperTransport™ specification to a time long enough to initialize the FPGA. In this scenario, the HTX™ daughtercard has its own "Power OK" circuit to detect that supply voltages are within acceptable values and initializes the FPGA before the motherboard asserts the PWROK signal at the HTX™ connector.

The advantage to this scenario is that no additional components are required on the HyperTransport™ signals. The disadvantage is that this is only possible if the designer can modify the motherboard's PWROK circuit.

e. Design Option 3 – The "FET" Solution

If the FPGA device can be initialized within 500 milliseconds after the assertion of PWROK (e.g. it can meet the CAD, but not the CTL timing requirements), a pair of FETs may be added to the daughtercard for the purpose of driving CTLIN[H,L] to a logic 0 during the assertion of RESET# while the FPGA is being initialized.

If the FPGA initialization time is too long to assure proper assertion of CADIN[H,L] and the HTX™ motherboard implements the open-drain RESET# signal, the daughtercard may assert RESET# in order to extend its duration until the FPGA initialization is complete and the FPGA can properly drive the CADIN[7:0] signals.

Finally, if the motherboard does *not* implement the open-drain RESET# signal, FETs may be added to the daughtercard for the purpose of driving CTLIN[H,L] to a logic 0 during the assertion of RESET# and placing the proper value on CADIN[7:0] while the FPGA is being initialized.

The disadvantages to the "FET solution" are 1) increased complexity and component count and 2) routing difficulties and possible signal integrity problems caused by the need to route up to eighteen FETs on the HyperTransport™ signals of the daughtercard. The advantage is that this solution, properly implemented, will work with existing HTX™ motherboards.

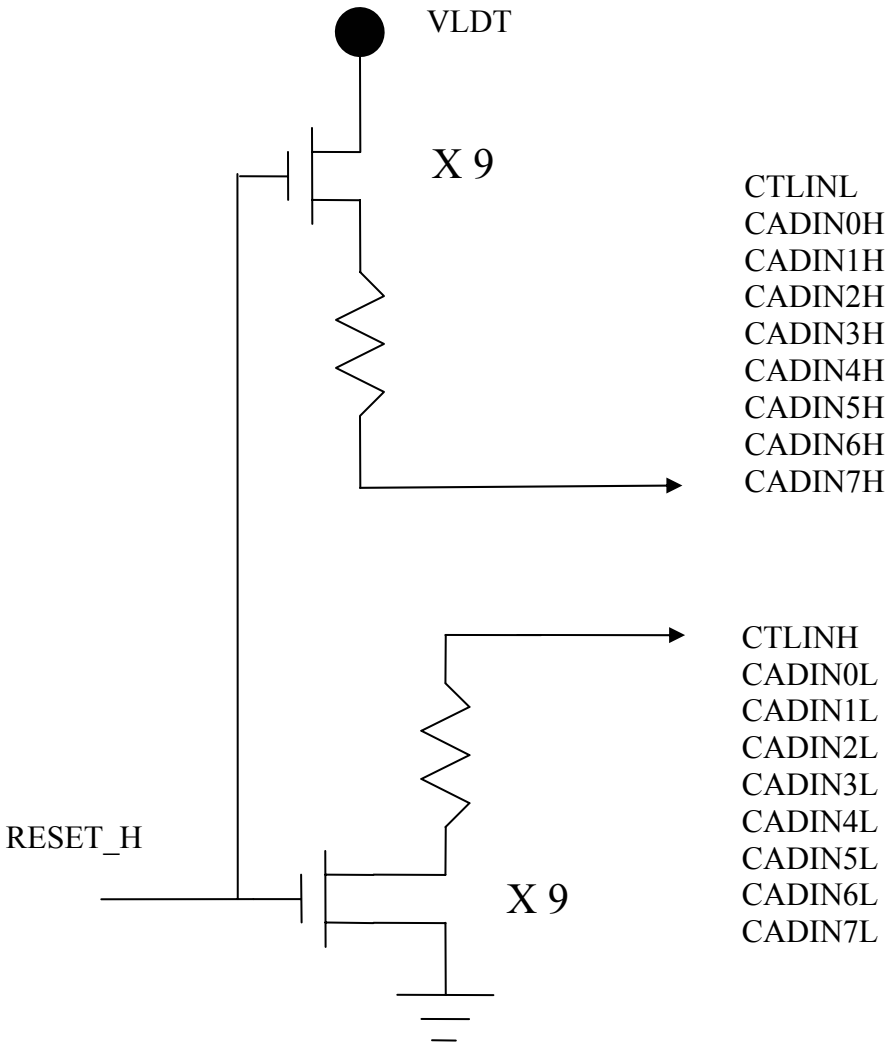
VLDT
X 9
CTLINL
CADIN0H
CADIN1H
CADIN2H
CADIN3H
CADIN4H
CADIN5H
CADIN6H
CADIN7H
CTLINH
CADIN0L
CADIN1L
CADIN2L
CADIN3L
CADIN4L
CADIN5L
CADIN6L
CADIN7L
RESET_H
X 9

Figure 11

For more information on HyperTransport technology please visit the HyperTransport Consortium website at www.hypertransport.org where additional white papers, detailed specifications and information on becoming a member of the HyperTransport Consortium is available.

A low-cost membership in the Consortium enables member companies to have royalty-free access to HyperTransport IP and to participate in technical working groups that define specifications and guide new additions to extend the technology to support future industry protocols.