HS 4540 KEY TECHNOLOGIES

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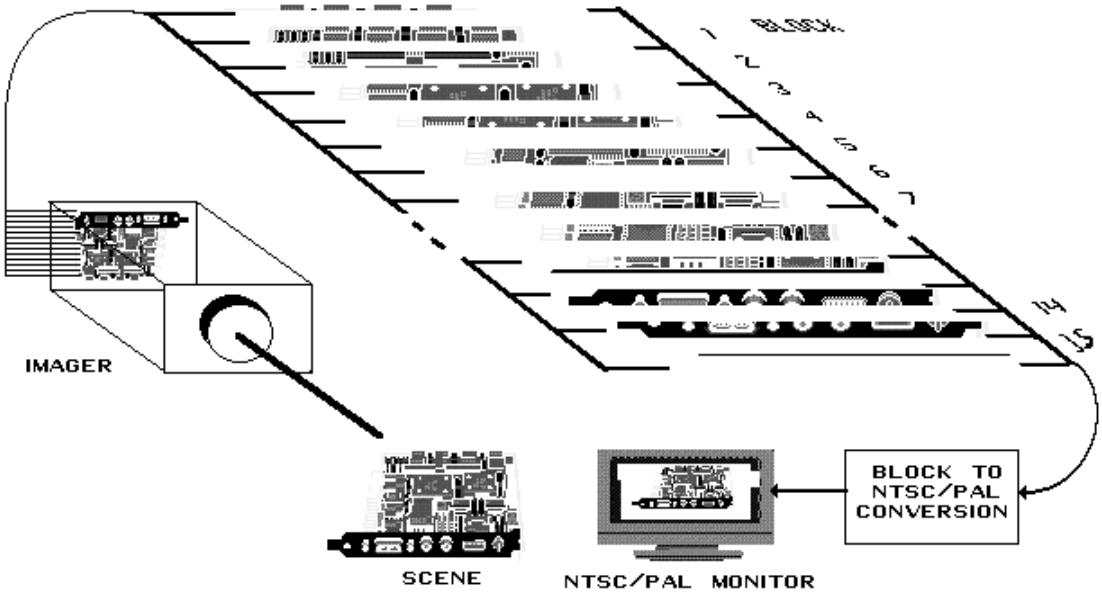
BLOCKED VIDEO FORMAT

The video format used by the EktaPro HS 4540 motion analyzer was based on the same technique utilized in the EktaPro 1000 motion analyzer and the SP 2000 Motion Analysis System. The video format breaks the single high-speed video channel into many parallel channels, each of moderate bandwidth. This approach simplifies the signal processing functions compared to handling one very complex channel. The pixel on any given channel is immediately preceded and followed by pixels located adjacent on the same picture line. The pixels present on adjacent channels are from adjacent physical lines of the picture. This creates a high correlation of adjacent pixels in a physical image. This helps to prevent introduction of picture artifacts by the scanning process. This parallel block readout from a sensor is covered under a Kodak patent.



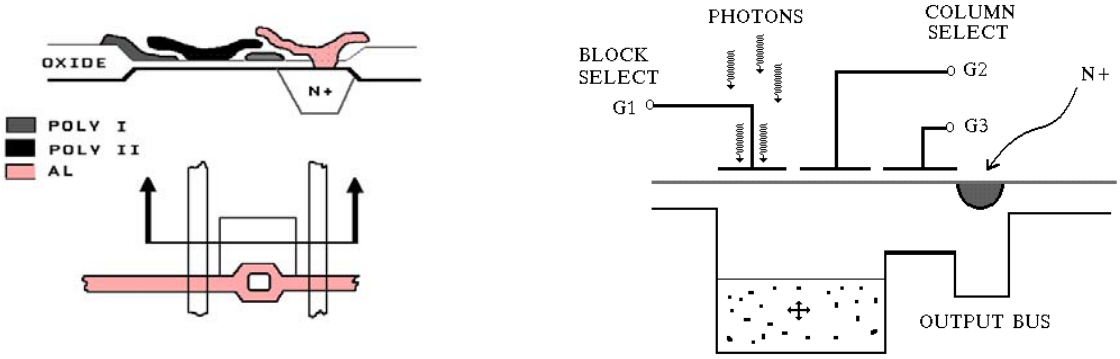
The figure above illustrates the parallel blocked image format. The image is divided into sixteen horizontal blocks, each of 16 lines, for 256 horizontal lines per picture. A video frame consists of sixteen block read-out intervals. During block 1, the data for picture line 1 is sequentially scanned to signal line 1, picture line 2 to signal line 2, and so on, up to line 16. During block 1, the first 16 lines are scanned with an output interval. The second set of 16 picture lines is scanned with an output to the 16 signal channels. This process continues until all sixteen blocks have been scanned. The sequence repeats to read the next frame.

IMAGING SENSOR

Technology used in the EktaPro HS4540 imager incorporates a solid-state NMOS sensor. This sensor captures the optical image by tessellating the incident light into a 256 by 256 picture elements (pixels)array.

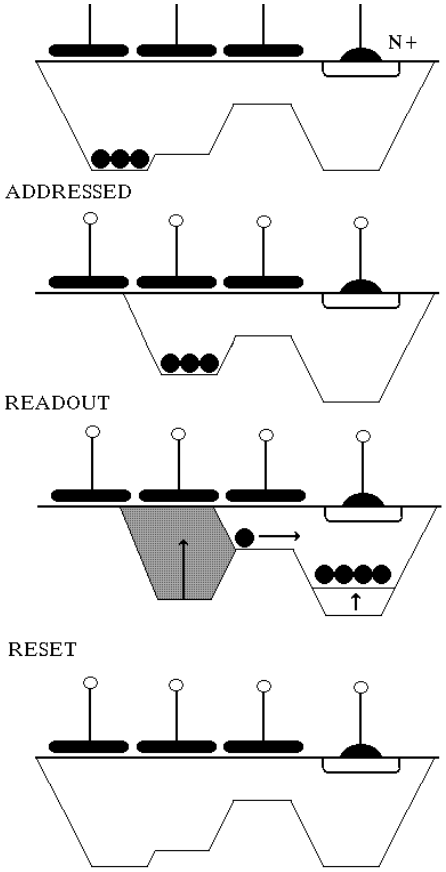
This sensor operates at 4500 full frames per second. The light energy is converted into an electrical charge by a photo capacitor. The photo capacitor is the photosensitive element called a pixel. The pixel dimension is 40.0 microns square. Eighty percent of the pixel area is light sensitive.

The operation and control of one pixel within the sensor is illustrated in the figure below. A pixel consists of a MOS photo capacitor formed under gates G1 and G2. Gate G3 provides a DC potential barrier to isolate the photo capacitor from the N+ output bus. This bus runs the



entire length of a row. During charge accumulation, G1 and G2 are held at a negative voltage, which creates a potential well beneath the photo capacitor electrodes. Photons may pass through the polysilicon material of G1 to create hole-electron pairs. The electrons are swept out of the region. The holes are captured in a depletion zone under the electrodes. The charge continues to integrate as photons create hole-electron pairs, until the cell is scanned during read-out. This read-out cycle occurs when the G2 column electrode is pulsed to ground by the column scanner. First, G1 is grounded for the block scanned. This moves the photocharge under the G2 electrode in the selected block. Next, G2 is pulsed to ground. In the enabled block, charge is forced over the G3 barrier and onto the output bus. This bus is a floating capacitor. The signal is detected as a change in voltage on the bus due to the injected photo-charge. In the blocks, which are not enabled, the G2 electrode is pulsed. This moves the photocharge temporarily under the G1 capacitor electrode. After the charge has been sensed on the output bus, the bus is reset to a reference voltage. This is in preparation for reading the next pixel. G2 is returned to its negative level to begin accumulating charge.

The sensor full well potential is approximately 40,000 electrons. The sensor provides good sensitivity and excellent blooming insensitivity.


N+
ADDRESSED
READOUT
RESET