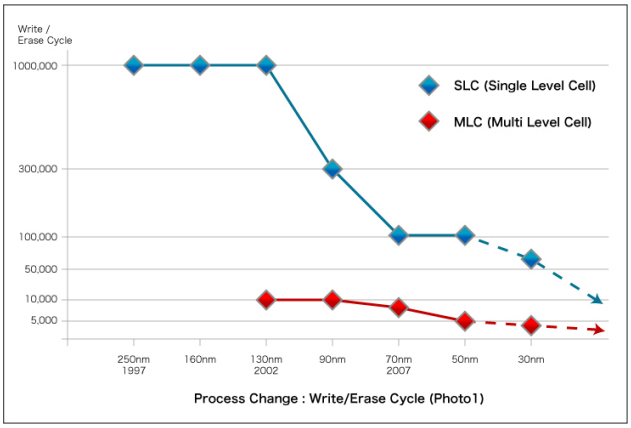
TECHNOLOGY FOR MANAGING NAND FLASH

WHAT IS TO SELECT SSD OF CRITERION FOR EMBEDDED APPLICATIONS?

1. Compensating the effects of NAND Flash Design-Rule Shrink in relation to SSD reliability

In the embedded computing market, non-volatile flash memory solutions, also referred to as solid state drives (SSD), have been widely utilized in various applications over the past decade. The inherent high physical tolerances to temperature, shock and vibration and low power consumption have allowed flash memory solutions to be utilized in situations that are otherwise very difficult for conventional hard disk solutions without costly modifications and improvements. It has been thought by many that flash memory solutions could store data semi-permanently.

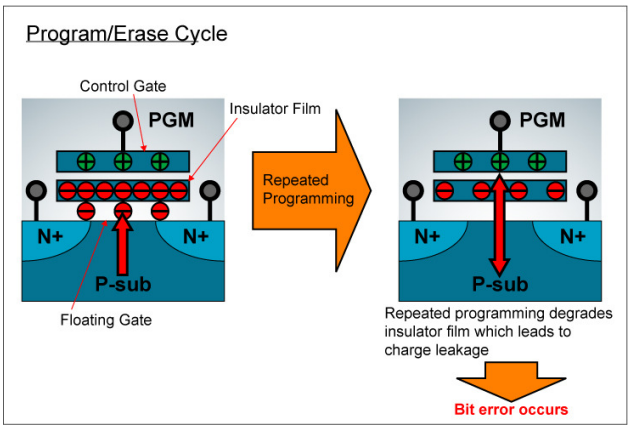
But recent new developments of flash memory require re-evaluation of this belief. The current consumer market demands force NAND flash design-rule shrink in order to increase density and cost performance. Unfortunately, this process affects attributes of the NAND flash that degrade device reliability, thus requiring SSD vendors to design and implement measures to compensate. The two most affected are "Program/Erase Cycle" and "Read Disturb".



In order to deal with these issues, the SSD device must have the capability to monitor and obtain accurate Program/Erase Cycle Count and Read Count internally based on the user's actual usage.

Program/Erase Cycle

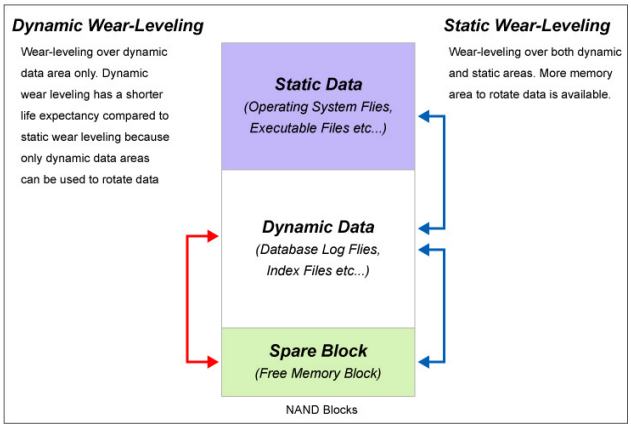
In general terms, "Program/Erase Cycle" refers to how many times a single data block within the NAND flash can be written which correlates to the device life.



Design-rule shrink affects the insulator film, reducing tolerance due to repeated programming. For this reason, current 56nm MLC NAND flash can only tolerate 5,000 program cycles where in comparison older 90nm MLC NAND flash could tolerate 10,000 program cycles.

Wear-leveling

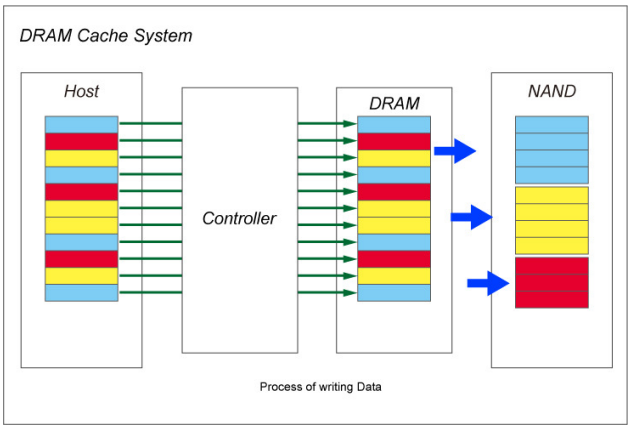
A method known as wear-leveling evenly distributes the program/erase over the entire medium in order to extend the life of SSD. Currently there are two types of wear-leveling algorithms, Dynamic Wear-leveling and Static Wear-leveling.



In the past, the more tolerant, earlier generations of NAND flash were managed by Dynamic Wear-Leveling, a simpler algorithm that utilizes only the dynamic area for wear-leveling. But due to increased issues of reliability with newer generation NAND flash, a more advanced and complex method, Static Wear-Leveling, which utilizes both static and dynamic areas for wear-leveling, is becoming more prominent in future SSD designs.

Cache

Another method for addressing the limited program cycle is by utilizing on-board DRAM cache. An SSD without cache programs data in the order received in small fragmented data blocks over multiple times, resulting in high inefficient programming.

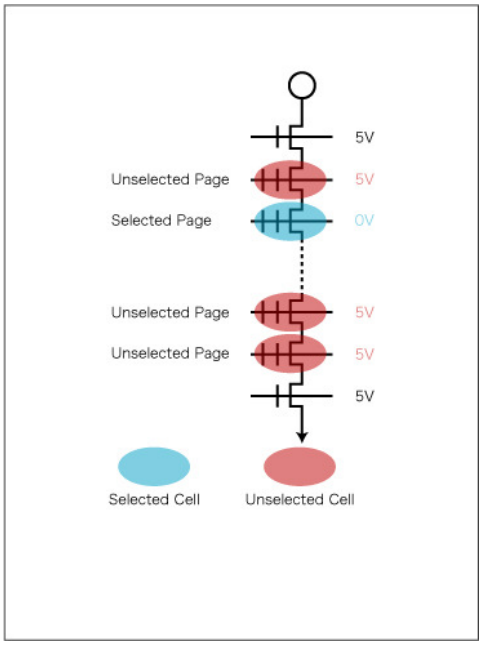


By effectively utilizing cache to temporarily store fragmented data, which is organized into larger blocks of data, the SSD can avoid inefficient programming and gain an improvement of NAND flash longevity.

A positive side effect of having on-board cache is a drastic improvement of random access due to reduced host command overhead.

Read Disturb

"Read Disturb" is an anomaly caused by very high number of read access which can actually reduce the voltage in the surrounding cells resulting in erroneous data stored. Although ECC (Error Correcting Code) can detect and fix the data where the electrical properties may have been altered, a method known as "Refresh" re-writes ("*re-charges*") the stored data to prevent "Read Disturb" from occurring.



Summary

As the market demand rises, advancements in NAND flash technology will continue. And the issues associated with NAND flash design-rule shrink will progressively become more complex. There will be a need for further development and enhancements in controller designs including accurate information collection and reporting technologies to insure better SSD reliability.

Unlike with previous more tolerant NAND, flash memory solution vendors must take steps to meet these advancements and it will become increasingly important to have a better working knowledge of NAND flash management and controller functionality.

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