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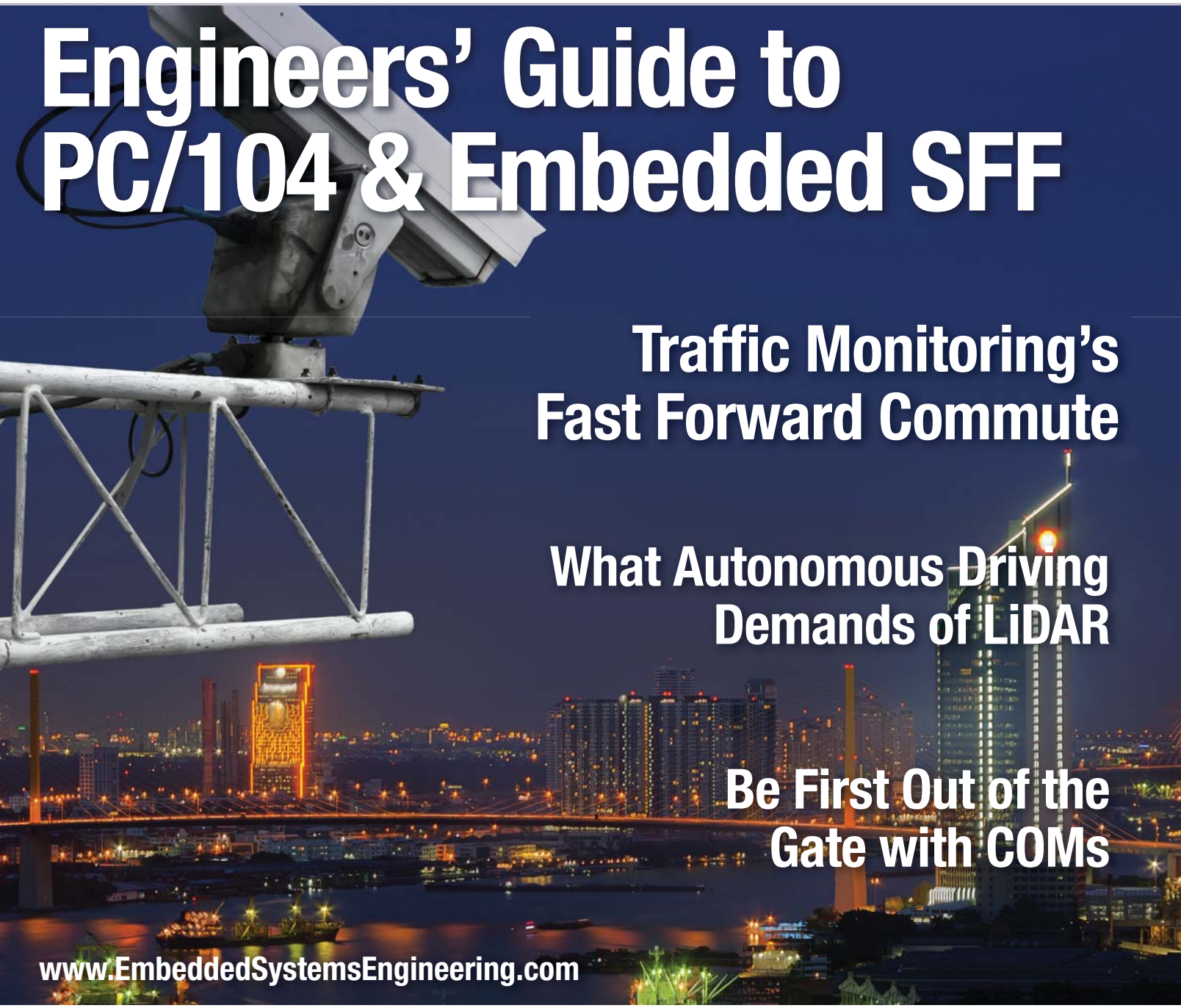

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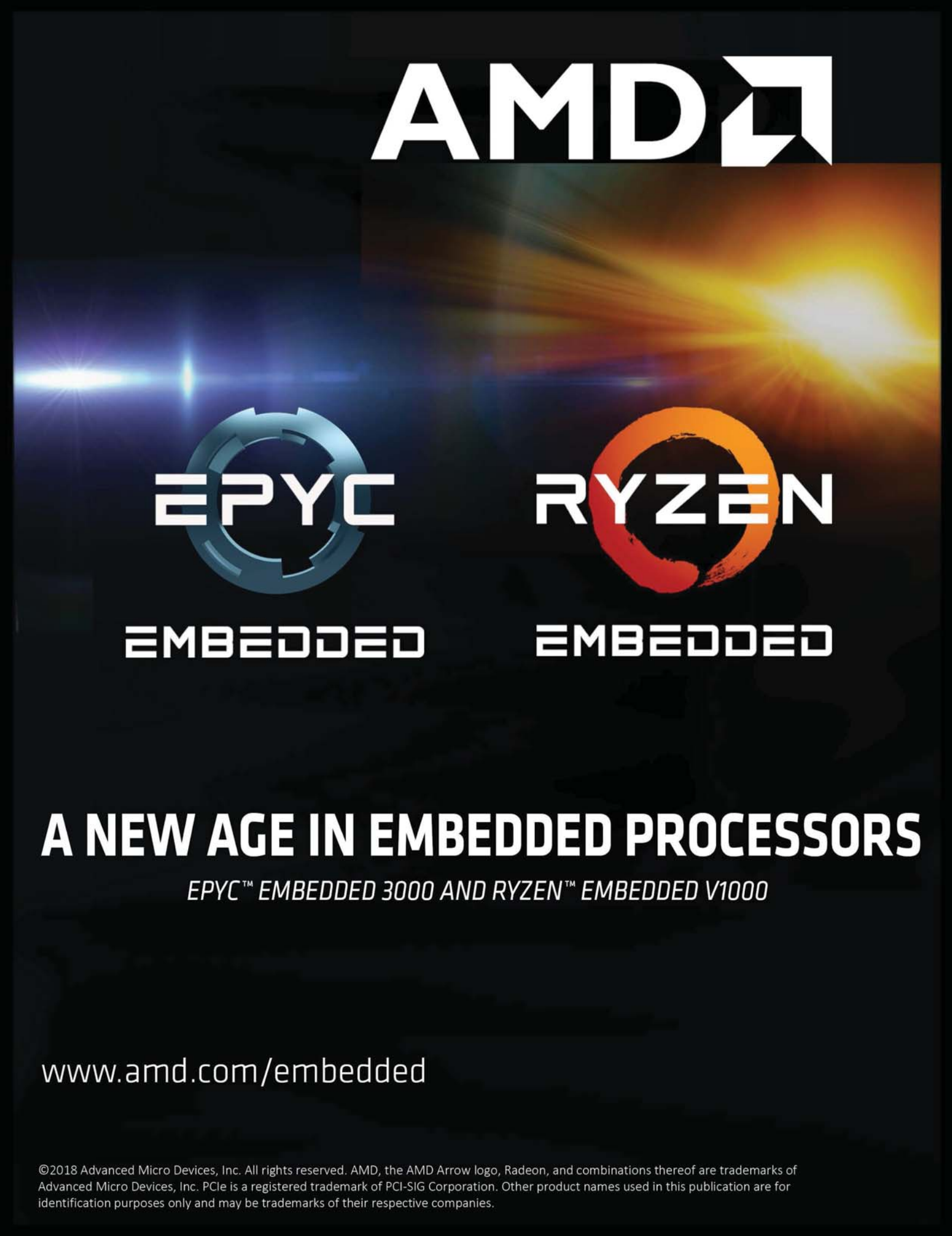

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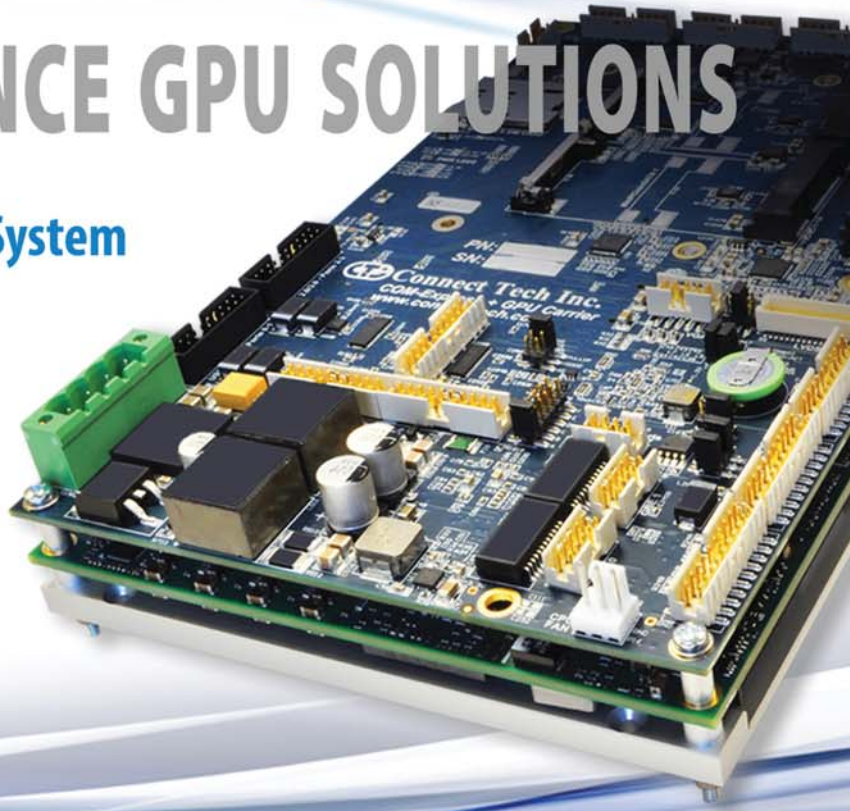

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Taking a Risk on RISC-V, an Open Source ISA

The payoff could include increased transparency, with time savings and error avoidance

By Lynnette Reese, Editor-in-Chief, Embedded Systems Engineering

RISC-V is an open Instruction Set Architecture (ISA), named thus because it is the fifth Reduced Instruction Set Computer (RISC) ISA developed at UC Berkeley. The base ISA was designed to be simple, clean, and similar to other RISC instruction sets. In 2015, RISC-V was officially kicked off by the RISC-V Foundation as a zero cost, royalty- and paperwork-free ISA. Today, there are three different RISC-V instruction sets with address sizes in 32-, 64-, and 128-bits. The RISC-V Foundation, with more than 100 members, believes that RISC-V has potential to dominate computing from embedded and small form factors all the way to warehouse servers. The Foundation creates and manages working groups to guide future development. RISC-V Foundation members include Berkeley Architecture Research, Google, Microsemi, NVIDIA, Qualcomm, Western Digital, IBM, NXP, Samsung, Express Logic, Siemens, and many others.

Why not have a standard ISA? An ISA is a vital interface where hardware meets software. After several decades, computing seems to have reached a consensus favoring Reduced Instruction Set Computers (RISC). Even Complex Instruction Set Computers (CISC) are using RISC "under the hood." Although there seem to be many open projects in many areas, until recently, there has been no open source ISA for open and free implementation. ISAs add a necessary but considerable amount of cost to computing. To port software from one ISA to another ISA is expensive. Systems-on-Chips (SoCs) have many different ISAs, but ISAs do not affect system performance or energy efficiency as much as algorithms, compilers, circuit design, or fabrication processes, making RISC-V a good candidate for open use.

The benefits of RISC-V include a shorter time-to-market, fewer errors given more developers are looking at it, lower cost from reuse of the open ISA, and transparency that makes it difficult for governments or nation-states to add secret trapdoors. The fabless Arm has successfully proven that a company can come up with the IP for an instruction set or processor and that many others will fabricate it. It is much easier for designers to take an open ISA and change or add proprietary sections for reuse. An industry-standard ISA lends itself to a larger population of engineers with a collective experience, ecosystem, and community forums. Architecture research and education would be more realistic and able to leverage fully open hardware and software stacks. Open source makes products such as the Internet of Things less expensive. RISC-V can span the small to the large in computing. Historically, standards bodies have cooperated together for many other open technologies, but not an ISA. Until now.

Lynnette Reese is Editor-in-Chief, Embedded Intel Solutions and Embedded Systems Engineering, and has been working in various roles as an electrical engineer for over two decades. She is interested in open source software and hardware, the maker movement, and in increasing the number of women working in STEM so she has a greater chance of talking about something other than football at the water cooler.

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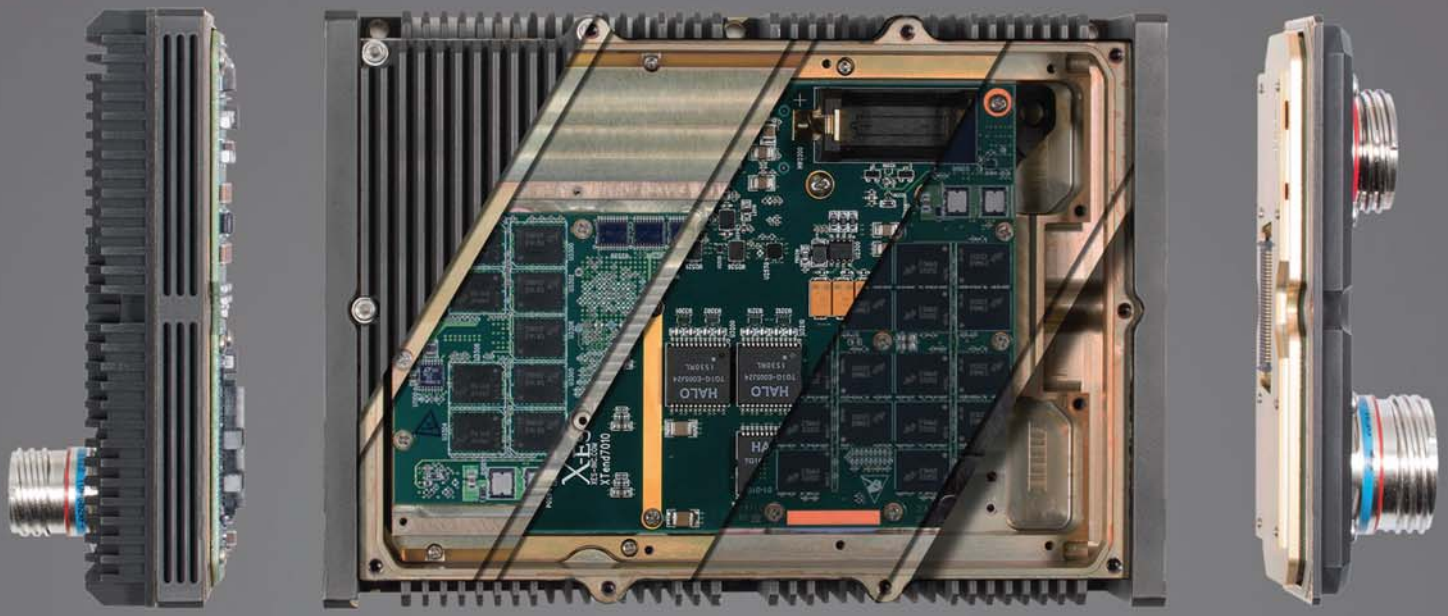

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How CoaXPress and Machine Vision Are Giving Traffic Monitoring a Fast Commute to the Future

As the world develops more efficient methods of transportation on our roads and highways, ways of managing the influx in vehicles must keep pace.

By Donal Waide, BitFlow

From the prevention of red light runners and toll evaders to daily traffic reports via the web and traffic counting evaluations for future road expansions, machine vision is fast becoming the means to safer, more coordinated, and more "intelligent" use of our roads. The late 1970s gave birth to the first Intelligent Traffic System (ITS) in the form of the license plate reader. Since then, several companies have developed machine vision technology for ITS to a point where efficiency and accuracy are at their highest levels ever.

(Courtesy BitFlow)

MACHINE VISION AND INTELLIGENT TRAFFIC SYSTEMS

Essentially, machine vision is the ability to use a camera, computer, and an illumination source to make a decision. For all its sophistication, an Automatic License Plate Recognition (ALPR) system is basically comprised of the same components as an imaging solution for checking the quality of toothbrush bristles, for example. Technological developments have changed over the years, such as lighting taking the infrared illumination path and then LED, and options such as strobing and flash have emerged. Yet the basic components remain the same: Camera, illumination, and PC.

Traffic Analysis is another application under the ITS umbrella where imaging is deployed. Instead of concentrating on license plates, it inspects traffic itself. High-speed cameras frame the roadway to detect the volume of free-flowing traffic, as well as the speed at which it is moving through the frame. In areas of high traffic or where a traffic study is needed to determine the need for extra lanes, Traffic Analysis is a helpful tool. It is also valuable as the live video feed can be given to news networks and law enforcement or streamed on the Internet, showing us what the traffic looks like in real-time at a specific location.

"Analog data in these systems is transmitted at a sluggish 11Mbps over a single coax cable from the camera to the computers. Now, consider the potential volume of data over a single coax cable with just one CXP link at 650Mbps—we're talking almost 60 times more data."

Advancements in computer chips have solved many ITS problems, with systems getting cheaper and faster every three to six months. PCs are now fast enough to allow database matching for blacklist and whitelist applications in real-time, for instance, to prevent unauthorized entry into buildings. Cameras, once analog across the traffic world, have migrated to digital with the option now for CMOS over CCD cameras. Over the last number of years, CMOS has emerged to be lower cost, with lower noise issues in visible light and requiring lower power to run. All these are indicative of CMOS cameras being the better option for the majority of ITS applications. While typically in a NEMA protective housing, cameras for traffic applications are more robust than ever before, able to handle temperatures ranging from -30°C to 75°C (-22°F to 170°F) and 10%-90% condensing humidity. Unlike in machine vision applications, cameras in traffic systems need to manage variable lighting conditions, unpredictable appearance of cars, long distances to the processing system, and changing weather conditions. Consequently, low-end machine vision cameras are not suitable for most of these systems. Instead, they need to rely on high-performance cameras to increase accuracy—regardless of traffic volume, speed, or weather conditions.

MACHINE VISION INTERFACES

Besides camera, illumination, and PC, another aspect in system design is the machine vision interface between the camera and the computer.

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Figure 1: The Aon-CXP frame grabber is part of a trend that is seeing CoaXPress cameras shrinking while also offering higher performance and improved power efficiency. (Courtesy BitFlow, Inc.)

Cameras need to transmit bandwidth-heavy data to the PC so that data is not lost and arrives without lag over long distances. When analog cameras were in use, and some of them still are, the interface was a BNC coaxial connection between the camera and a data acquisition board, known as a frame grabber. The frame grabber was usually a PCI interface, fitted into the motherboard, and allowed data to transfer seamlessly between the analog camera and computer memory.

As technology's march has continued forward, so has frame grabber design. Now enabled are digital interfaces such as LVDS, RS422, Camera Link, and most recently, CoaXPress (CXP). With the advent of these additional interfaces, camera choice has broadened, encompassing, for example, camera sensor sizes, options such as IR/monochrome or color, and frame rates. Of these interfaces, CXP appears to be the most promising for ITS.

COAXPRESS

The Japan Industrial Imaging Association formally introduced the CoaXPress V1.0 high-speed point to point serial communication standard back in 2010, followed by CXP V1.1 in 2013. Designed for transmission over single or multiple coaxial cables, the original version had a high-speed downlink of up to 6.25Gbps per cable, plus a lower speed, 20Mbps uplink for communications and control. Power is also available over the cable ("Power-over-Coax"), and cable lengths of greater than 130m may be achieved without an extender. CoaXPress V2.0 is due to be released in mid 2018 and will add two speeds: 10 Gbps (CXP-10) and 12.5 Gbps (CXP-12). Uplink speed will also be doubled to 40 Mbps for CXP-10 and CXP-12, allowing trigger rates over 500kHz without requiring a dedicated high-speed uplink cable.

CoaXPress has been one of the fastest growing interfaces in the machine vision industry over the past three to four years. Because of the low cost of coaxial cables, and its ultra-fast data transmission rates and achievable distances, CXP is certain to remain a major player in the coming years.

SLUGGISH TO SPEEDY

With signal latency a critical consideration for vehicle tracking and highway control applications, the CoaXPress standard can be useful, as it allows the transfer of uncompressed video, making zero latency possible. High frequency real-time triggering and exposure time adjustment can also be accommodated.

To get a better sense of CXP capability, let's look again at (Automatic) License Plate Readers. In Europe, the standard license plate is easy enough for a machine vision system to read. The plates are 18 x 20 inches. Letters/numbers appear four inches high in large, bold unhindered fonts. The story in the United States is different, as the plate is 12 x 6 inches. Apart from up to seven alpha-numeric characters, there is also a state name and sometimes an image superimposed on the plate. This can lead to confusion with a low-resolution image. Yet using a high-resolution camera demands an advanced interface to transmit the data back to the processing center quickly and accurately. This is where the advantages of a CoaXPress interface come into play.

For example, consider a toll plaza where a car drives through without paying. Current technology can capture the image, but making the distinction between the plate being recognized as "ABC123" or "A8CIZ3" requires the processing center to verify the car make and interaction with the registry. This, in turn, dramatically reduces efficiency of what should be a simple read if the resolution and data delivery were fast enough. In traffic analysis the requirement for CoaXPress is even more pronounced. Currently there are thousands of analog traffic cameras in place on our highways. Analog data in these systems is transmitted at a sluggish 11Mbps over coax cable from the camera to the computers.

Now, consider the potential volume of data over a single coax cable with just one CXP link at 650Mbps—we're talking almost 60 times more data. This would enable images of traffic on routes to be crystal clear, and also allow for better dissemination of information in terms of traffic backlogs, accidents and break downs, thus improving overall driver safety.

This takes us to the chief advantage of CXP in traffic applications, besides its high speed: retrofitting. CoaXPress uses the same coaxial cable network as the analog cameras, making retrofits cheaper and easier. Swapout of a board and camera is all that's needed to obtain high-quality, high-speed CXP images. In fact, these enhanced images are clear enough to easily see license plate numbers on a smartphone app. And because CXP offers Power-over-Coax, there is no need for additional cabling work. Power over CoaXPress applies a constant 24V DC voltage to the cable core, without influencing the signal integrity, to provide up to 13W per cable. In short, CoaXPress combines the simplicity of off-the-shelf 75-ohm coaxial cable with high-speed serial data technology.

In conclusion, CoaXPress can play a vital role in the many applications that make up ITS, two of which were touched upon in this article. As designers sit down with this interface at their disposal, more ideas will be formed, and CoaXPress will take its place among the important developments to enable ITS to perform more efficiently.

Donal Waide is the Director of Sales for BitFlow, Woburn, MA USA. Waide can be reached at donal.waide@bitflow.com or +1-781-932-2900. Donal began his life in machine vision in the ITS sector in the 1990's and has been with BitFlow since 2010.

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What the Future of LiDAR Looks Like

Autonomous cars by 2020 is a good bet—as long as goals across five key criteria are met.

By Dr. Mark McCord, PhD, Cepton

The LiDAR market is approaching a tipping point of mass market adoption that spans from individual to fleet vehicles, factory and farm automation, to UAVs. While there is an explosion in demand for high-performance, low-cost LiDAR to meet a broad spectrum of commercial and individual use applications, there have been no solutions that meet price, performance, weight, size, manufacturability or other market criteria.

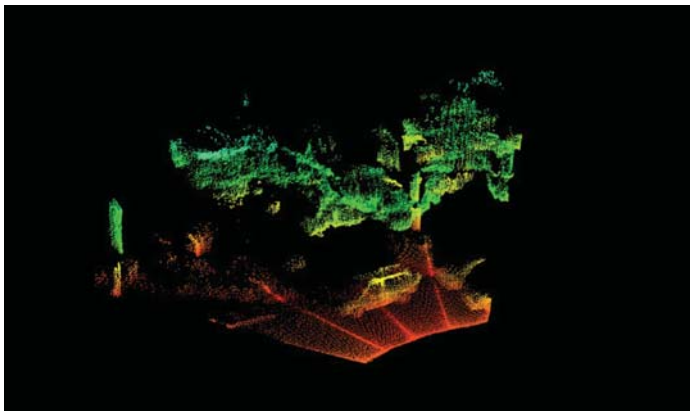

Figure 1: Point cloud capture of a car and tree by Cepton's HR80W LiDAR

AUTOMATED VEHICLES AT SCALE BY 2020?

In order for automakers to achieve ambitious goals of producing and deploying automated vehicles at scale by 2020, they need to acquire high-performance, low-cost LiDAR solutions for testing and integration today. The requirements include product performance, cost, and manufacturability across five key criteria:

- Range—200 to 300 meters
- Resolution—0.1 to 0.2 degrees of spatial resolution
- Cost—to enable broad LiDAR adoption, automakers will require LiDAR volume unit pricing to hit hundreds of dollars
- Reliability—LiDAR sensor technology must be automotive grade to match the lifespan of other critical vehicle systems

"Smaller devices are desirable because automakers want to seamlessly integrate LiDAR technology into a vehicle's existing, and subtle, headlamps and tail-lamps rather than compromise styling to accommodate legacy LiDAR technologies."

- Scalability—Companies must be able to produce reliable LiDAR units in the large quantities required for the automotive market. The design and architecture of LiDAR units must support highly automated manufacturing rather than manual heavy processes.

WHY LEGACY LIDAR IS LIMITING

The lack of LiDAR solutions that balance long-range, high-resolution performance with affordability puts 2020 autonomous vehicle production goals at risk. Many LiDAR companies see this gap and consider it an opportunity—creating a race to develop high-performance technologies that can meet market demand today.

Advances in LiDAR technology that make these requirements achievable include new micro-motion techniques. Such techniques eliminate mechanical components that are prone to wear and tear and produce a durable, low-maintenance product. Micro-motion enables the production of significantly smaller devices, without compromising range or resolution. Smaller devices are

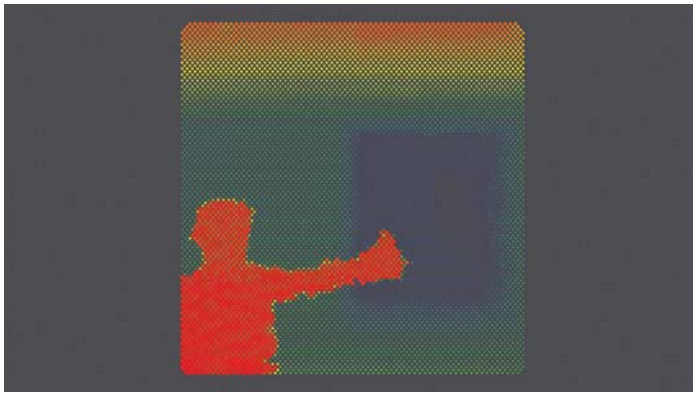

Figure 2: Thumbs-up captured by Cepton's HR80T LiDAR

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desirable because automakers want to seamlessly integrate LiDAR technology into a vehicle's existing, and subtle, headlamps and tail-lamps rather than compromise styling to accommodate legacy LiDAR technologies.

Day and night detection and classification of cars and obstacles are possible beyond 200 meters with micro-motion LiDAR units. This enhanced LiDAR sensing capability is a key milestone for autonomous vehicle applications.

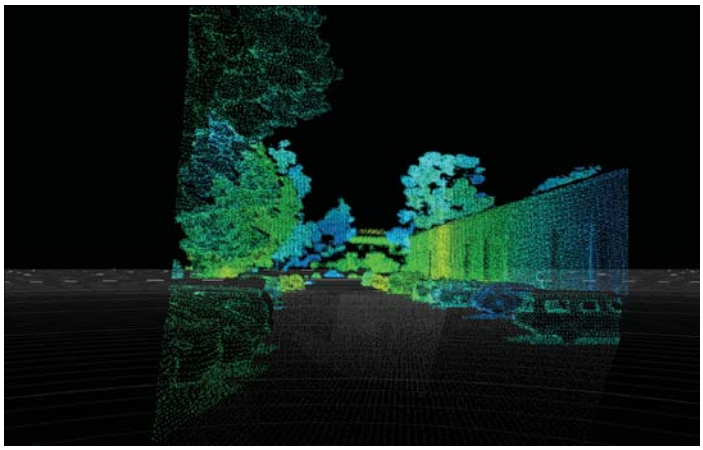

Figure 3: Parking Lot Scan by Cepton's SORA LiDAR

Micro-motion LiDAR and solid state LiDAR will coexist in the near future, each with discrete use cases depending on technology/application market fit. Close range applications in robotics and warehouses/factories may soon be served by solid state LiDAR products. However, technical limitations will continue to eliminate solid state LiDAR from automotive applications, where the criteria require long-range, high-resolution, low power, and low cost. Many key technology components used in illumination or detection of solid state LiDAR cannot be mass produced at acceptable costs, or deliver the performance at the stability or reliability meeting requirements for automotive applications.

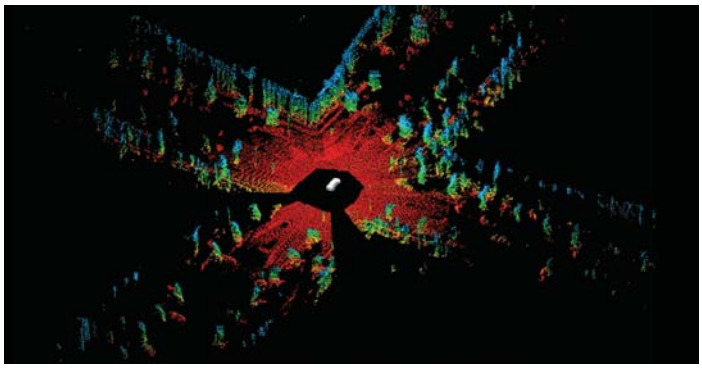

Figure 4: 360 Degree Capture by Cepton's HR80W Sensor Array

THE FUTURE

To enable faster, safer transportation, LiDAR will continue to evolve and deliver higher resolutions capable of producing camera-like images with longer range, lower cost, in smaller form factors. The fusion of LiDAR and other environmental sensors, such as camera and radar, will happen at the pixel level to provide accurate 3D multi-spectrum environmental knowledge of the surroundings. These devices will be seamlessly integrated into the next generation of vehicles without sacrificing visual design. Leading suppliers will introduce new components such as integrated units that combine LiDAR with head and tail lights. Consumers won't be able to visually tell the difference.

As Co-Founder and Vice President of Engineering at Cepton, Dr. McCord leads the development of high-performance, low-cost imaging LiDAR systems. Prior to Cepton, Dr. McCord was Director of System Engineering, Advanced Development at KLA-Tencor, where he developed electron beam technologies for etching and imaging silicon chips.

Earlier in his career, Dr. McCord served as an Associate Professor of Electrical Engineering at Stanford University, where he and his group researched various methods of nanometer-scale silicon processing, and as a Research Staff Member at IBM Research, where he worked on development of X-ray and electron beam chip lithography.

Dr. McCord earned a B.S. in Electrical Engineering from Princeton University and a PhD in Electrical Engineering from Stanford University.

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Patch Work: Q&A with E Ink

Low power consumption, small form factor, and lightweight features are leading wearables beyond the smartwatch/smartband stage.

By Anne Fisher, Managing Editor

Paul Apen, E Ink

Editor's Note: Paul Apen, Chief Strategy Officer at E Ink, which introduced with customer and partner LTS a "Smart Patch" initial prototype at the CPhI show in Messe Frankfurt in 2017 (Figure 1), spoke with EECatalog about the attributes wearable medical devices need to succeed.

EECatalog: How is the ePaper technology that is part of E Ink's portfolio relevant to medical device applications and in particular to wearable devices used for medical purposes?

Paul Apen, E Ink: E Ink displays are a perfect match for medical applications for several reasons. First, the displays are bi-stable, meaning they only consume power when an image is changed. That gives quite a bit of benefit to the end user with regard to battery life. The display can also be autonomously powered by energy harvesting methods or even through the use of small solar panels or small solar cells.

Second, the reflective ePaper displays are ruggedized, making them ideal for the kinds of use cases where it is becoming more demanding to put information displays into IoT types of applications.

Third, the technology is low power, can be flexible and is thin and lightweight. You can integrate electronics in that small display to make wearable applications possible.

EECatalog: How are wearable applications being deployed in the medical sector?

Apen, E Ink: Wearable applications have typically been thought of as smartwatches or smartbands that are worn around the wrist. However, these applications also include medical packaging and transdermal therapeutic patches.

If wearable technology is thin and lightweight, it can go directly on the patch the patient wears and offer

Figure 1: Product image for illustration purposes only. (Courtesy E Ink)

information, for example, about the use of the medication and the length of time the patch has been worn—things that are key to monitoring, understanding, and advancing the use of the medication. Also, the patch can be easily seen and connected to other smart devices.

EECatalog: How is the experience that E Ink has acquired to date playing a role as the company brings solutions to the medical sector?

Apen, E Ink: Our past experience is valuable to our partners for prototyping concepts and supporting further development of product concepts. We have a long track record of being able to show that ePaper displays can be brought to market in mass production.

We also have a deep understanding of how to design and drive the display. In the case of the Smart Patch prototype—it's a segmented display that includes preset images and icons. We are very familiar

with how you can design a display to show particular information to the end user, or to the patient in this case.

Know-how of integrating the display drivers and the microcontrollers is also valuable. In the case of the Smart Patch prototype, it has a pressure sensor on the devices, which is used to indicate when the patch has been activated. The user gets a sense of when he or she has applied pressure as well as an indication of when enough pressure has been applied. That know-how and experience can help in the product development cycle with our customers.

EECatalog: What developments in the sensors industry are you watching?

Apen, E Ink: More and more sensors are being used to monitor patients' health, such as monitoring temperature levels and heart rates or heart rhythms, glucose levels, and UV exposure.

The kinds of sensors I've just named are being incorporated into smaller and smaller form factors and wearable configurations that can be put on the body or deployed in a hospital environment. There's interest in being able to show information at the same time with these sensors. We're excited about the potential for real-time updates with a low power display and how it can dovetail with the work we are currently doing with the Smart Patch prototype.

EECatalog: How is E Ink addressing the issue of cost sensitivity in the medical device market?

Apen, E Ink: I don't see any road blocks to addressing the market on the value or cost side. We will be working closely with our customers on that. The Smart Patch is not out on the market yet, and we have not completed all the testing activities. As the solution's different pieces come together, it will be possible to evaluate the TCO and the benefits flowing from medical and patient adherence to medication regimes.

As a study by the New England Healthcare Institute (NEHI) revealed, poor medication adherence is a multi-hundred billion dollar problem in the U.S. and any kinds of technical solutions that can help that alone—whether our display or other smart types of wearables—I think can show sufficient value for what might be needed in terms of some additional costs.

EECatalog: Anything to add before we wrap up?

Apen, E Ink: I want to emphasize that E Ink's approach to wearables extends beyond just the smartband/ smartwatch markets. Flexible electronics and displays that are low power and lightweight will increase the opportunity for E Ink and ePaper technology to be integrated into medical devices and even into fabrics and apparel. Our technology can help solve some of the challenges that exist out there and we're excited to see what's next.

Go-to-Market Accelerator

Why industrial device manufacturers eager to integrate the coming NXP iMX8 processor need not linger at the starting gate

By Christian Eder, congatec AG

The NXP i.MX8 processor, based on Arm Cortex A53/A72, is expected to be available in series in early 2019 (Figure 1). With Computer-on-Modules, however, industrial device manufacturers can deploy first-to-market strategies. Developers of low-power x86 systems will also be evaluating this new processor closely, as x86 roadmaps are increasingly designed to address all personal computing performance needs with a single pin-compatible processor layout, ultimately resulting in larger dimensions than the (ultra-) low-power small form factor range requires. But that's not the only reason why the new Arm Cortex A53/A72 processor is a very interesting option. The stable roadmap that Arm processors in this class now offer is another good reason, as the core feature set is already standard in consumer smartphones and tablets. Last but not least, the processor's performance and feature set improvements are also convincing, based on NXP's pre-production specifications.

HARDWARE VIRTUALIZATION AND DOMAIN PROTECTION

The NXP i.MX8 processor enables fast deployment of multiple operating systems through advanced hardware virtualization and domain protection, essential for many IoT and Industry 4.0 devices. Such devices can thus separate the IoT gateway from the actual application. Also appealing is the suitably high graphics performance of the i.MX8 processor, which can deploy up to four streams of independent graphics content on four HD screens. This enables, for example, attractive digital menu boards for system catering or individual infotainment in four-seat-across rows on planes, buses, or trains with just one system.

A failover-capable display controller with SafeAssure function can ensure that all displays are always available for their dedicated applications. This means a restart in a virtual machine cannot cause the display of another application to switch off. For instance, the display of a credit card reader GUI remains active, while the digital signage player is restarted remotely. This is an important feature in vending machines, as well as in commercial and public transport vehicles for driver assistance, fleet management, and infotainment. The displays can even support 4K resolution to offer individual applications a particularly high image quality.

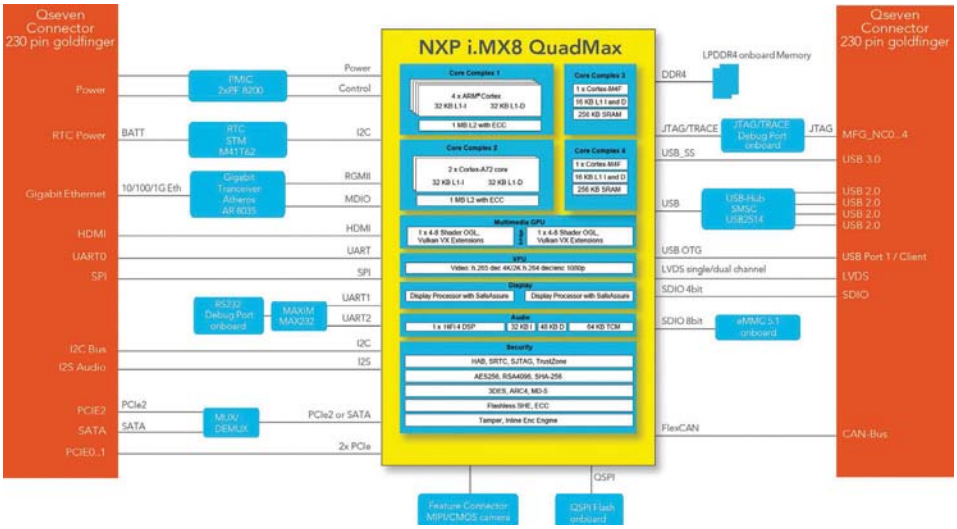


Figure 1: The NXP i.MX8 processor, which congatec will support on Qseven and SMARC Computer-on-Modules, offers an extremely attractive feature set for low-power small form factor designs.

INCREASING INTERACTIVITY

In addition, the feature set includes hardware-accelerated image and voice recognition with a powerful vision pipeline and audio processing subsystem for

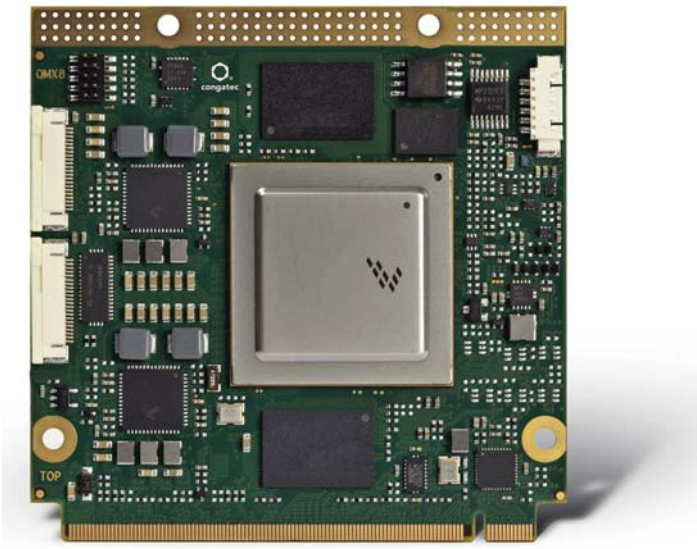


Figure 2: Computer-on-Modules can greatly accelerate the go-to-market strategy of OEMs who are not admitted to early access programs.

high interactivity—such as augmented reality, gesture control, user authentication, or even collaborative robotics. The scalable feature set comes in pin- and power-compatible single-, dual-, and quad-core packages as well as software-friendly, copy-exact IP blocks, so the processors can be adapted granularly in line with the functional and TDP needs of the respective applications and the environment.

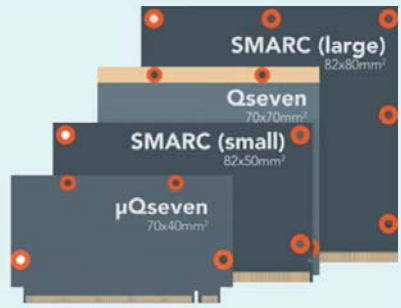
Such adaptability is why such a wide range of operating systems is supported, from Android and Linux to FreeRTOS, QNX, Green Hills, and the DornerWorks Xen hypervisor. To match the requirements of the automotive sector according to AEC-Q100 grade 3 (-40 to +125 °C Tj) and industry (-40 to +105 °C Tj), NXP offers a long-term availability of 10 and 15 years. All this makes the new i.MX8 a very attractive platform for many developers of embedded, IoT, and Industry 4.0 devices that must deliver 24/7 operation in harsh environments.

HOW COMPUTER-ON-MODULES CAN CLOSE THE GAP

Yet while developers are understandably eager to get the new processor into their applications as quickly as possible, if they are not among the large-volume OEM customers who receive first development samples before series production, they have little chance of initiating i.MX8-based designs today. Those not among the select few also lack the necessary detailed knowledge of the dedicated features as well as the firmware and middleware such as board support packages (BSPs), drivers, and APIs. That lack prevents them from developing a system and application design that would be ready to hit the market as soon as the processor becomes available in series. It will typically take another nine to 12 months for OEMs without access to NXP's Early Access Program to bring their own designs to market.

This time-to-market gap can now be closed with customized system designs based on standardized Computer-on-Modules (Figure 2). They provide a standardized feature set that is processor-independent and therefore reusable across multiple processor families. Computer-on-Modules come complete with bootloader and BSPs covering all relevant interfaces of the module specification. In addition, their very comprehensive documentation even includes instructions on how to lay out the individual carrier boards for the Computer-on-Modules. Developers can design the system as if the processor were already there although it is not yet available. For

COMPUTER-ON-MODULE STANDARDS FOR I.MX8



The NXP i.MX8 is available in two form factor standards for Computer-on-Modules: Qseven and SMARC. Both standards are maintained by the SGET, and both allow slim designs thanks to their direct edge connectors. But what's the difference? Qseven offers 230 pins and SMARC 314 pins. SMARC primarily targets high-performance multimedia applications, while Qseven offers a wider range of processors required in deeply embedded and industrial applications. The difference in the number of interfaces between Qseven and SMARC 2.0 is also a price indicator for credit card sized designs: Qseven suits less complex designs, while SMARC is designed for high end applications. Deeper insight into the form factors is provided in a congatec whitepaper available at https://tinyurl.com/y86vus4s.

Figure 3: System design example for faster upgrades: Datik's DCB fleet edge computer is equipped with i.MX6-based Qseven Computer-on-Modules from congatec, which can easily be swapped for the even more powerful new i.MX8 performance class modules.

Figure 4: Evaluation boards for Computer-on-Modules provide an essential basis for OEMs' own carrier board designs.

functional tests, it is possible to use processors from preceding generations. To this end, the ecosystem of small form factor and ultra-low-power Computer-on-Module standards such as Qseven or SMARC provides evaluation carrier boards, for which the layouts can also be obtained in order to use them as templates for the developer's own solutions. Best practice designs can be used via copy and paste.

WHY BOTH TIME AND NRE SAVINGS ARE REALIZED

There are also providers who specialize in carrier board designs with Computer-on-Modules, allowing developers to work on new solutions without hardware effort well before the availability of a new processor. By using Computer-on-Modules, developers can save a minimum of 50 percent and up to 90 percent in development time and NRE costs over a full-custom design. And if this minimized development effort occurs before the new processors reach series production, achieving first-to-market in a given industry is almost guaranteed.

One advantage of this module approach is that there is no need to deal with the inevitable teething problems of new processors in the Early Access Program; the Computer-on-Module manufacturer will have already done this. Such a Computer-on-Module approach is therefore particularly suitable for industrial batch sizes. It is no coincidence that most industrial x86 designs are equipped with Computer-on-Modules, as independent studies by IHS Markit show[1]. So why not also use them for the powerful Arm Cortex performance classes—such as A9 or A53/A72?

FLEET MANAGEMENT USE CASE

To see how easy it could be to switch from i.MX6 to i.MX8, let's look at the example of the Datik DCB edge computer for fleet management (Figure 3). Based on congatec's Qseven Computer-on-Modules with i.MX6 processor, it is already in use in Southern Europe, France, Spain, and Latin America. With its comprehensive range of features it can control all locally required functions of buses. This includes intensive data exchange with control centers as well as the transmission of surveillance video data with up to 3.9 Gbps via LTE. This system can now be upgraded to a new level of performance simply by swapping the modules. As a rule, it will be ready to use immediately as long as the interface requirements of the carrier board are fully supported by the BSPs of the modules, which is the case with most standard equipment. Accompanying migration support also helps OEMs master design-in challenges as quickly and easily as possible.

Manufacturers such as congatec are offering Computer-on-Modules for the new i.MX8 in the SMARC and Qseven form factor standards (Figure 4). These modules can be scaled across Arm and x86 processors in the low-power small form factor class, which means that the choice of form factor won't limit the choice of processor technology. Developers of currently change-sensitive x86 designs can capitalize on this freedom of choice to gain experience in previously unknown Arm areas.

EARLY ACCESS PROGRAM FOR SMALL AND LARGE OEMS

To allow developers to concentrate fully on the functional evaluation, congatec also offers numerous other services around its modules, ranging from starter kits to customer-specific Embedded Design and Manufacturing Services for carrier boards. Thanks to congatec's personal design-in support, OEMs also benefit from the premium service of experts with know-how spanning from requirement engineering to mass production. congatec will present the first modules and matching starter kits at Embedded World 2018 Nuremberg.

Christian Eder is Director of Marketing for EMEA and is one of the founders of congatec. He has 28 years in embedded computing and was draft editor of the PICMG COM Express and SGET SMARC 2.0 specification.

1. https://technology.ihs.com/587541/embedded-computer-board-technologies-continue-to-grow-but-atca-revenues-significantly-decline

Adding Intelligence to Fixed Function ICs: Q&A with TI

A low-cost entry point approach to simple sensing applications

By Anne Fisher, Managing Editor

Dave Smith, Texas Instruments

Editor's Note: The announcement that Texas Instruments (TI) now offers its ultra-low-power MSP430™ microcontrollers (MCUs) at around 25 cents in high volume made for a good occasion to speak with Dave Smith. Smith is the Product Marketing Manager for TI's MSP430 FRAM-based microcontrollers and argued that there are Big Reasons for Small MCUs in an earlier article. Now, Smith explains that reasons for designer interest in the MSP430 line go beyond just the low-price entry point. Edited excerpts from our conversation follow:

EECatalog: What comprises the MSP430 Value Line Sensing MCU family?

Dave Smith, TI: This is a collection of application reports complete with code libraries aimed at adding a little bit of intelligence to fixed function ICs—that is, some of the common things found on a PCB: comparators; real-time clocks; EEPROMs; supply voltage supervisors; reset controllers—some of the simple functions that many PCBs have.

EECatalog: What goes into the decision to use a microcontroller rather than an off-the-shelf product?

Smith, TI: When thinking about the decision to use a microcontroller as compared to an off-the-shelf product you're often looking at a situation where there is not an exact fit for one of the off-the-shelf products. In those cases, using a microcontroller can enable an engineer to tailor the functionality, whether a simple timing parameter or a particular sequence of wake up events, for example, to their application needs. However, we are not trying to go head-to-head with an off-the-shelf whatever-type IC, but rather adding to that.

Figure 1: Smith notes the applicability of microcontrollers that allow the customization of system-level functions to markets such as Smart Home. (Courtesy TI)

EECatalog: Could you offer an example?

Smith, TI: Yes. Things like a real-time clock or a system wake up controller is where we are targeting some of these applications or these functional blocks. So, while I can buy an off-the-shelf real-time clock, what I can't buy is something that really fits in with the system needs that I have. In this case we are using the FRAM nonvolatile memory along with the real-time clock and allowing them to use that as a combination of real-time clock and EEPROM.

Another example is a programmable system wake up controller. Yes, I can buy an external chip that is going to trigger a wake up every 100 milliseconds, two hundred milliseconds, whatever is hard-wired into that part. With the MSP430 based solution we can adjust the sleep interval and wake up schedule by simply sending a command over the UART, this added flexibility can help to extend system battery life.

Or say I have an RF chip, Bluetooth, Wi-Fi or whatever, but I want it in a battery-powered system, some home security product or network product. I may not want that to be active all the time because

I want the battery to last more than six months, 12 months. With this type of device, I can program it so that it only wakes up that RF chip when something relevant happens—that could be monitoring an ADC for example.

In the low-power MSP430 we can monitor an ADC or use the window comparator to significantly drive down the power consumption of that overall system. Many of those functions could be incorporated into the main logic processor, but it is often very inefficient to do that. So, it may be a part that may have low-power modes and may be able to go into some of the shut-down modes but may be limited or use even more power when it is in those modes, than the MSP would.

EECatalog: So designers can hew a bit closer to their application's demands than they might be able to with an off-the-shelf IC?

Smith, TI: Yes, we see a lot of customers that are trying to develop energy harvesting or maybe scavenging applications where the ability to do very low power stores, or nonvolatile stores, or operate for longer with a very limited power supply. Whether that's a rechargeable battery that is charged by solar panels or just a conventional battery, lasting longer between service intervals will help to reduce maintenance costs and overall system ownership costs.

A couple of other examples: On the PWM one of the example code snippets creates a dual 8-bit DAC, so in a standalone situation this could be a simple sounder. Maybe it gets a push button or some other trigger from an ADC or a comparator and then it plays a tone or a series of tones to indicate that something has happened. Everything from a simple doorbell to a simple timer.

Or it could be incorporated into a larger system, where you are going to send some communication data, some serial data, to trigger that signal. So that's a little dual DAC. It could be as simple as controlling color blending on an RGB LED.

One of the areas that we have really seen this being taken up by our customers is where they are looking to do very low power nonvolatile writes. With an energy-harvesting solution or with a small coin cell battery, if you need to write data in a conventional flash or EEPROM memory the mA's of current required will quickly deplete the available stored energy. Conventional EEPROM and Flash technologies include a charge pump within the device that is required to boost the supply voltage to a higher voltage. It takes timing to do that and, more critically, it takes a significant amount of energy to do that.

If you want to store something in a system whether sensor data or whatever data it is—and want to store it frequently—that can quickly deplete the battery. The FRAM technology we're using with the MSP430 Value Line is very, very low power. We don't have the charge pump involved, which also makes it faster.

It's also very high erase/write endurance, with 1015 cycles as compared to the typical 100K or 1M cycles of EEPROM or Flash.

EECatalog: What are you seeing in the ecosystem of folks coming up with interesting sensors?

Smith, TI: We see a lot of activity in and around the connected home. Yes, there is a lot of activity going on in office and factory automation as well, but the home automation that is going on at the moment and is driven by cloud services and the big names rolling out the personal assistants stands out.

The automation being built into homes is going into places that I don't think even a couple of years ago we would have expected to see that level of intelligence, whether through some of the simple applications we have been talking about here, or things that use capacitive touch to program thermostats or to operate a voice assistant just to trigger something. I think where we are going to see explosive growth is in the home automation, small appliance, and personal assistant areas, and these parts can definitely play roles in that because many of these are battery-powered. Longer battery life makes battery changes less frequent and helps the environment.

EECatalog: Are there some additional things our readers should know before we wrap up?

Smith, TI: These half-a-kilobyte to 1-kilobyte in FRAM devices also have half a kilobyte in SRAM, and this is one of the characteristics which sets them apart from competitive devices. Usually if you have a small program memory, you will have a very small data memory. With the competitions' 512-byte program memory, you might get 64 or 128 bytes of data memory.

In our parts, if you get 512 bytes of program memory, you actually get 512 bytes of data memory as well, so that makes it a little more programmer friendly; it allows you to do more with the device.

Out of Home Media in the Data Revolution

How digitization and data are transforming the media landscape

By Mark Boidman, Susan Wang, and Brandon Yoshimura, PJ SOLOMON

Mark Boidman

Susan Wang

Brandon Yoshimura

The Out of Home media and advertising ("OOH") industry is undergoing a digital and data-driven transformation. OOH reaches consumers who are "on the go" or in transit and encompasses a variety of formats including billboards, posters, transit advertising (bus wraps, taxi tops, airport displays), street furniture, kiosks, and retail signage. With advancing technologies, OOH advertising formats are becoming easier to deploy, update and measure.

Digital displays are beginning to replace traditionally static installations. We work with a number of providers who are enabling this transition through the creation of stunning digital displays and compelling programmatic and backend offerings. Companies in the sector, including BrightSign/, have developed cost-efficient media players which enable reliable, non-PC based digital signage solutions to be implemented nearly everywhere—from small retail displays to massive outdoor installations. A proprietary OS built specifically for digital signage has real advantages when considering security and ease-of-use.

SMALL DISPLAY TO 4K INTERACTIVE

Intel® technologies drive approximately 75 percent of PC-based solutions for digital signage. Intel's Open Pluggable Specification ("OPS"), developed in partnership with NEC and Microsoft and launched in 2010, standardizes system architecture between displays and media players, allowing for more cost-effective design and seamless deployment and management of digital display solutions. Recent products such as the BrightSign HO523 OPS media player (Figure 2) are adding value to this deployment model by bringing the end-user's TCO even lower. The new Intel Smart Display Module ("SDM") released in 2017 was developed as an answer to the ever-thinner and power-efficient digital displays coming to market. Delivering the same level of interoperability and intelligence as the OPS, the SDM is Intel's smallest product yet (at 60mm x 100mm and a maximum thickness of 20mm). The

"Actionable data and Internet of Things ("IoT") technologies are enabling a second wave of OOH innovation centered on making displays more intelligent, efficient and impactful. "

Figure 1: Speed cameras formed an integral part of an OOH display promoting Reebok ZPump footwear. (Robin Nilssen, Courtesy of Reebok)

SDM also has an expanded range of supported processors, from the energy-efficient Intel® Atom™ processor, which is optimal for powering tablets and other small display devices, to the high-performance 7th generation Intel® Core™ processors, which are capable of driving 4K interactive displays and motion recognition while delivering real-time content and audience analytics. One point of consideration is that the OPS is an open specification and the overall adoption rate is low. And given new SDM is a proprietary module, and not a specification that the industry can adopt, there are even more obstacles to any mass industry adoption.

AHEAD FOR DIGITAL OOH: MORE COMPETITIVE PRICING, DATA MANAGEMENT, RISK CONTROL

Digital billboards offer the ability to display dynamic content with little associated production cost. Messages can incorporate countdowns (buy now!), user-generated content (pulled from social media feeds) or be contextually customized to account for time of day or weather. Further, these installations can display video, stream live events (see the celebrated "Rise of the Tomb Raider" OOH campaign) or rotate through a carousel of brand-specific content.

Figure 2: Capitalizing on standardized system architecture are solutions such as the BrightSign HO523 Open Pluggable Specification (OPS) media player.

On top of these content improvements, advances in OOH purchasing technologies allow brands to leverage OOH infrastructure in ways never before possible. Leading OOH media owners have developed homegrown, cloud-based dashboards that allow agencies or brands to view available inventories in real-time with additional data on asset demographics and reach provided by Geopath, a not-for-profit audience location measurement organization. In addition, certain vendors have begun consolidating digital inventories to allow for true, programmatic offerings. In spite of these advances, hurdles remain (including fragmentation of networks, standardization of measurement, standardization of technologies and pricing), but the OOH industry is rapidly beginning to resemble web-based alternatives in terms of breadth of media formats available, ease of deployment, and standardization.

Unlike other digital formats, however, OOH media and advertising cannot be blocked or skipped. As digitization accelerates and consumers continue to be increasingly mobile, we anticipate rapid growth in OOH media coupled with improved margins resulting from realized efficiencies in the time and information-intensive buying / selling processes. These improved processes will allow for more competitive pricing, data management, and risk control for the industry as a whole.

FULL STEAM AHEAD: DIGITAL GROWTH AND INVESTMENT ACCELERATING

The digital billboard opportunity is substantial. Today, in the United States alone, there are approximately 334,000 static billboards and only 7,300 digital billboards (~2.2 percent) according to the Outdoor Advertising Association of America ("OAAA").

The largest OOH operators are driving the transition to digital. Recently, Lamar Advertising committed to adding 150 digital installations per year for 2018 and 2019 through organic growth and acquisitions, adding to an existing base of 2,700 screens. OUTFRONT Media acquired Dynamic Outdoor, which owns a portfolio of 52 digital billboards across Canada in June 2017 for $94 million, adding to its base of roughly 1,000 digital installations. OUTFRONT Media management estimates that digital inventory will comprise over 20 percent of revenue in three years. JCDecaux currently owns more than 1,400 digital billboards globally and is actively pursuing ongoing digitization of its street furniture assets in major cities, including its London Digital Network of over 675 bus shelters, its New York Digital Network of 300 digital bus shelters and newsstands and its recently announced installation of 150 digital City Information Panels and bus shelters in Chicago. Clear Channel Outdoor installed 450 new digital displays last year internationally, bringing its base to 1,180 digital billboards in North America and 13,300 globally. CIVIQ, the hardware provider for New York City's LinkNYC digital smart city information kiosks, currently has 1,600 kiosks throughout the city's five boroughs, and will deploy 7,500 kiosks over the next eight years. We also see the beginnings of vertical consolidation in this space. In 2014, OUTFRONT Media acquired advertising technology company Videri, a cloud-based app-linked ecosystem that powers smart digital displays.

The OOH industry as a whole is projected to grow at 5% annually, a figure dwarfed by projected digital OOH growth of 13% annually from 2015 to 2019. Digital penetration of OOH is expected to reach 30% by 2019. This digitization will be crucial to mitigating legacy OOH format restrictions.

DATA DRIVING THE FUTURE OF OOH

Leveraging connected technologies across these new digital portfolios will create a differentiated value proposition for sector participants. Actionable data and Internet of Things ("IoT") technologies are enabling a second wave of OOH innovation centered on making displays more intelligent, efficient and impactful.

The rise of Telecom Data as a Service ("TDaaS") has provided OOH operators with access to critical customer insights. Telecom giants including AT&T, Verizon, Sprint and Telefonica have begun to collect, analyze, package and sell aggregate customer data to OOH operators and advertisers. Some carriers, including AT&T, have established their own in-house units to monetize data, while others have partnered with technology firms like SAP, IBM, HP, and AirSage, which take over management of the backend and marketing of the packaged data products.

TDaaS data includes demographic and location details in addition to browsing, messaging and call information gleaned from subscribers' files. AT&T's home-grown division, AT&T Data Patterns, collects customer data such as age, sex, ethnicity and income to provide anonymized and aggregated group insights to clients—chief among them Clear Channel Outdoor. AT&T Data Patterns can also measure lift in actions that are supported by AT&T services. As an example, the program is able to measure the percentage of an audience that passed an OOH advertisement and later watched TV programming that was promoted on the ad on their DirecTV networks. Or, when a retail store uses AT&T Wi-Fi, AT&T Data Patterns can measure the percentage of an OOH audience that converts into store visits. In all cases, the lift percentage is given to clients as a statistic, providing them valuable insight into campaign effectiveness. SAP, which offers a service called Consumer Insight 365, receives regularly updated data from carriers, covering daily mobile activities (which can reach 300 unique events per day) of 20 to 25 million subscribers. The data is anonymized and sold to advertisers, who can use the information to target specific audiences and measure ad effectiveness. In one application of TDaaS and digital OOH installations, beverage-maker Anheuser-Busch InBev employed geo-fencing technology to deliver mobile advertisements to consumers passing by one of its digital OOH advertisements in Atlanta. While TDaaS offers

actionable insights for OOH operators, it is somewhat constrained as it is controlled by third-party providers and existing telecom IT infrastructure is not optimized to handle the aggregation and distribution of massive data sets in real-time.

IOT INTEGRATIONS CREATE UNIQUE OPPORTUNITIES

To achieve more granular insights on audience demographics and engagement, OOH operators can now leverage IoT devices on their digital installments, including cameras. In a recent campaign in Sweden for ZPump shoes, Reebok installed street-level OOH displays with speed cameras that measured the pace of passing pedestrians (Figure Y). Runners able to achieve a pace in excess of 10.5 miles per hour were awarded free shoes. Similarly, last year, eyewear retailer Kirk&Kirk deployed a campaign that offered pedestrians custom-color glasses based on the colors of their outfits.

Cameras with facial recognition technology can also be integrated into displays to track engaged viewers, attention time, age and gender (all on an anonymized, aggregate basis), in addition to analyzing real-time audience data to drive ads based on viewer groups. In the advertising context, facial recognition technology works to capture and identify select facial features of an individual (such as facial shape, distance between facial features, existence of wrinkles, etc.) and compare them against a database of features and combinations of features to identify that individual's age, sex and other demographic attributes. This biometric technology, combined with counting and tracking capabilities built in to digital displays, is able to yield data like 'number of women in a viewer group', or 'average time spent looking at the display by a senior man.' This data not only holds rich insights into advertising effectiveness, it also represents enormous opportunity for advertisers to increase ROI by communicating in highly engaging, targeted way with specific audiences.

MASS MESSAGING TO SMART MESSAGING

Facial recognition platforms, including Paris-based Quividi, measure mood, audience reactions and engagement. Quividi can be integrated into digital displays to scan viewers' faces and run algorithms trained on computer vision and machine learning to identify facial and voice expressions, such as furrowed eyebrows or a loud laugh, against a database of pre-programmed expressions, in real time. They then equate these expressions to certain emotions or social cues and provide data on an aggregate basis to give advertisers insight into how effective and appropriate their current ads are. In 2016, Apple acquired Intel Capital-backed Emotient, a startup specializing in emotion detection and sentiment analysis based on facial expressions. The company offers a cloud-based service that can deliver direct measurement of a customer's unfiltered emotional response to advertisements, content, products, and customer service or sales interactions. This emotional response data, combined with location and demographic data, is a powerful tool for OOH operators and advertisers to gain insight into and target consumers in unprecedented ways.

Telecom and IoT data combine to provide OOH operators with visibility into audiences at the most opportune time, when they are mobile and close to or at the point of sale. As digital formats proliferate and data is used and leveraged, the OOH industry will continue its transition from a mass messaging medium to a smart mass messaging medium with hyper-targeting capabilities and unparalleled scale and impact.

Mark Boidman is a Managing Director and Head of Media Services at PJ SOLOMON, an investment bank in New York City. Brandon Yoshimura serves as an Associate on the Media Services team. Mark and Brandon advise companies across the media and technology landscape, including digital media and media services with a focus on out of home media, retail (in-store) technology, and mobile technologies and solutions. They have advised clients on sector-shaping merger and acquisition transactions, with a combined transaction value of over $40 billion.

Susan Wang is a Senior Analyst with PJ SOLOMON.

ADL Embedded Solutions

NEW! Compact, Modular and Fanless Industrial PC

APPLICATIONS

- Industrial IoT (IIoT) Network and Cloud Computing
- Cyber Security Edge Devices for ICS and SCADA threat security
- Secure Networking (Secure Routing, Traffic Monitoring and Gateways)
- Intelligent Machinery and Equipment Controllers

The ADLEPC-1520 is a rugged, compact industrial-grade chassis constructed from 6063 aluminum, with thick-walled design and a fanless, conduction-cooled CPU for wider temperature operation. It features a durable anodized finish, flush-mounted screws, and flexible mounting options. At only 2.3" x 3.4" x 3.7", it is ideal for a variety of industrial applications and environments...whether on the factory floor or in the external environments.

FEATURES & BENEFITS

- Compact footprint: 2.3" x 3.4" x 3.7"
- Intel® E3800 -Series Atom processors
- Stackable Extension Connector
- Modular I/O Expansion
- Fanless Design
- Custom I/O and Power available to support specific application requirements
- Operating Temperature: -20C to +60C (optional extended temperature available

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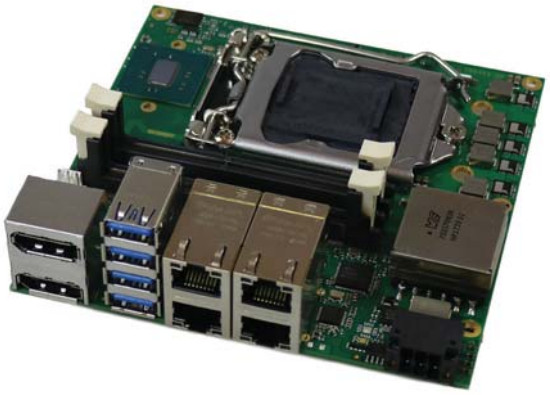
NEW! Intel® Core™ / Celeron® 6th Generation Stackable SBC



APPLICATIONS

- Secure Networking, Secure Routing, Traffic Monitoring and Gateways
- Cyber Security Edge Devices for ICS and SCADA threat security
- Unmanned and Drone Payload Computing
- Industrial IoT Gateways and Controllers

The ADL120S is a high-performance, compact 120mm x 120mm SBC based on 6th Generation Intel Core and Celeron processors. It is full-featured with robust I/O including USB 3.0, LAN, M.2 PCIe/SATA and a wide operating temperature range (-40C to 85C) and high-resolution DisplayPort outputs. Eight PCIe X1 expansion lanes allow for customization for any application-specific environment.

FEATURES & BENEFITS

- Compact 120mm x 120mm Footprint
- 6th Generation Intel® Core™ and Celeron Processors (Formerly Codenamed Skylake)
- Intel® Q170 Chipset
- Long-term available Intel Embedded Processors
- Up to 32GB DDR4 , 4x USB 3.0
- 8x Stackable Expansion PCIe lanes with up to 4x SATA and/or 4x USB3.0
- Wide operating temperature range (-40C to 85C)
- 2x DisplayPort Outputs

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Connect Tech Inc.

COM Express® Type 7 Carrier Board

Connect Tech's COM Express® Type 7 Carrier Board is based on the PICMG COM Express® COM.0 R3.0 specification. It includes dual 10-Gigabit Ethernet from SFP+ modules, 2x GbE ports, M.2 NVMe Storage, 4x USB 3.0, full and half size Mini PCIe expansion slots, 8x 3.3V buffered GPIO, and a Console connection via Micro USB. The carrier board is ideal for high-compute, enterprise level applications that have a need for a small form factor rugged solution providing access to high-end Xeon D class processors. This board has an extremely small form factor of 125 x 95mm and an extended temperature range of -40°C to +85°C (-40°F to +185°F).

TECHNICAL SPECS

- Ethernet: Dual 10-Gigabit Ethernet; 2x Gigabit Ethernet (10/100/1000)
- Storage: 1 x M.2 2280 M-Key Slot (Dual function PCIe + SATA), NVMe (PCIe x4 Gen 3) capable
- Expansion: 1x mini PCIe slot full size (USB + PCIe), 1x mini PCIe slot half size (USB + PCIe)
- Power: +12V Input
- Miscellaneous: 4x USB 3.0, 8x 3.3V buffered GPIO, 1x CPU Console UART, 1x General Purpose UART

CONTACT INFORMATION

Connect Tech Inc.
Embedded Computing Experts

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Toll Free:1(800)426-8979
Fax: 1(519)836-4878
sales@connecttech.com
www.connecttech.com

Connect Tech Inc.

Xtreme/10G Managed Ethernet Switch/ Router

Connect Tech's Xtreme/10G Managed Ethernet Switch/ Router provides high density, high port count Layer 2 switching and Layer 3 routing with 10G uplinks. A total of 36 switchable ports, with 4 x 10GbE, 8 x 1GbE (SGMII), and 24 x 1GbE (Copper 10/100/1000Mbps) ports in an extremely small form factor 85mm x 85mm. The device targets managed Layer 2 and Layer 3 equipment in SMB, SME, and industrial applications where high port count 1GbE switching with 10GbE aggregation/uplinks are required.

TECHNICAL SPECS

- 36 switchable ports (4x 10GbE; 8x 1GbE [SGMII]; 24x 1GbE)
- High-density board-to-board connector
- 85mm x 85mm module
- +4V to 14V input range
- -40°C to +85°C (-40°F to +185°F)

CONTACT INFORMATION

Connect Tech Inc.
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Compact, Rugged Mission Systems Built to Perform

Compatible Operating Systems: Linux and Windows
Supported Architectures: PCI/104 and COM Express

The ComSys-5301 combines leading edge processing with Type 6 COM Express based modularity and high capacity solid state storage in a sturdy chassis featuring robust cable-less internal connectivity and a thermally efficient and light weight design. The system is SWaP optimized for fanless and ultra-reliable operational performance in harsh environments encountered in mobile ground, shipboard and air defense equipment, homeland security and emergency service installations and drilling and mining operations. I/O expansion enables fast system redefinition. MiniPCIe sites support the modular design for easy I/O re-configuration and quick and cost effective operational upgrades when the mission evolves in ways that demand changes to the system I/O, CPU and storage. The all-aluminum extruded chassis is an extensible design which can accommodate 1,2 or 3-board stacks. This opens the possibility that a common base chassis design can address multiple applications you may have in mind. Elma will work with your design team to model the thermal characterization for your specific I/O set. The chassis is available in a wide range of color options for your application.

FEATURES

- High capacity solid state storage
- Dual 10/100/1000Mbps GbE Ports
- Solid cable-less internal construction for high shock and vibration resistance
- Passive conduction cooled and fanless thermal design

BENEFITS

- Compatible with leading edge Intel CPUs
- Ideal for space constrained, rugged, or extended temperature applications
- Easy CPU, storage and I/O upgrade reduces tech refresh costs using industry standard Type 6 COM Express and mini PCIe modules
- Intelligent mechanical design for reduced volume manufacturing costs
- Mighty Mouse or MIL-STD38999 I/O connectors for reliable performance in harsh environments
- The support services of Elma's experienced systems integration team

AVAILABILITY

8 to 12 weeks, configuration dependent

APPLICATION AREAS

Defense and rugged industrial applications that demand performance in extended temperatures and high shock and vibration environments.

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USA
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http//:www.emacinc.com/sales/ipac-9x25

Quantity 1 pricing for the iPAC-9x25 starts at $198/ea.

Please contact EMAC for OEM & Distributor Pricing.

FEATURES & BENEFITS

- Wi-Fi and Bluetooth [Optional]
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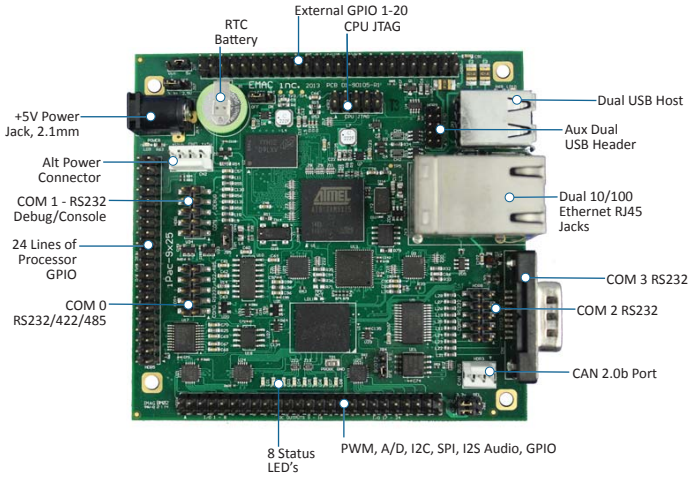
- Battery-Backed Real-Time Clock/Calendar, Up to 4x 16-bit Pulse Width Modulation (PWM)
- 7x A/D Channels with10-bit A/D Converter - 0 to 2.5V Range
- -40° to + 85° C Industrial Wide Temperature



TECHNICAL SPECS

- Atmel AT91SAM9x25 400 Mhz Processor
- 128 MB DDR2 RAM, 4 GB eMMC, 16 MB Serial Data Flash
- 2x Ethernet 10/100 Base-T with RJ45, 20x General Purpose SAM9X25 Digital I/O Lines, 16x SPI I/O Expander Based Digital I/O, 8x High Drive Digital Outputs
- 2x USB 2.0 High Speed, 1x USB 2.0 Full Speed Host Port, 1x USB 2.0 High Speed OTG (Host/Device), 1 CAN 2.0b Port
- 4x Serial Ports (3x RS232, 1x RS232/422/485)

AVAILABILITY

Now

APPLICATION AREAS

Industrial Automation, Test & Measurement, Data Acquisition, Industrial Control

CONTACT INFORMATION

EMAC, Inc.
2390 EMAC Way
Carbondale, Illinois 62902
United States
Tel: (618) 529-4525
Fax: (618) 457-0110
info@emacinc.com
www.emacinc.com

VersaLogic Corporation

Lion (VL-EPMe-42)

Compatible Operating Systems: Windows, Windows Embedded, Linux, VxWorks, and QNX
Supported Architectures: x86

The Lion is a high-performance single board computer (SBC) which combines Intel's 7th generation Core "Kaby Lake" processor, with a newer PCIe/104 OneBank expansion interface. Compatible with the PCIe/104-Express format, it includes a legacy PCI connector, and a high-speed PCIe connector. This provides flexible system expansion, while leaving more on-board space available for product features. The single bank connector is mechanically and electrically compatible with PCI/104-Express Type 1 and Type 2 modules. In addition, the Lion also contains a full complement of on-board I/O interfaces, including USB 3.0, USB 2.0, mini PCIe expansion socket, TPM chip, multiple serial interfaces, and 8-bits of digital I/O. The Lion is available with an embedded i7-7600U, i5-7300U, or i3-7100U Kaby Lake processor, providing standard clock rates up to 2.8 GHz and Turbo Boost rates to 3.9 GHz. The Kaby Lake processors feature dual-core CPUs and Hyper-Threading logic allowing up to 4 simultaneous threads to be executed. As with all VersaLogic products, the Lion is designed to support OEM applications where high reliability and long-term availability are required. Lion is backed by a five-year warranty, 5+ year off-the- shelf availability guarantee, and expert US-based technical support. From application design-in support, to its 10+ year extended life programs, the Lion provides a durable embedded computer solution with an excellent cost of ownership.

FEATURES & BENEFITS

- Intel "Kaby Lake" Processor - Up to 2.8 GHz clock rate, dual-core.
- Trusted Platform Module - On-board TPM security chip can lock out unauthorized hardware and software access.
- High-performance Video - Integrated Intel HD Graphics 620 core supports DirectX 12, OpenGL 4.4, and H.264, MPEG-2 encoding/decoding. Dual Mini DisplayPort outputs (DP++). DisplayPort supports HD audio output.
- Network - Dual Gigabit Ethernet (GbE) with remote boot support plus Mini PCIe Card Sockets. Supports Wi-Fi modems, GPS receivers, flash data storage with auto-detect mSATA flash storage support, and other mini PCIe modules.
- Industrial Temperature Operation -40° to +85°C operation for harsh environments. MIL-STD-202G Qualified for high shock / vibration environments.

TECHNICAL SPECS

- PCIe/104 OneBank™ form factor with stackable expansion (on back side). High speed stack-down PCIe connector
- Intel Active Management Technology
- Up to 16 GB RAM
- MicroSD Socket - Supports removable microSD card solid-state drives
- USB 3.0 and 2.0 ports, Serial I/O (RS-232/422/485),Digital I/O

AVAILABILITY

Currently on the shelf!

APPLICATION AREAS

For rugged OEM applications needing high-performance in a PC/104 format such as Defense, Medical and Industrial applications.

CONTACT INFORMATION

VERSALOGIC CORPORATION

VersaLogic Corporation
12100 SW Tualatin Rd
Tualatin, OR 97062
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IFTLE 350 DARPA Electronics Resurgence Initiative: Going Beyond Moore's Law

By Dr. Phil Garrou, Contributing Editor

IFTLE has discussed in detail the coming end of Moore's Law and the implications that holds for our electronics industry. For instance see IFTLE 300 "ITRS 2.0 – It's the End of the World As We Know It"

Well DoDs DARPA has stepped up and is attempting to lead the industry out of the quagmire that is the myriad of options that have presented themselves.

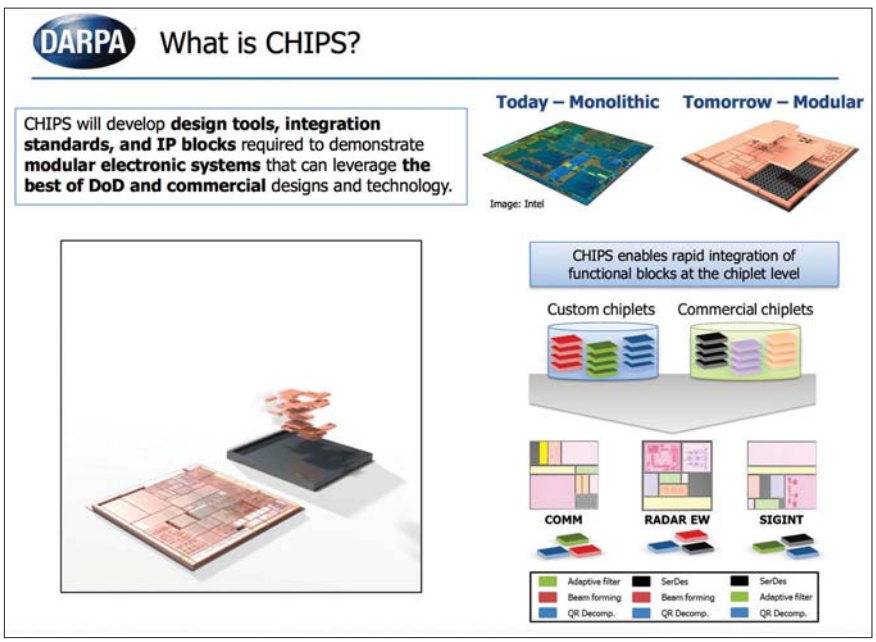
On June 1, DARPA's Microsystems Technology Office (MTO) announced a new Electronics Resurgence Initiative (ERI) "to open pathways for far-reaching improvements in electronics performance well beyond the limits of traditional scaling". Key to the ERI will hopefully be new collaborations among the commercial electronics community, defense industrial base, university researchers, and the DoD. The DoD proposed FY 2018 budget reportedly includes a $75 million allocation for DARPA in support of this, initiative. It is reported that in total we are looking at a $200,000MM program.

For details on the ERI see DARPA-SN-17-60[1].

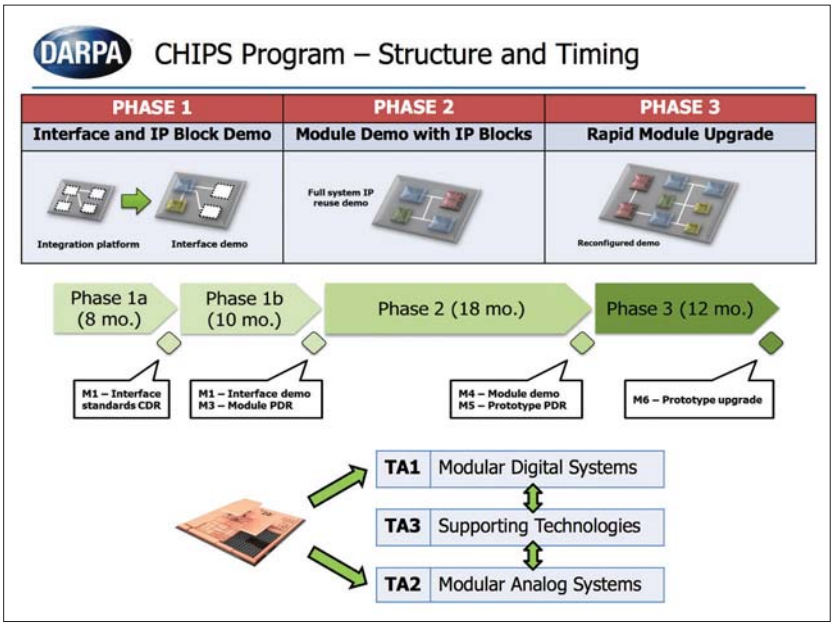
The program will focus on the development of new materials for devices, new architectures for integrating those devices into circuits, and software and hardware designs for using these circuits. The program seeks to achieve continued improvements in electronics performance without the benefit of traditional scaling. Bill Chappell, director of DARPA's Microsystems Technology Office (MTO), which will lead the program, announced "For nearly seventy years, the United States has enjoyed the economic and security advantages that have come from national leadership in electronics innovation.....If we want to remain out front, we need to foment an electronics revolution that does not depend on traditional methods of achieving progress. That's the point of this new initiative – to embrace progress through circuit specialization and to wrangle the complexity of the next phase of advances, which will have broad implications on both commercial and national defense interests."He continued "We need to break away from tradition and embrace the kinds of innovations that the new initiative is all about..."

Bill Chappell

The chip research effort will complement the recently created Joint University Microelectronics Program(JUMP), an electronics research effort co-funded by DARPA and SRC (Semiconductor Research Corporation). Among the chip makers contributing to JUMP are IBM, Intel Corp., Micron Technology and Taiwan Semiconductor Manufacturing Co. SRC members and DARPA are expected to kick in more than $150 million for the five-year project. Focus areas



1. http://bit.ly/2Bj4Xhw



include high-frequency sensor networks, distributed and cognitive computing along with intelligent memory and storage.

The materials portion of the ERI initiative will explore the use of unconventional materials to increase circuit performance without requiring smaller transistors. Although silicon is used for most of the circuits manufactured today, other materials like GaAs, GaN and SiC have made significant inroads into high performance circuits. It is hoped that the initiative will uncover other elements from the Periodic Table that can provide candidate materials for next-generation logic and memory components. One research focus will be to integrate different semiconductor materials on individual chips, and vertical (3D) rather than planar integration of microsystem components.

The architecture portion of the initiative will examine circuit structures such as Graphics processing units (GPUs), which underlie much of the ongoing progress in machine learning, have already demonstrated the performance improvement derived from specialized hardware architectures. The initiative will explore other opportunities, such as "reconfigurable physical structures that adjust to the needs of the software they support".

The design portion of the initiative will focus on developing tools for rapidly designing specialized circuits. Although DARPA has consistently invested in these application-specific integrated circuits (ASICs) for military use, ASICs can be costly and time-consuming to develop. New design tools and an open-source design paradigm could be transformative, enabling innovators to rapidly and cheaply create specialized circuits for a range of commercial applications.

DARPA CHIPS

As part of this overall Electronics Resurgence Initiative, DARPA, last week, had their kick of meeting for the CHIPS program (Common Heterogeneous Integration and Intellectual Property (IP) Reuse). We have previously discussed CHIPS here [see IFTLE 323 "The New DARPA Program "CHIPS"..."

The CHIPS vision is an ecosystem of discrete modular, IP blocks, which can be assembled into a system using existing and emerging integration technologies. Modularity and reusability of such IP blocks will require electrical and physical interface standards to be widely adopted by the community supporting the CHIPS ecosystem. The CHIPS program hopes to develop the design tools and integration standards required for modular integrated circuit (IC) designs.

Program contractors include Intel, Micron, Cadence, Lockheed Martin, Northrop Grumman, Boeing, Synopsys, Intrinsix Corp., and Jariet Technologies, U. Michigan, Georgia Tech, and North Carolina State University.

The CHIPS program will tackle digital interfaces and systems and their supporting technologies with the goal of:

- developing common interface standards
- enabling the assembly of systems from modular IP blocks
- demonstrating the reusability of the modular IP blocks via rapid design iteration

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Don't Underestimate the Challenges of IoT

Adhering to ISO 26262…avoiding repairs to IoT devices in hard-to-reach factory floor locations…dealing with the complexities of server-class chips with as many as eight CPU cores—developers will find no shortage of IoT hurdles to overcome

By Tom Anderson, OneSpin Solutions

After several years of hype about the potential for the Internet of Things (IoT), some sense of reality is emerging. Perhaps no one needs an Internet-enabled toaster, but there are plenty of other applications in the home, vehicles, and factories that do make sense. Many observers envision IoT devices as being incredibly cheap as well as ubiquitous, easily tossed away and replaced when they fail or become outdated.

This leads some engineers to believe that IoT designs can be done quickly and easily, with less rigor than goes into today's smartphones and other complex consumer devices. They may look to bypass some aspects of verification, perhaps settling for lower coverage goals or an informal test plan that does not correlate intended functionality and coverage. In many cases, there seems to be little concern about long-term safety and reliability.

Is an IoT device really the ultimate disposable product? Can designers and verification engineers really cut corners?

The situation is much more complicated than it might at first appear. For a start, IoT devices may contain highly sophisticated electronics. The Intel Atom family of processors, sometimes cited as ideal for IoT applications because of its lower power requirements, has grown to include server-class chips with as many as eight CPU cores. System-on-chip (SoC) devices built with these processors can be as complex as one can possibly imagine.

Verification of complex electronic designs, of course, remains a major challenge. It costs millions of dollars to turn a chip, so a bug that escapes to silicon can be costly to fix. A missed market window may cost hundreds of millions. IoT chips must be verified as thoroughly as designs for any other application. The high volumes

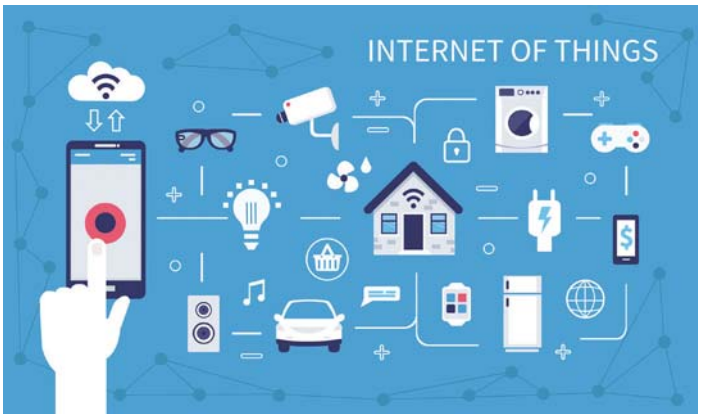

Figure 1: Not all devices connected by the IoT will be simple to design or verify. (Source: Fotolia)

expected for many types of IoT devices mean that any campaign to replace defective chips would be enormously expensive.

Further, many IoT devices will be in locations that are not easily accessible, making repair even more difficult. Such devices in the home or office include security cameras, environmental sensors, and heating and cooling controllers. On the factory floor, every second that production is halted costs money, so IoT repairs must be avoided. Even if a hardware bug can be fixed by an over-the-Internet software patch, some percentage of chips are likely not to update properly without manual intervention.

Some observers maintain that the majority of IoT devices will be built using field programmable gate arrays (FPGAs) rather than custom chips. This avoids the long delay and expense of fabrication for both the initial build and subsequent bug fixes. But repairs are just as difficult regardless of the chip technology used, and leading-edge FPGA design and verification engineers generally follow a flow much like their application-specific integrated circuit (ASIC) and custom chip counterparts. Choosing a complex FPGA, which may very well qualify as an SoC, offers no shortcuts for verification.

As if all this isn't enough, some categories of IoT chips must follow rigorous verification and safety standards, such as ISO 26262 for automotive electronics. These standards typically require high coverage metrics, with coverage points mapped back to the functional requirements for the product. The design must be bug-free before chips are fabricated. In the field, manufactured devices must be "safe" and robust in the presence of random errors such as a wire breaking or an alpha particle flipping a memory bit.

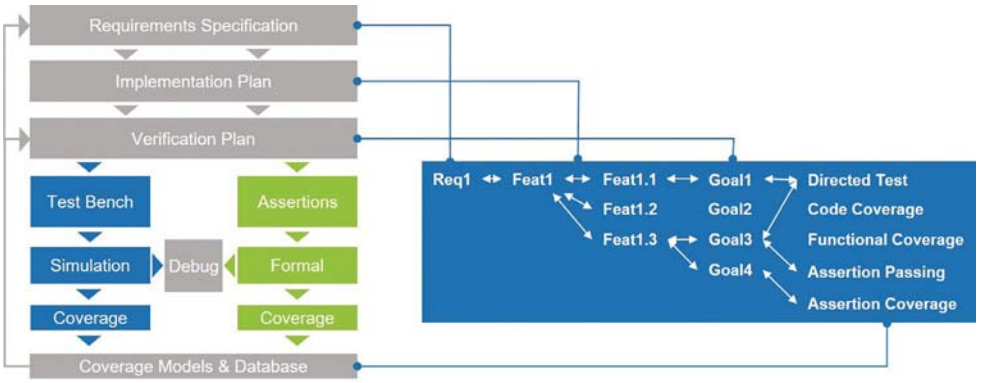

Figure 2: Robust verification of IoT devices requires a flow that maps requirements to features and uses appropriate coverage metrics to measure the contribution from multiple verification engines. (Source: OneSpin)

Tool vendors, chip suppliers, and systems houses must undergo a long process of certification to these standards. As knowledge of safety standards grows, consumers are likely to demand that all manufacturers be certified. In truth, verifying some classes of IoT devices may be harder than verifying a smartphone or tablet, not easier.

WHAT IS AN IOT VERIFICATION TEAM TO DO?

Many of the answers lie in formal verification technologies. Formal tools such as property checkers have the ability not just to find bugs, but to prove mathematically that there are no longer any bugs to be found. This provides a measure of certainty impossible to obtain with simulation or emulation alone. Formal tools operate on assertions about how the design should (and should not) operate. With standardized assertion formats and tools that can determine how much of a design is covered by assertions, many of the traditional barriers to the use of formal have been shattered.

This is especially true for formal applications ("apps") that verify specific aspects of the design with little or no manual effort. Some apps can extract certain kinds of design intent from the hardware description language (HDL) model or setup files and auto-generate assertions for formal analysis. Other apps include pre-packaged assertions. Many formal users rarely, if ever, write their own assertions, relying instead on apps to check for such issues as improper block connectivity, propagation of unknown values, and interface protocol violations.

The team must establish a robust verification flow, starting with requirements and mapping these to features that represent every aspect of desired behavior. The verification plan must specify which engines (simulation, emulation, and formal) will be used for each feature. Appropriate coverage metrics must be selected and monitored to ensure that every aspect of the design has been verified. Robust coverage metrics are now available from formal tools and these can be combined with results from simulation and emulation for a comprehensive view of verification completeness.

The verification team must also employ formal equivalence checking between the HDL model of the design and its gate-level implementation. Modern logic synthesis tools apply a wide range of transformations and optimizations to the design. Equivalence checking flags any mismatches due to synthesis tool errors, improper synthesis setup, or optimizations inappropriate for a particular design. Formal equivalence checking must be applied for FPGA designs as well as for ASICs and other custom chips.

Finally, where standards or consumer demand require long-term reliability, the team must verify that random faults during operation can be detected by hardware safety mechanisms. These faults must either be corrected or used to trigger an alarm of improper operation. This stage of verification is also performed primarily using formal techniques, including random fault injection, fault propagation analysis, and safety coverage metrics. If a fault simulator is used, the work can be cleverly split with the formal tools and the results can be combined.

In summary, IoT development teams do not get a pass on using the most advanced design and verification methodologies. They must verify their chips and devices thoroughly and, where appropriate, guard against random events that can compromise operation. The good news is that there are proven tools available today to meet all these challenges.

Tom Anderson is technical marketing consultant at OneSpin Solutions. His previous roles have included vice president of marketing at Breker Verification Systems, vice president of applications engineering at 0-In Design Automation, vice president of engineering at IP pioneer Virtual Chips, group director of product management at Cadence, and director of technical marketing at Synopsys. He holds a Master of Science degree in Computer Science and Electrical Engineering from M.I.T. and a Bachelor of Science degree in Computer Systems Engineering from the University of Massachusetts at Amherst.

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VORTEX86DX3 PC/104 RUGGED SBC

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- PC/104 standard compliant single board computer
- Watchdog Timer, software programmable
- Operation Temperature: -20C to +70C, -40C to +85C (Optional)
- Integrated 10/100Mbps Ethernet and RTL8111F GbE
- Isolated I/O with optional CANBus
- Supports SATA interface

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