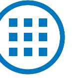
MAPPER

MAPPER: High throughput Maskless Lithography

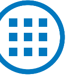
Marco Wieland

Today's agenda



- Introduction
- Applications
- Qualification of on-tool metrology by in-resist metrology
- Wrap up and conclusions

Today’s agenda



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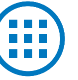
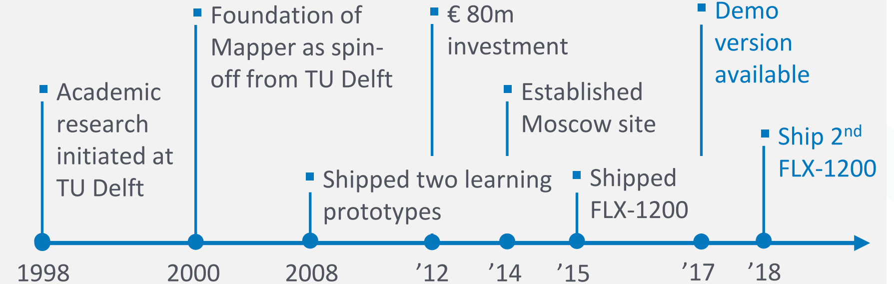
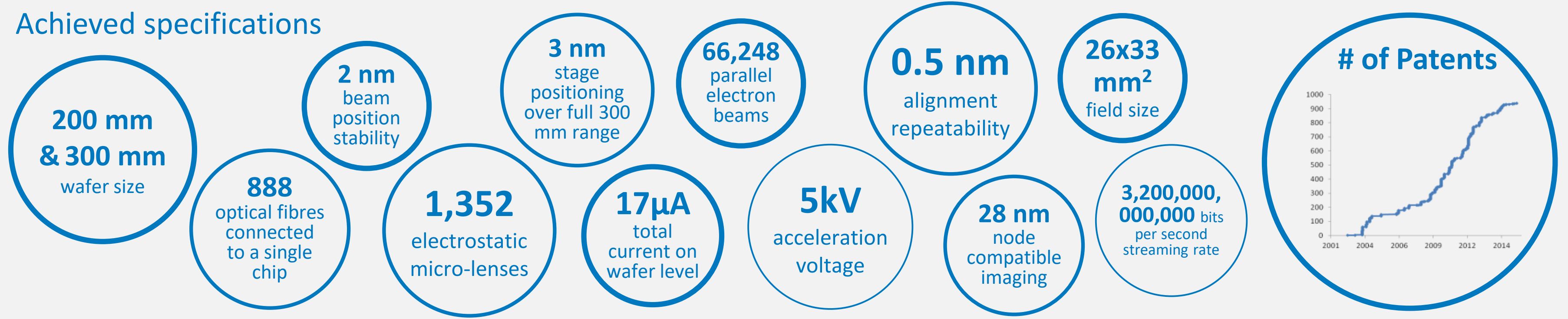
17 years of lithography innovation @ Mapper

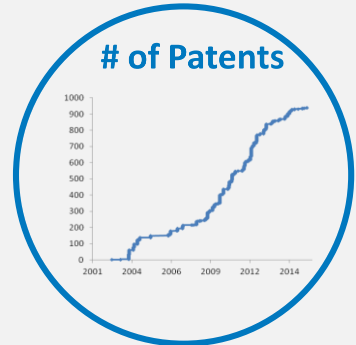


The vision of one man,
Arthur del Prado (1931-2016)

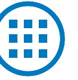
Father of the semiconductor equipment industry
Involved in the creation of ASML, ASM International and BESI
CEO of ASM International (1964 -2008)



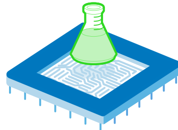


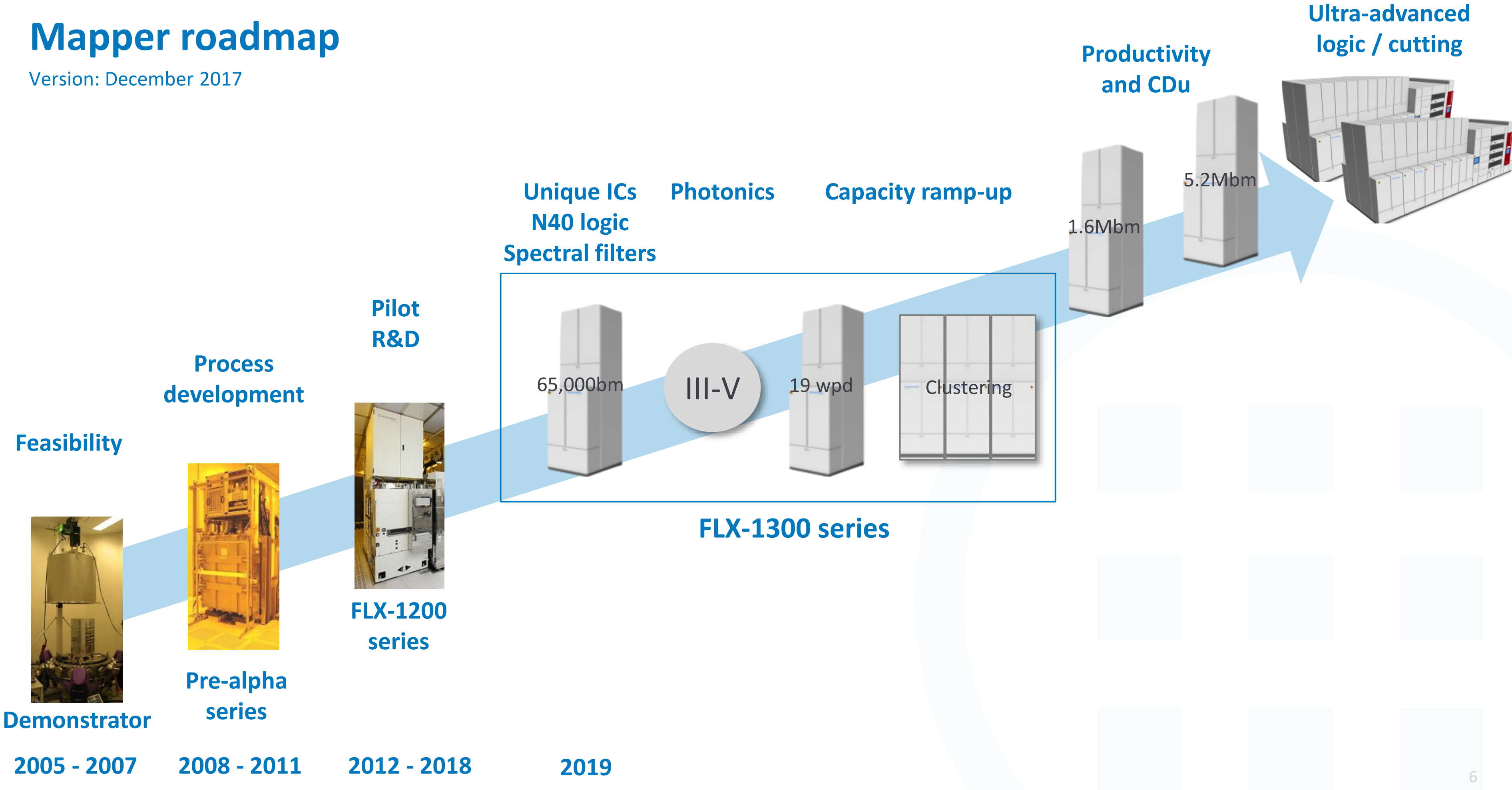


Mapper makes e-beam direct write for volume manufacturing possible

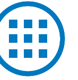


Traditional e-beam	Mapper FLX	FLX extension
1 electron beam per system	65,000 beamlets per unit	> 1,000,000 beamlets per unit
		Evolution on the same platform
No optical alignment	Compatible, optical, alignment	Unit clustering for >40 wph
No full wafer placement accuracy	Matching to DUV and 193i	
< 25 full 300 mm wafers per month	> 450 wafers per month (300 mm)	>5,000 wafers per month/unit
Throughput proportional to pattern density and resolution	Throughput independent of pattern density and resolution	It takes minutes only to expose a wafer at <50nm
Lab use only	Down to 40nm logic node	28nm logic node and below

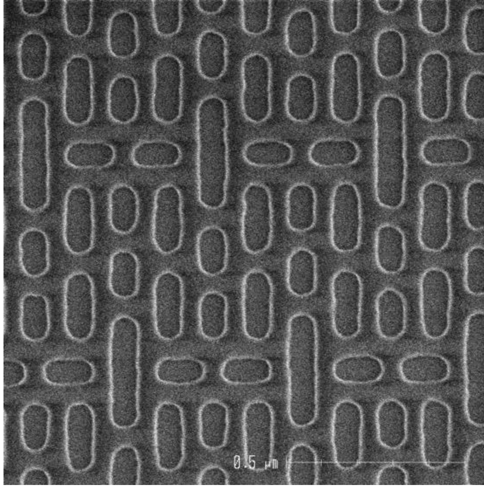



Mapper roadmap
Version: December 2017
Feasibility
Demonstrator
2005 - 2007
Process development
Pre-alpha series
2008 - 2011
Pilot R&D
FLX-1200 series
2012 - 2018
Unique ICs
N40 logic
Spectral filters
Photonics
Capacity ramp-up
65,000bm
III-V
19 wpd
Clustering
FLX-1300 series
2019
Productivity and CDu
1.6Mbm
5.2Mbm
Ultra-advanced logic / cutting
6

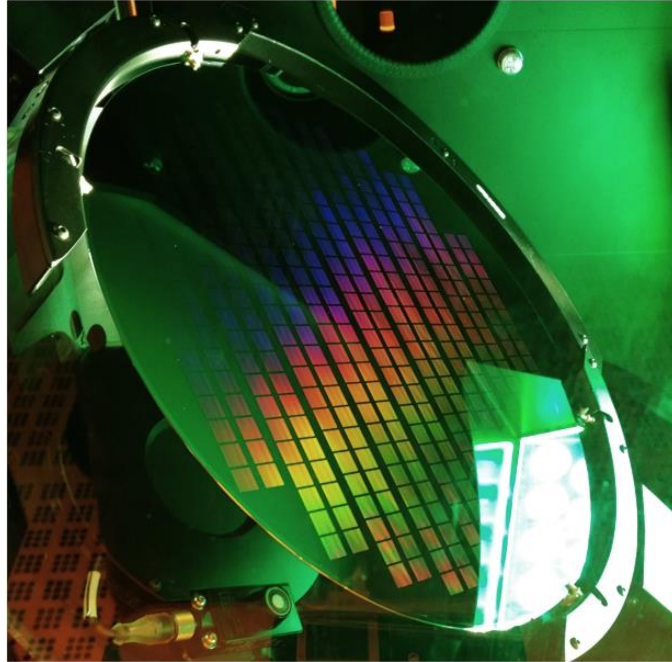
Status FLX-1200: full column operational at CEA-LETI as of August 2017



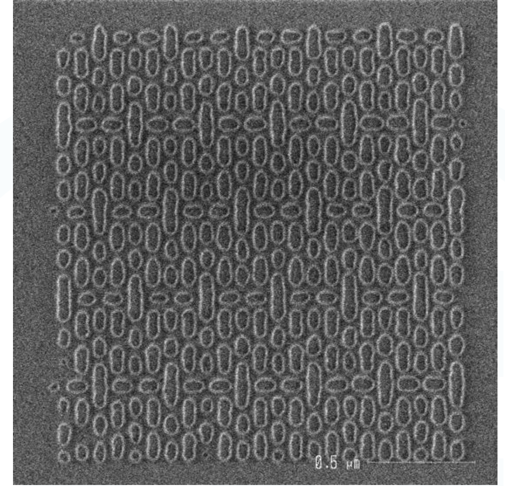
65k beams in 13x2 mm^2 slit. First exposures after upgrade to fully programmable blanker:



60 nm HP (N40)



Getting close to covering a full 300 mm wafer in 60 minutes



40 nm HP (sub N28)

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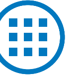

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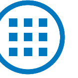
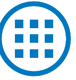
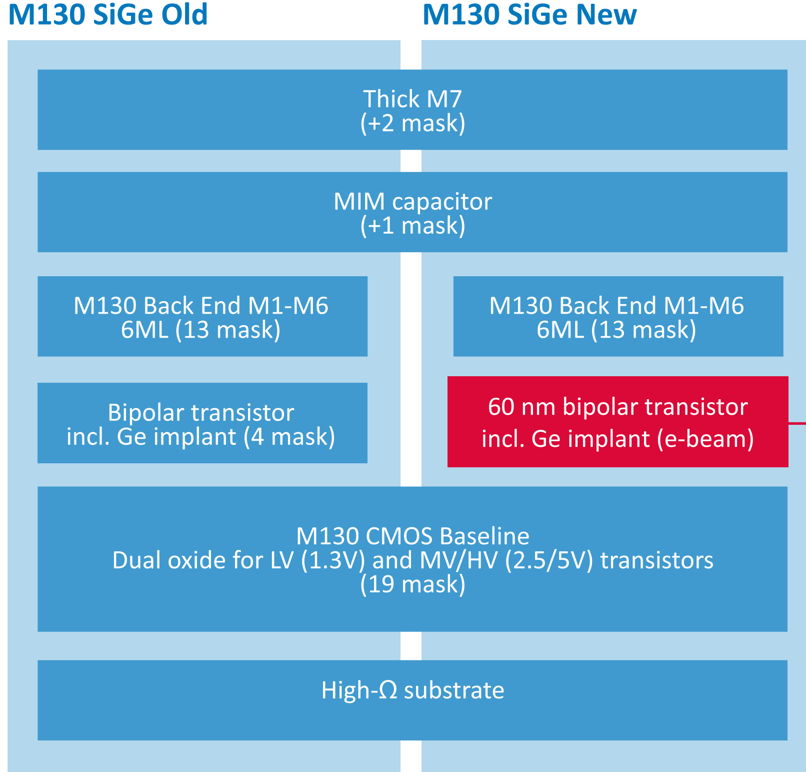
Many different end markets targeted by Mapper



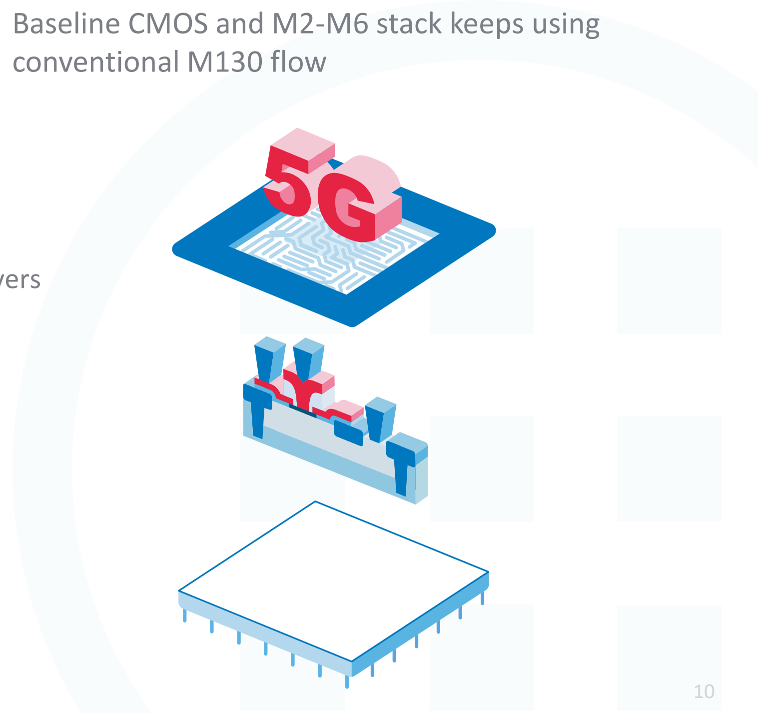
Mapper applications			Tool	Description
Mapper market potential	I R&D, prototyping and technology evaluation		FLX-1300	▪ Use in research labs/fabs for scientific experiments, prototyping and ultra-small-scale series production
	II Fab capability expansion	Defense and high-security applications	FLX-1300	▪ Use of maskless litho for small-series production (e.g., chip emulation) and to avoid external treatment of design data in mask shops
		III-V photonics devices & circuits	FLX-1300	▪ Use for producing III-V photonics circuits and passive devices, avoiding mask cost and enabling new device design features that cannot be produced with mask-based lithography
		Specialty silicon circuitry	FLX extension	▪ Use for small-series products for specialty applications in silicon, as a low-cost replacement of a mask-based system
	III Integrated CMOS sensor optics		FLX-1300	▪ Use for novel optical filters/elements that are directly integrated on top of a silicon CMOS sensor that cannot be produced using mask-based optical lithography
	IV Truly unique ICs	RFID	FLX-1300	▪ Use for 1 layer per chip creating unique, hard-wired ID for RFID tag to be used as trusted root of trust for security applications
		Scale-up across applications	FLX extension	▪ Embedding of unique, hard-wired IDs into security chips across different applications and uses (e.g., smart cards, IoT,…)

Technology migration with Mapper: <90nm SiGe technology on 8”

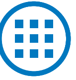


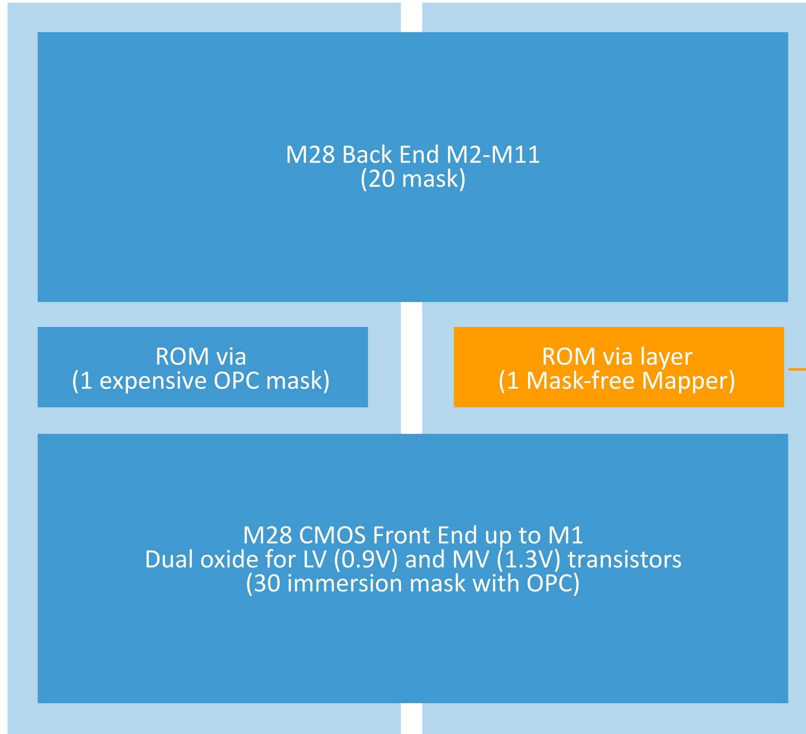


- Basic SiGe transistor (and M1) using Mapper for small feature size and (much) higher f_T
- Improved lateral control
- Baseline CMOS and M2-M6 stack keeps using conventional M130 flow

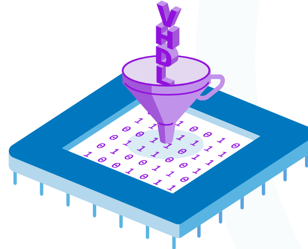


Technology migration with Mapper: ROM and structured ASIC





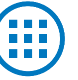
Mapper layers



Mapper layer replaces very expensive ROM-via programming layer in nodes where Flash is not available

- Classical optical mask very expensive due to closely spaced repetitive via pattern
- Mapper has no problem with these patterns and could even allow smaller ROM dimensions
- Mapper layer has a much faster turn-around time due to 100% software; one day cycles possible
- Eliminate need to add external memory → simpler and lower cost devices

Mapper tool can generate unique pattern for every chip



Data security

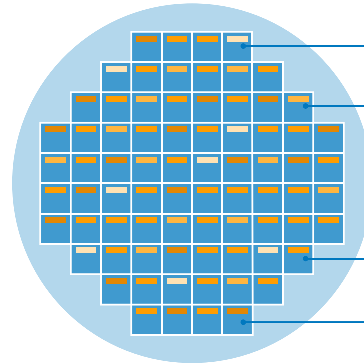
- Industrial infrastructure
- IoT gadgets
- Digital rights management
- Mobile storage
- Smart cards

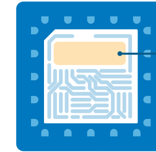
Traceability

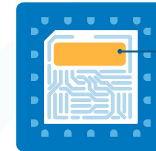
- Automotive
- Aviation
- Medical
- Postal
- Retail

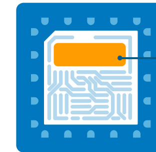
Anti-counterfeiting

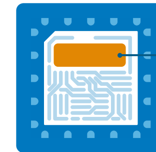
- Defense spare IC's for 20+ year old equipment
- Luxury goods
- Bank bills, coins



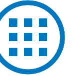


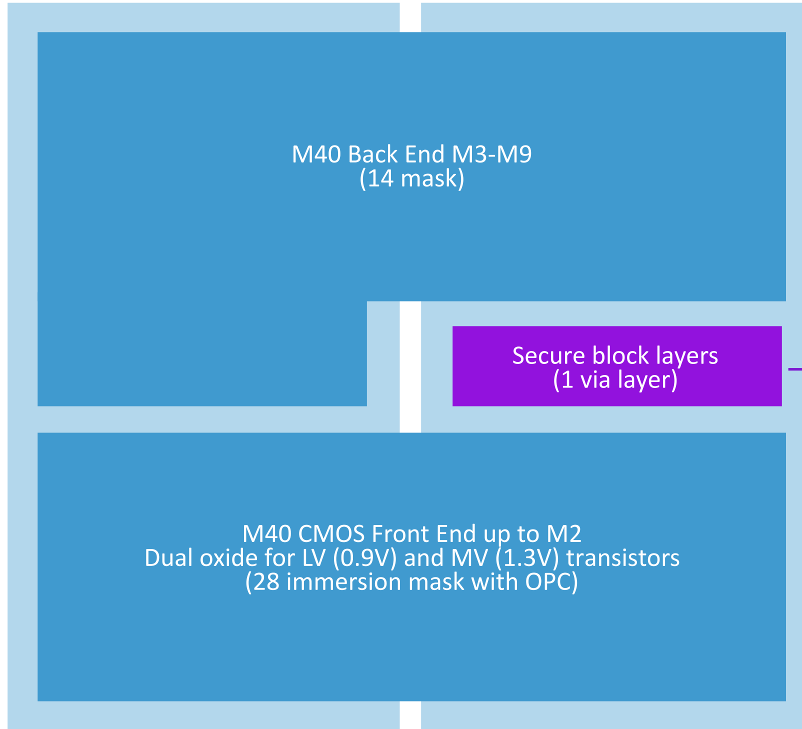


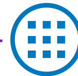




Technology migration with Mapper: Every chip unique



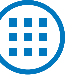




Mapper allows hard-wired, per chip unique IP

- E.g. security code generator
- Leaves all other parts off technology mask stack unchanged
- No additional mask costs, only additional processing time
- This example assumes secure IP on top of GO1+M1+M2 fixed block structure
- One via layer with Mapper
- Many variations possible

Today's agenda



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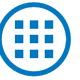
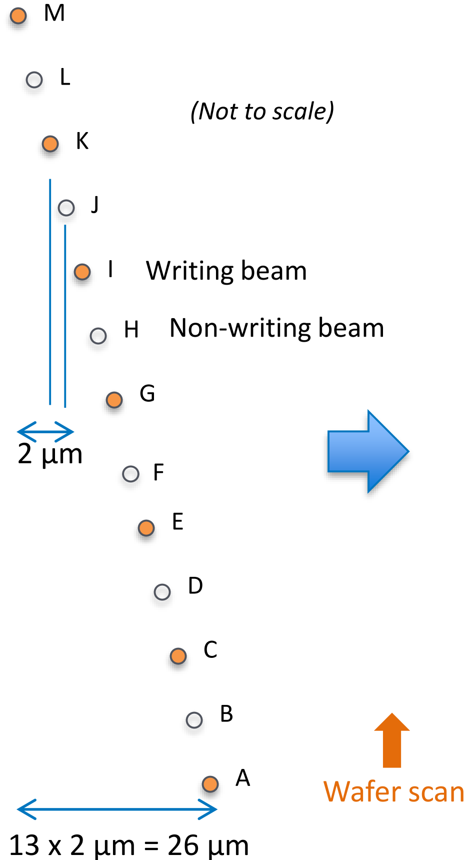
Redundancy: exposing with 50% of beams at the same time





M K I G E C A

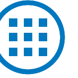
4 µm

10 µm

2 µm deflection

- We can't assume all beams are always working or fully within specification
- Therefore before every full scan of the wafer all beams are measured
- Then the 'good' beams are used to expose the wafer
- **Therefore we need an additional 'redundancy scan' to complete the whole wafer**

Beam properties corrected in datapath based on on-tool metrology



Before

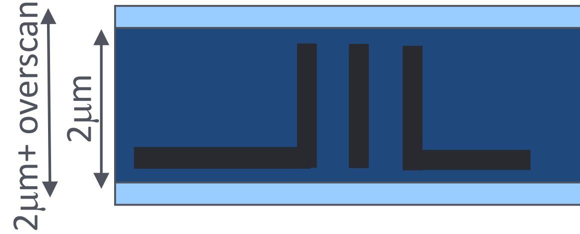
After

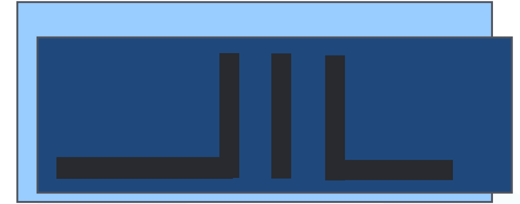
Shift

-beam position

-field size + shape (for overlay)

-field position

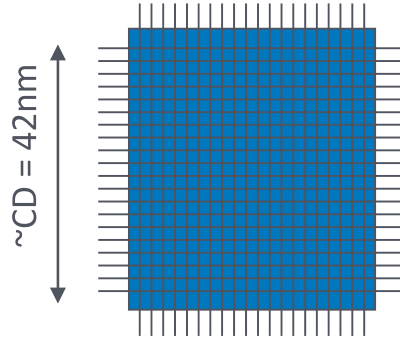


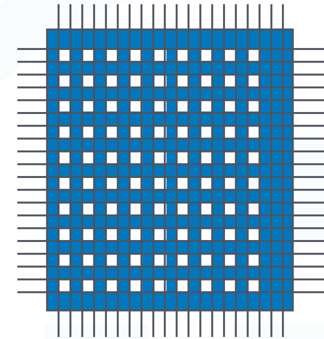


Beam to beam dose

-beam to beam current

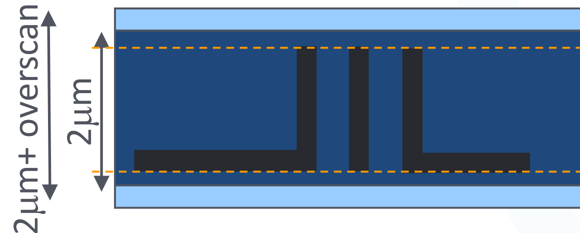
-part of btb deflector strength

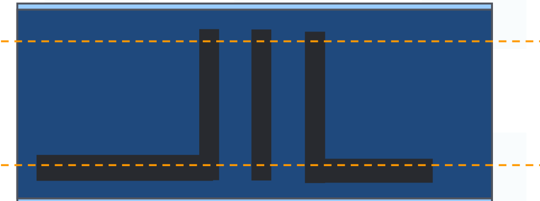




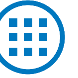
Scale

- beam to beam deflector strength





Results of on tool metrology qualification in Leti presentation

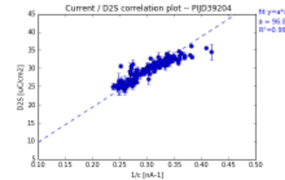


THE MAIN ACHIEVEMENTS (ABOUT THE INTERNAL METROLOGY)

Goal = to correlate the in tool measurements (tool parameters) with the in resist (after exposure) measurements:

✓ **Beam current vs dose to size**

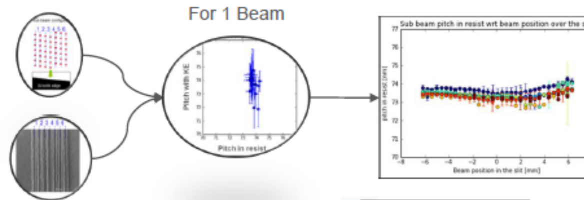
- Current measurement of each Beam (@ ≠ process steps)
- Dose to size measurement CD-SEM in resist exposed for each beam



Stable correlation kept for >5h with multiple loading & unloading in the tool

✓ **Sub beam pitch**

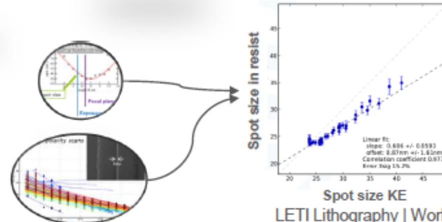
- 49 Sub Beams scan a Knife Edge
- CD SEM measurement form exposed dense line



Uniform & Narrow distribution across the slit (blanker)

✓ **Sub beam spot size**

- All beams scan a Knife Edge in parallel (spot size vs focus)
- CD SEM measurement form exposed line (CD vs Dose)



Robust & good correlation (performed on several exposure & sub-beams)

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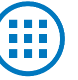

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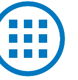
Wrap up and conclusions



Roadmap:

- FLX-1300: step in manufacturability, availability, overhead reduction
- FLX-1300: will support various wafer sizes and substrates
- Path to 1.6M and 5.2M beams to improve productivity and CDu

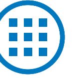
Application highlights:

- Fab capability expansion
- Truly unique IC’s

Qualification of on-tool metrology by in-resist metrology

- Beam selection
- Tool calibrations

Put your design on the demo shuttle



- FLX-1200 can print fields of 5mm x 5mm
- If you want your design printed, contact:

Bert Jan Kampherbeek

Mapper Lithography

Bert.Jan.Kampherbeek@mapper.nl

Laurent Pain

CEA-Leti

Laurent.Pain@cea.fr

Thank you for your attention