White Paper

Altera's Strategy for Delivering the Benefits of the 65-nm Semiconductor Process

Introduction

Altera's strategy for delivering the benefits of the 65-nm semiconductor manufacturing process focuses on leveraging advanced technologies and methods to provide the most capable and highest performance devices at the lowest cost, while minimizing risk and ensuring short time-to-market for customers. Altera's market share gains with 130 nm and 90 nm devices demonstrate that containing the risks of advanced semiconductor technologies improves an FPGA architecture's attractiveness in the market. To that end, Altera has been steadily developing and testing its 65-nm technology since early 2003. This paper explores the engineering strategies Altera uses to minimize production and schedule risk to customers while delivering the substantial improvements in density, performance, cost, and power consumption that are possible with the 65-nm process.

The 65-nm process presents specific product definition, design, and delivery challenges as semiconductor fabrication techniques are pushed to new limits. Undesirable deep submicron effects, including increased power consumption, process variation, and parametric failures that were manageable at 130- and 90-nm channel lengths, become pronounced engineering challenges with the 65-nm process. The physical realities of IC development with this process represent significant risks that can jeopardize the capabilities or manufacturability of an FPGA. Because many customers choose programmable logic as a risk mitigation strategy, Altera is taking the most proactive and comprehensive approach in the industry to control that risk.

Power Consumption at 65 nm

The move to the 65-nm process delivers the expected Moore's law benefits of increased density and performance. For example, the next-generation Stratix® FPGA family based on 65-nm processes will reinforce Altera's density leadership and extend the Altera® device advantage by delivering significantly more performance compared to 90 nm-based Stratix II devices. The 65-nm process will also reduce the cost of the Altera Cyclone® series of devices, resulting in an even greater price/performance advantage versus competitive offerings.

However, the performance increases made possible with the 65-nm process can result in significant increases in power consumption, introducing the risk of devices that consume unacceptable amounts of power. If no power-reduction strategies are employed, power consumption becomes a critical issue because static power can increase dramatically with the 65-nm process. Static power consumption rises largely because of increases in leakage current, including tunneling current across the thinner gate oxides that are used in the 65-nm process, as well as subthreshold leakage (channel- and drain-to-source current). Figure 1 shows how these sources of leakage current (shown in blue) increase as the technology makes smaller gate lengths possible (shown in green). Also, without any specific power optimization effort, dynamic power consumption can increase due to the higher density of switching transistors combined with the higher switching frequencies that are attainable.

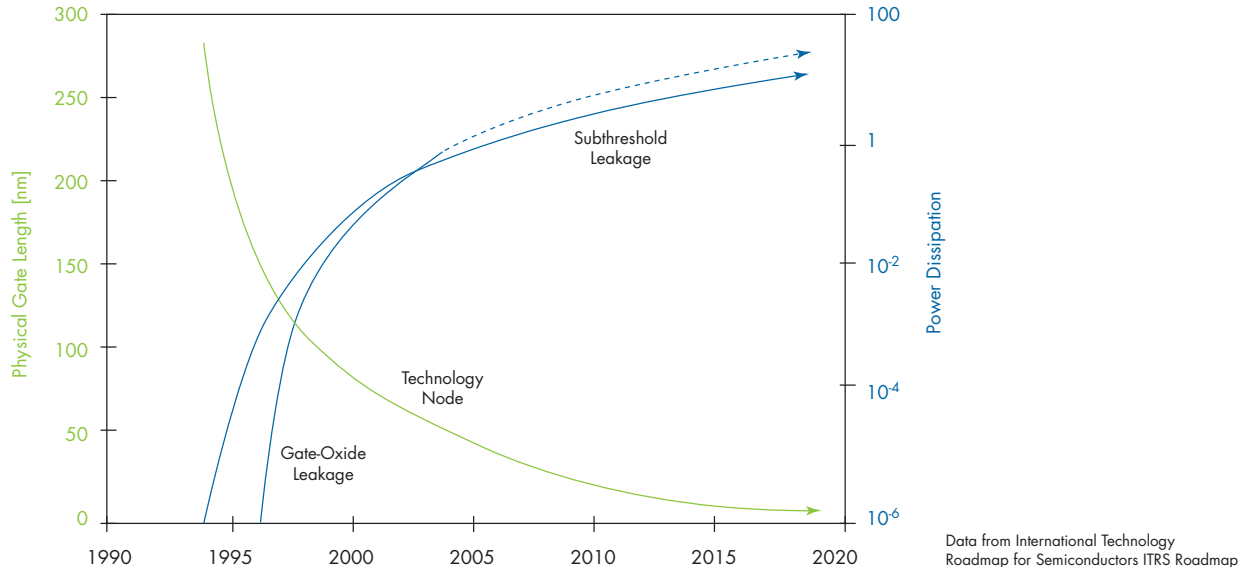

Figure 1. Static Power Dissipation Increases Significantly at Smaller Process Geometries

Although power requirements vary across different applications, the benefits of lower power consumption are applicable to any hardware platform because of the inherent cost, complexity, and reliability advantages. In addition to the power properties of the 65-nm process, today's design trends—such as increasing compactness of system form factors and portability—have significantly heightened the sensitivity to power consumption in PLDs. In "tethered" applications where wall power is the primary source, system enclosures are becoming dramatically thinner and smaller, restricting airflow, heat sink, size, and other thermal management solutions. In portable applications, a relatively new domain for FPGAs, battery-life objectives place new restrictions on both static and dynamic power consumption. These shifts in design goals promote power consumption to the first-order selection criteria for PLDs.

"Performance Where You Need It"—Altera's Strategy for Power Reduction

Altera's devices and the Quartus® II software that customers use for designing are engineered in a tightly coordinated and integrated effort between Altera's IC designers and software engineers. For example, IC designers and software engineers at Altera can analyze trade-offs between power and performance using a common, shared set of models, and identify whether the best solution will be a silicon or a software feature. Altera's strategy for 65-nm power reduction combines advanced process techniques, architectural enhancements, and powerful software tools that provide customers with maximum control over balancing power and performance requirements. It also results in the most accurate power estimation tools for programmable logic today.

Altera's strategy for power reduction is to give customers maximum control over balancing power and performance requirements. The elements of Altera's 65-nm power-minimization strategy include:

- Power-optimized silicon processes
  - Triple oxides
  - Strained silicon
  - Low-k dielectrics
- User-selectable core voltage
- Programmable power technology
  - High-performance mode
  - Low-power mode
- PowerPlay power analysis and optimization tools built into Quartus II software

Power-Optimized Silicon Processes

With the 65-nm process, Altera employs a triple-oxide process technology to reduce leakage current. Triple oxides increase transistor voltage thresholds and reduce their performance, so Altera applies this technique to transistors judiciously to minimize power consumption while still providing the best performance for user designs. Altera also uses strained silicon, which increases carrier mobility in transistors, enabling increased drive current without corresponding increases in leakage current. Finally, Altera uses low-k dielectrics to insulate metal layers, which reduces capacitance and has a direct relationship with reducing dynamic power consumption.

User-Selectable Core Voltage

User-selectable core voltage gives the customer the ability to choose varying levels of power and performance. Choosing the lowest supported core voltage reduces dynamic power consumption by an average of 30 percent. If performance does not meet the requirements, the user can change to a higher voltage, then use different techniques to reduce power without violating timing requirements, as outlined in Figure 2.

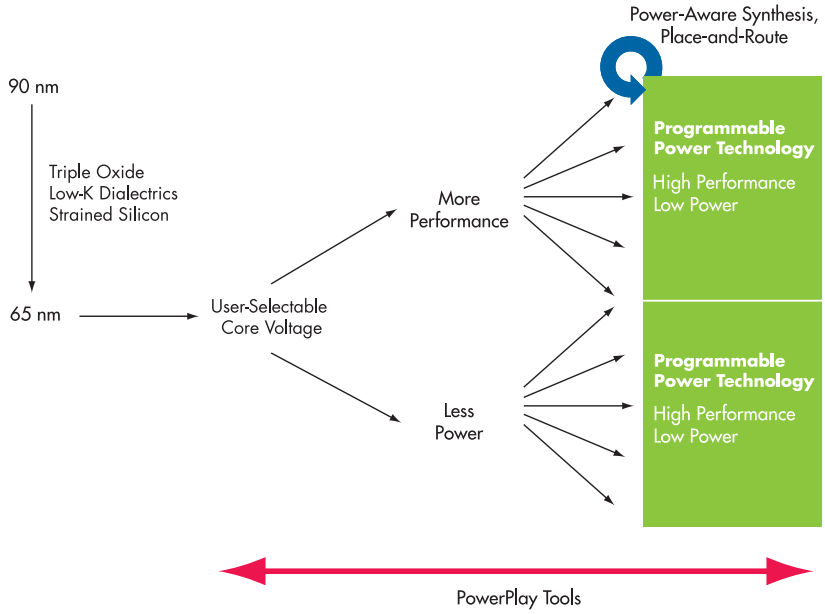

Figure 2. Altera's Efforts at Reducing Power Consumption With the 65-nm Process Include Process Optimization and User-Controlled Power-Optimization Tools

Programmable Power Technology

Altera's analysis of typical FPGA designs shows that they vary widely in terms of the numbers of critical paths, as well as in terms of the speeds that those critical paths need in order to meet end-users' performance requirements. This analysis shows that, on average, about 10 percent of the logic in a high-density FPGA is in the actual critical path of the design. Altera's programmable power technology enables individual logic circuits in the device to be configured to run in a high-performance mode or a low-power mode. Using this unique technology, critical paths can be programmed to operate in high-performance mode, while the rest of the design operates in low-power mode to minimize power consumption. With this powerful FPGA architecture feature, users will be able to get performance that meets the specific needs of their design, while minimizing power consumption throughout the rest of the device.

Users take advantage of these power consumption features by using Altera's Quartus II software. It contains the most accurate power tools in the PLD industry, including a power optimization advisor, power estimation, and three stages of power optimization, outlined below:

- *"Power-aware" logic synthesis:* Quartus II software synthesizes the design to reduce or eliminate logic that toggles at a high frequency and minimizes the number of RAM blocks accessed at each clock cycle.
- *Power-aware placement and routing:* Quartus II software places signals to minimize capacitance, or creates more power-efficient DSP block configurations.
- *Power-aware mode assembler:* Quartus II software programs unused portions of the device to operate in low-power mode so overall power is minimized.

PowerPlay Power Analysis and Optimization Tools

Quartus II software includes the PowerPlay power analysis and optimization tools, which offer automated power optimization based on timing constraints. The design engineer simply sets the timing constraints as part of the design entry process and synthesizes the design. The PowerPlay power analysis tool automatically selects the required performance for each piece of logic as well as minimizes power through power-aware placement and routing. The resulting design meets the customer's timing requirements with minimum power consumption.

Altera's Power/Performance Advantage

Altera's power consumption strategy for the 65-nm process significantly reduces the leakage current in its 65-nm devices. Despite industry concerns that high leakage current in 65-nm devices would present a considerable detraction for users by resulting in an unacceptable amount of static power consumption, Altera's 65-nm FPGAs deliver lower static power than its 90-nm FPGAs and competing 65-nm FPGAs. Through aggressive and innovative power reduction techniques, Altera's 65-nm FPGAs also consume less dynamic power than 90-nm FPGAs and competing 65-nm FPGAs, while delivering better performance.

In addition to offering lower power consumption, Altera extends its performance advantage over competitive 65-nm offerings. For example, a design migrated from a 90 nm-based Stratix II device to a 65-nm Stratix III device can expect to see a 50 percent reduction in total power at the same operating frequency (see Table 1). Users who want to maximize their performance by moving from Stratix II FPGAs to Stratix III FPGAs can expect to see a 30 percent reduction in power consumption while gaining a 20 percent performance boost.

Table 1. Altera's Efforts to Reduce Power Consumption With the 65-nm Process Result in Lower Power Consumption Than 90-nm Devices While Increasing Performance

Design Clock Frequency	Change in Total Power Consumption From Stratix II Devices to Stratix III Devices
+20%	-30%
Parity	-50%

Through the overall combination of power management steps from process innovations to intelligent power management through FPGA design software, Altera users obtain maximum benefits of the 65-nm process to get the performance they need, along with the lowest possible power consumption.

Production Challenges at 65 nm

While Altera has overcome these power complexities, there are also production risks inherent with the transition to more advanced processes. At smaller geometries, variability in the manufacturing process has a much greater impact on device operation. Variability in the semiconductor manufacturing process arises from many sources, including lithographic effects, changes in metal thickness resulting from chemical-mechanical polishing (CMP), dopant fluctuations, variances in gate length and oxide thickness, and well proximity effect (WPE).

In particular, lithography with the 65-nm process is a significant challenge because the dimensions of the device features and the spaces between them are less than half the wavelength of the light that is used to create them. This means that silicon features on a die cannot be created simply by using a photomask that corresponds to their shape and size, because distortion will cause the resulting feature to deviate from the intended shape. Many methods have been developed to address this problem, including resolution enhancement technologies (RET) like optical proximity

correction (OPC) and phase-shift masks (PSMs). However, none of these eliminates all of the distortion resulting from lithography, and some introduce additional distortions, resulting in further variations.

No matter the source, these variations present significant challenges in submicron semiconductor manufacturing. For example, WPE can contribute as much as 60 mV to threshold voltage variation in 90 nm designs, severely affecting the ability to design circuits predictably*(1)*. These effects become even more severe as the space between transistors is reduced. Parasitic resistive and capacitive effects resulting from layout also represent significant hurdles to manufacturing at submicron levels, since they impact timing and signal integrity, and are increasingly difficult to model and analyze.

Strategies to Minimize Production Risk at 65 nm

Altera is applying the latest techniques to minimize the negative impacts of variation in 65-nm manufacturing. To deliver the benefits of the process reliably while minimizing the risks of leading-edge technology, Altera employs a strategy that includes advanced process techniques, a comprehensive 65-nm test-chip program, and a proven system of reducing defect densities.

Statistical Static Timing Analysis Reduces Process Corner Variation

One of the new manufacturing stabilization techniques that Altera leverages is statistical timing modeling and analysis, which takes into account statistical distributions of timing and functionality under varying process, voltage, and temperature conditions rather than the traditional approach of focusing solely on best- and worst-case values. With these distribution results, Altera can better maximize performance and parametric yield by understanding the probabilities of how circuits will operate under the many conditions and variations to which they are subjected.

To support leading-edge techniques like statistical timing modeling, Altera develops proprietary methods and adopts advanced tools from multiple EDA vendors. For example, Altera is using the "variation-aware" Star-RCXT tool from Synopsys for parasitic extraction to generate accurate resistance capacitance (RC) parasitic values. Star-RCXT, which has also been adopted by Toshiba, Renesas, and ATI for submicron design, can deliver accurate modeling of the parasitics resulting from the many variations arising from 65-nm manufacturing, including WPE and the metal fill process used to offset variability from CMP*(2)*. By applying the latest techniques and tools to understand and evaluate the many challenges introduced by 65-nm design, such as new sources and values of parasitics, Altera reduces the uncertainty associated with manufacturing and reliably yielding 65-nm devices.

Unique Redundancy Technology Improves Device Yields

Altera is the only programmable logic vendor that leverages patented redundancy technology. Redundancy is a very effective method for improving device yields and device availability. Altera applies this technology by embedding extra, or "redundant," columns of circuitry into its FPGAs. If a column becomes subject to a manufacturing defect, it can be deactivated and the redundant column activated by the use of electrical fuses. This technology saves a die and thereby increases the total yield of a silicon wafer.

Redundancy is very effective with larger die, which are more likely to be impacted by defects, especially in the early stages of a process or early in the life of a device. The addition of redundancy to the process improves yields for large die devices by up to eight times, as shown by the yellow line at the top of Figure 3. In this way, redundancy improves product yields early in the process life cycle, brings the costs down more quickly, and increases overall availability. As the manufacturing process matures and defect densities improve, redundancy continues to play an important role, enabling Altera to achieve twice the device yield in the long term, as indicated by the blue line in Figure 3. Overall, redundancy plays a major role in Altera's ability to achieve production-quality status for its products and reliable high-volume production more quickly than other programmable logic vendors, particularly with high-density products.

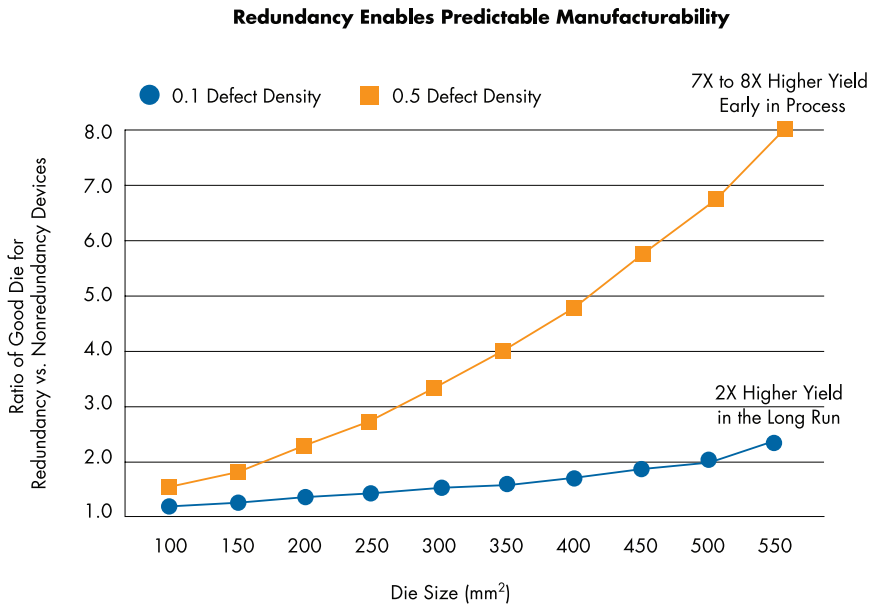

Figure 3. Redundancy Delivers Higher Yields Throughout a Product's Life Cycle, as Shown on This Graph Measuring Die Size vs. Ratio of Total Good Die in Redundancy Devices vs. Nonredundancy Devices

Comprehensive Test Chip Program Reduces Customer Risk

Altera demonstrated with its 130-nm and 90-nm devices that test chips were a valuable tool for early evaluation and refinement of architecture and device features on new semiconductor processes. This strategy helped Altera achieve smooth ramps to volume production of these devices, which has proved to be a point of distinction in the programmable logic industry. Altera taped out its first 65-nm test chips in April 2003, the first of 11 test chips designed to carefully evaluate different circuits, modules, and design techniques. Altera's test-chip program, the most comprehensive in the industry, allows it to evaluate all the elements of its 65-nm process well in advance of product introduction. With each successive test chip (shown in Table 2), Altera implements additional features and architectural elements to truly characterize and prove its designs, including early technology assessments, feasibility testing and validation of circuits and features, and confirmation of routing structures and architecture, as well as optimization and refinement.

Table 2. Altera's Comprehensive Test Chip Program Ensures That Customers Are Shielded From the Risks of Advanced Process Development

Test Chips	Tape Out
TC1	Q2 2003
TC2	Q3 2004
TC3A	Q2 2005
TC3B	Q2 2005
TC4	Q3 2005
TC5A	Q3 2005
TC5B	Q3 2005
TC6A	Q4 2005
TC6B	Q4 2005
TC7	Q1 2006
TC8	Q2 2006

By collecting and analyzing the test-chip data, Altera gains valuable insight into the impact of random and systematic variations, and is able to develop design strategies to reduce or eliminate them. Altera's significant investment in test chips ensures that customers are shielded from the many risks posed by leading-edge semiconductor design. This emphasis on risk management reflects Altera's commitment to reliably deliver new technologies without exposing customers to inconsistent or limited product availability, or products that fail to operate as specified, both hazards that have recent precedent with premature device introductions by other FPGA companies. As a result, Altera is on track to introducing its first 65-nm products later this year, with volume production in 2007.

Methodical Checkout Procedures

Beyond the test-chip stage, Altera performs a rigorous checkout, encompassing the development and manufacturing stages, to ensure that all of its silicon products operate exactly as specified. The checkout is comprised of the following steps:

1. Altera's IC design team ensures that the design meets the functional, performance, and power specifications through a vast number of simulations.

2. Through rigorous checking programs, Altera CAD and layout groups ensure the implementation of the design on the mask fully meets all of Altera's and TSMC's mask rules so the design can be processed successfully.

3. Cross-functional teams perform design-for-manufacturability (DFM) analysis with TSMC on critical die areas to ensure robust manufacturing. This involves a detailed review of the design layout with a view to removing any marginalities and making optimizations to the layout based on knowledge of the process technology to maximize yield.

4. TSMC's mask facility ensures that the masks are properly manufactured. The resulting products can be manufactured in high volumes with no yield or functionality issues due to mask dimension marginalities or defects.

5. Altera works with TSMC to ensure that the silicon is manufactured properly, meeting all appropriate in-line physical specifications (layer thicknesses, line widths, etc.) and end-of-line electrical specifications (transistor characteristics, metal line resistances, etc.).

6. Altera product engineering performs a full suite of characterization at both the wafer level and the packaged unit level to ensure that the end product meets all specified functional, performance, and power specifications. They also characterize nonfunctioning units and work with other Altera teams to determine causes for yield loss, which is fed back to TSMC for yield improvement activity.

7. Altera's applications team tests the device from the user's point of view, exercising all device features, using Quartus II software to develop configuration files and program the device, testing I/O voltage levels, and verifying functionality of all architectural elements.

8. Altera's reliability group subjects both test chips and final products to rigorous environmental tests to ensure the short-term and long-term quality of the final product before it is shipped to customers.

This uniform process is used and improved upon with each new device family offered by Altera. By applying these rigorous test and checkout procedures to every product, Altera ensures the highest levels of quality and reliability, as well as availability.

Altera's Foundry Partner Strategy—The Best in the Industry, the Strongest Partnership

Altera's foundry partner, TSMC, is the foundry market leader. TSMC has over 50 percent of the worldwide market share among dedicated foundries and an annual research and development investment 55 percent greater than its nearest competitor. These investments have resulted in industry-leading positions in lithography and

design-for-manufacturability (DFM) that further ensure TSMC's success in delivering products at advanced process generations. For example, TSMC is a pioneer in immersion lithography, a next-generation process that combines lithographic lenses with clear liquids to preserve higher-resolution light, enabling smaller, more densely packed devices.

TSMC complements its lithography expertise by creating its own mask sets, which creates a direct feedback mechanism on device yields. TSMC is one of very few foundries that provides this capability, and its mask-making facilities are the longest-running operation of its kind in the industry, allowing TSMC to improve its manufacturability and yields more rapidly and efficiently than its competitors. This infrastructure also provides strong support for TSMC's leadership in DFM efforts, which have produced the first DFM compliance initiative including the first unified data format for DFM across multiple tools, the first DFM data kit, and the first programs for defining DFM compliance for libraries and IP.

A strength of the Altera-TSMC partnership in achieving 65-nm success is the long-standing commitment the companies have to each other in pursuing advanced process technologies. By concentrating its efforts with the industry's strongest foundry player rather than dividing its attention among multiple foundries, Altera can focus on delivering reliable products without the risk of product inconsistencies that arise with multiple fabrication partners and the supply chain disruption that can result.

One of the most significant results of the Altera-TSMC partnership has been the steady reduction in defect densities achieved in Altera's products through the companies' joint efforts. Defects in the silicon process are inevitable, and defect densities are often quite high during the early part of a new process. Altera and TSMC actively work to reduce these defect densities through a combination of continuous feedback plus enhancements and improvements to manufacturing. Over the last five process generations, Altera and TSMC have not only reduced defect densities effectively, but have accelerated this reduction (see Figure 4). This coordinated effort to drive defect density reduction has taken many process generations to develop. As a result of this effort, the longest such in the programmable logic industry, Altera and TSMC are in the best position to get 65-nm FPGAs to market quickly, reliably, and with smooth ramps to volume.

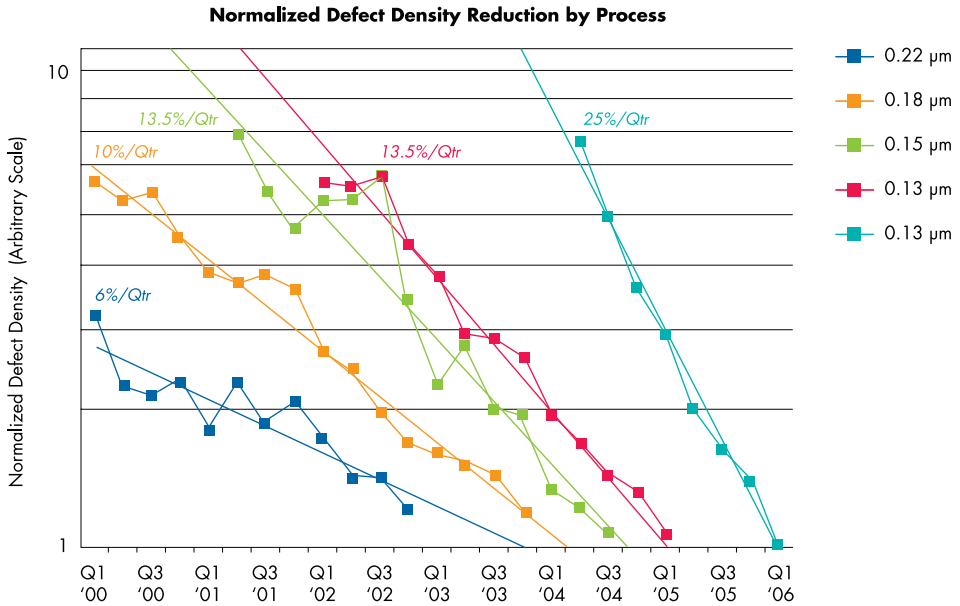

Figure 4. Normalized Defect Densities in Altera's TSMC-Based Products vs. Last Five Process Generations Show How Altera and TSMC Together Accelerate Reductions in Defect Densities Over Time

Accompanying Altera in partnering with TSMC to develop the 65-nm process are several other semiconductor industry leaders, including Broadcom, QUALCOMM, and Freescale. With these major semiconductor vendors driving its process technology, TSMC is in a unique position among dedicated foundries to deliver the highest reliability and quality in its 65-nm manufacturing.

Conclusion

Altera delivers the most advanced technology with the benefits and capabilities that its customers require to rapidly develop and manufacture successful, innovative products. While the promised benefits of the 65-nm process, including higher performance, greater logic density, and lower cost, continue to be very important programmable logic value propositions, users are increasingly concerned about improving productivity and lowering risk. Altera takes the most comprehensive approach in the programmable logic industry to deliver the benefits of the 65-nm process, while addressing the power issues and manufacturing challenges that have the greatest potential to undermine these benefits.

References

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