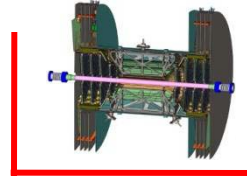


Sensors/FPHX Readout Chip

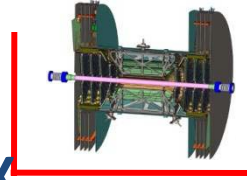
WBS 1.4.1/1.4.2

Jon S Kapustinsky



Outline

- Overall design of the FVTX wedge and FPHX readout chip
- Silicon sensor specifications and tests
- FPHX specifications and tests
- Schedule

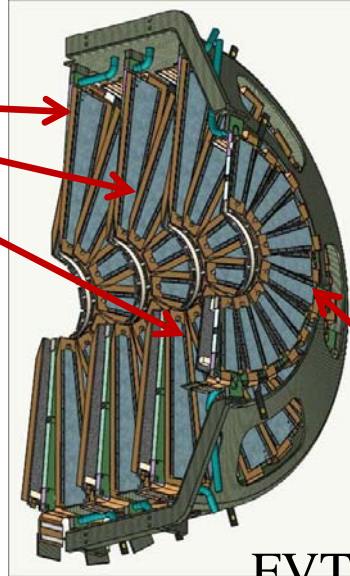
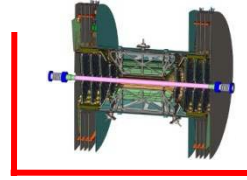


Design Decisions Leading to the FVTX Sensor Wedge and FPHX

Technical risk minimization the key driver

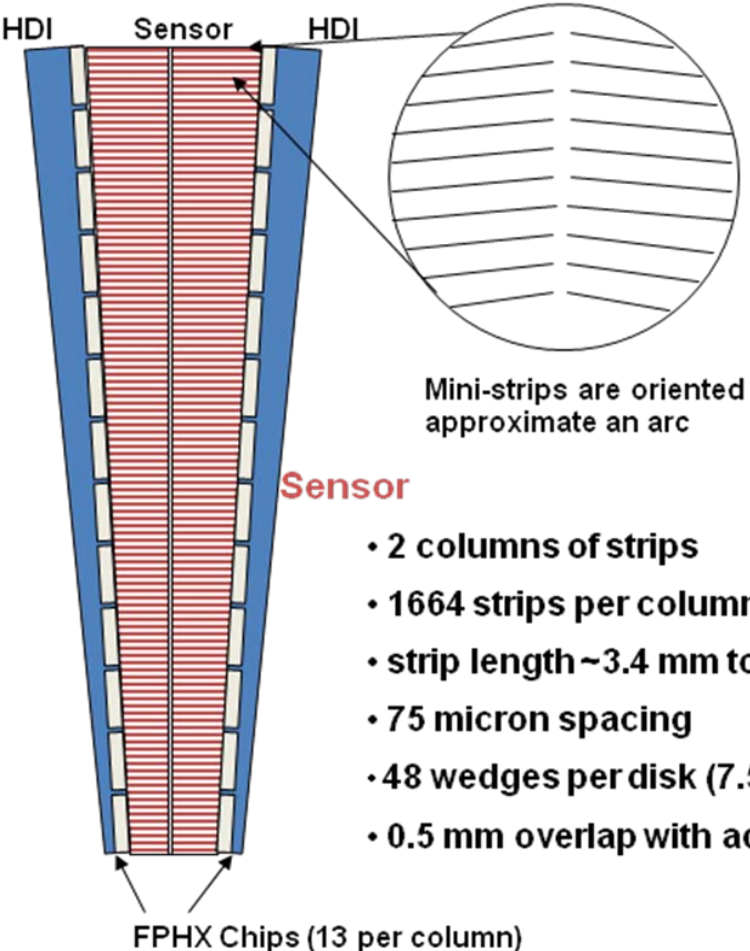
- Mini-strips maintain good resolution in r and ϕ with reasonable occupancy and manageable channel count
- Wire bonds (as opposed to bump bond design)
- Chip placement moved from centerline of sensor to the edges
 - minimizes potential noise coupling between chip and sensor
 - facilitates implementation of decoupling between sensor bias and chip reference and avoids long path-length sensor return to ground
- Wedge assembly unit based on ease of assembly (*see Dave Winter's talk later today*)

FVTX Sensor Long Wedge

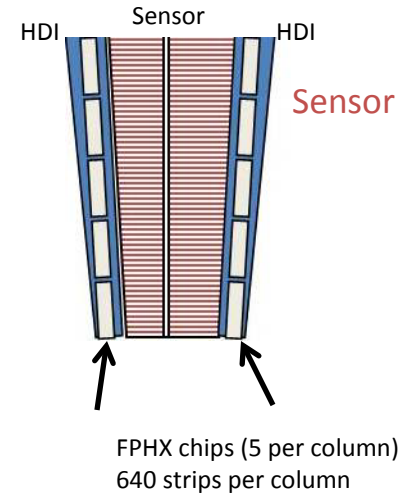


4 hermetic disks, z = 18.5 to 38 cm

FVTX Sensor Short Wedge



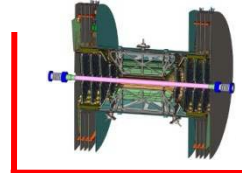
Overall length 126.8 mm
Overall width 8.8 mm i.r., 25.4 mm o.r.



Overall length 50.1 mm
Overall width 8.8 mm i.r., 15.3 o.r.

FVTX Sensors

Novel design places two independent sensors on one substrate



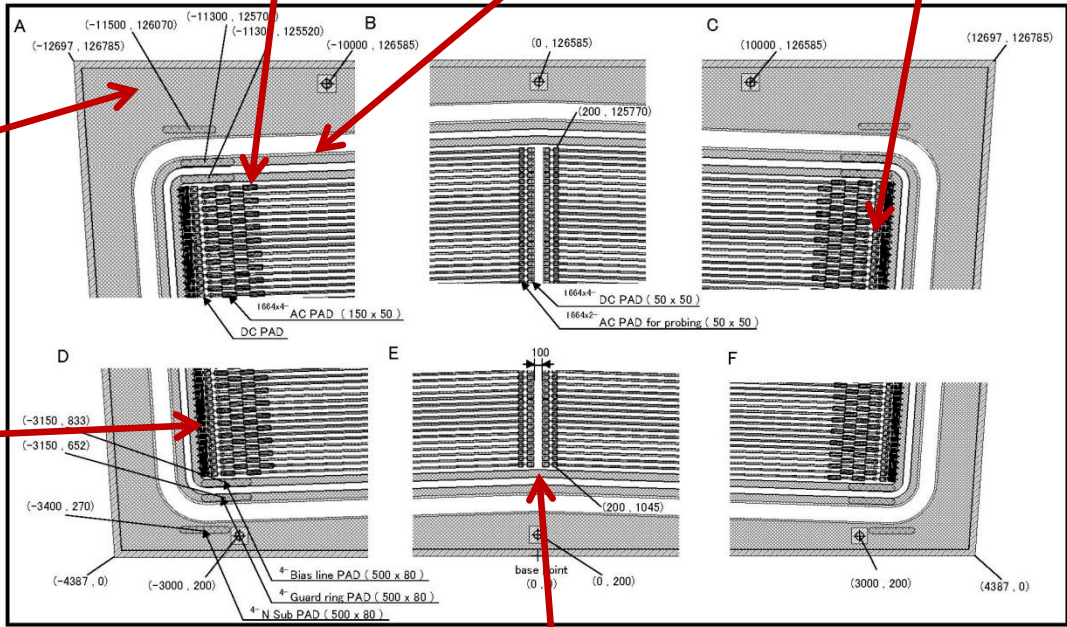
p-implant on n-bulk
ac-coupled
1.5 MΩ polysilicon bias resistors
Depletion voltage < 100V
75 micron pitch
320 microns thick



P-Bias Ring
P-Guard Ring
Double Bond-Pad Rows

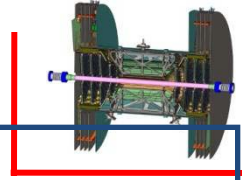
N-Surround

Polysilicon Bias Resistors



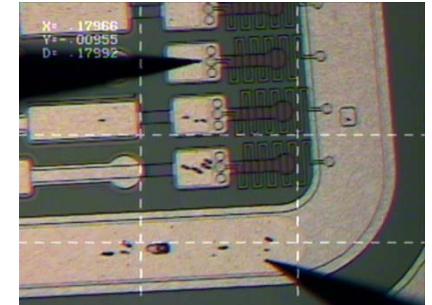
100 micron gap

QA Silicon Sensor Wedges (UNM, LANL)



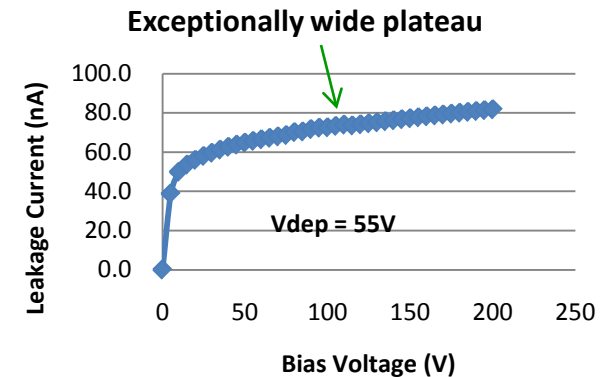
QA specifications

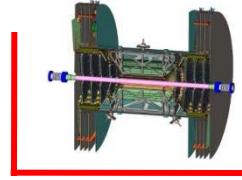
- Visual inspection to identify processing or handling flaws
- Current versus voltage characteristic curve for each sensor
- Full depletion voltage and breakdown voltage for each sensor
- Individual strips probed at UNM to confirm Hamamatsu results



Sensors delivered from Hamamatsu are fully tested

- Coupling capacitor integrity or short for each strip
- Implant open or short for each strip
- Polysilicon resistor open or short for each resistor



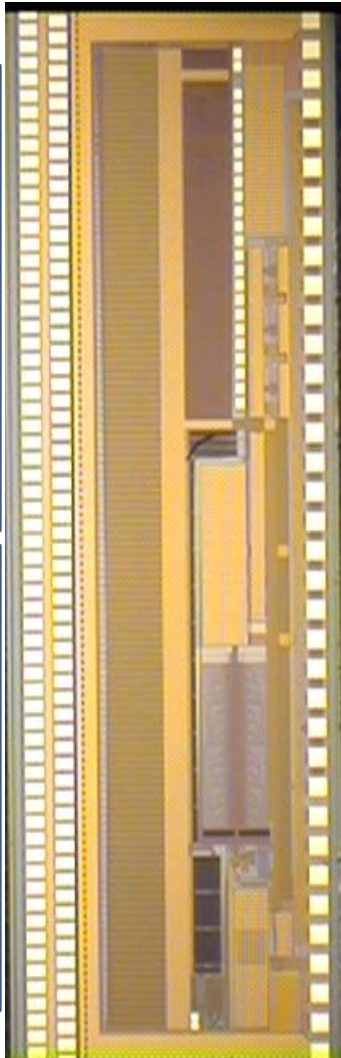


The FPHX Chip

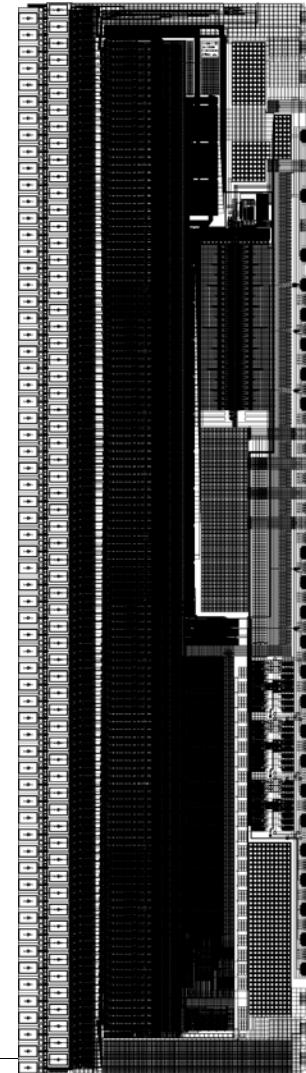
The FPHX is the custom readout chip designed for the FVTX Silicon Sensor. Each FPHX chip integrates and shapes (CR-RC) signals from 128 channels of mini-strips, digitizes and sparsifies the hit channels each beam crossing (106ns beam clock), and serially pushes out the digitized data.

- 128 channel
- 46 to 200 mV/fC
- 60 ns peak time (programmable)
- 3-bit ADC (programmable)
- Optimized for 1 to 2.5 pf
- 115e + 134e/pf
- ~ 70 to 140 uW/ch (Bias current)

- Data push architecture
- 10 MHz beam clock (BCO)
- 200 MHz data clock
- Zero suppressed
- Output 4 hits/chip in one BCO
- Approx. 300 uW/ch



Photo



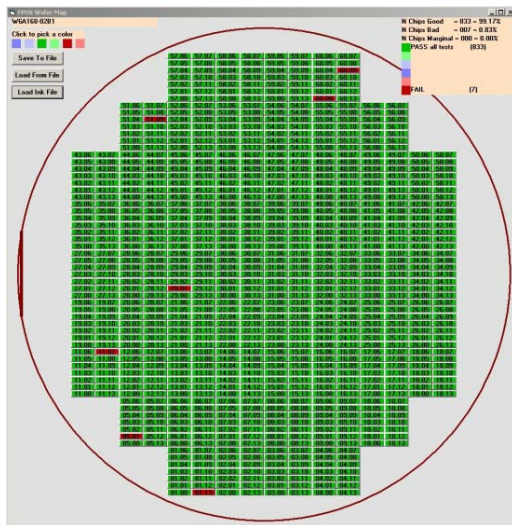
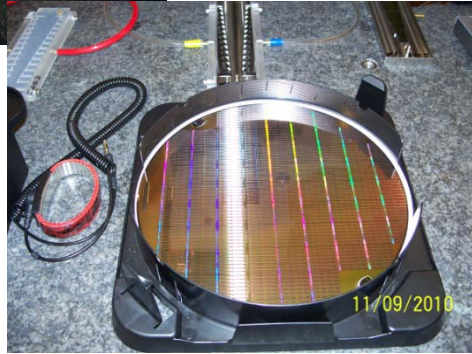
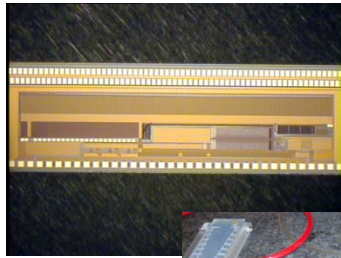
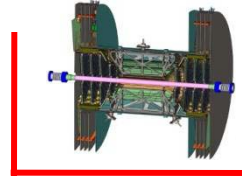
Layout

- Analog Ground
- Analog Ground 2
- Analog Power
- Substrate (Universal)
- Iset
- Substrate (Universal)
- inject Input (analog)
- Substrate (Universal)
- inject Input (digital)
- HitOR
- Reset
- Resetb
- Slow Control In
- Slow Control Inb
- Digital Power
- Digital Ground
- Digital Ground
- Digital Power
- BCOclk
- BCOclkb
- outClk
- outClkb
- Slow Control Out
- Slow Control Outb
- serialOut1
- serialOut1b
- serialOut2
- serialOut2b
- Chip ID 4
- Chip ID 3
- Chip ID 2
- Chip ID 1
- Chip ID 0
- Analog Power
- Analog Ground 2
- Analog Ground

The FPHX is a mixed-mode chip with two major and distinct sections, the front-end and the back-end.

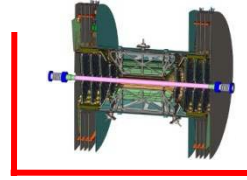
The FPHX Chip

All major functions of the FPHX tested on the wafer probe station. One wafer per day. Greater than 95% yield.



- FNAL designed FPHX-specific probe card
- FNAL developed control software to run the probe station
- FNAL developed software to run test program on the probe station
- All registers written to and read back
- Pulser scan tests run for each die
- Bad chips were inked
- All test results written to a database

Schedule For Sensors



Initial Prototype, ON-Semi – May, 2007

Current Prototype, Hamamatsu – shipped 31 October, 2008

Production Order submitted to Hamamatsu October, 2009

Production delivery 3-to-5 months ARO (partial deliveries)

Production order:

343 Large Wedge Sensors

- 288 installed in FVTX
- 55 spares

120 Small Wedge Sensors

- 96 installed in FVTX
- 24 spares

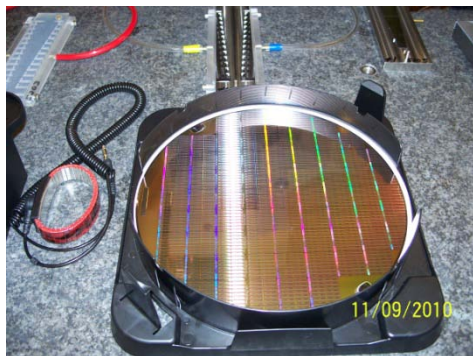
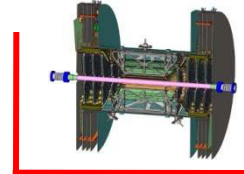
WBS	Item	Date
1.4.1.2.1	Design prototype sensor mask	06/24/08 done
1.4.1.2.2	Process prototype sensors	11/08/08 done
1.4.1.2.3	Test prototypes	02/10/09 done
1.4.1.2.4	Wire-bond sensor to FPHX	04/10/09 done
1.4.1.3.1	Submit production sensors	10/23/09 done
1.4.1.3.2	QA production sensors	04/20/2010 done

24 production wafers (approx. 20,000 die)

8448 installed in FVTX

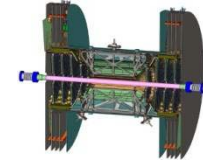
~13,000 tested die available for assembly

FPHX Schedule



WBS	item	Date
1.4.2.3	FPHX layout design	04/10/08 done
1.4.2.6	Design review	04/14/08 done
1.4.2.4.1	Submission to MOSIS	06/22/08 done
1.4.2.4.2	Prototype tests	10/10/08 done
1.4.2.4.3, 1.4.2.4.4	Submit second prototype run	06/16/09 done
1.4.2.4.5	Test second prototype	09/25/09 done
1.4.2.4.9	Second run performance review	10/01/09 done
1.4.2.5.1	Submit engineering run (production run)	12/17/09 done
1.4.2.5.2	Test production wafers	05/14/10 done
	Dice Production wafers	07/09/10

Summary



- **Sensor design, mask and prototype production complete**
- **Sensor QA complete**
- **Production sensor order complete**
- **FPHX first round fully functional prototype complete**
- **Bench tests validate analog and digital performance specs**
- **FPHX second round complete**
- **Second round changes perform as expected**
- **FPHX production complete**
- **FPHX probe station tests complete**
- **FPHX wafers diced and delivered to SiDet**